

Agenda Item:

Source: SAMSUNG Electronics Co.

Title: Additional simulation results of rate matching algorithm in uplink

Document for: Discussion

1. Introduction

This document supplements Tdoc [1] and [2] proposed by Samsung and LGIC with some additional simulation results for uplink over AWGN channel.

2. Simulation conditions

For turbo codes, the simulation conditions are as follows

- Block sizes: 324, 644, 964 for uplink
- Puncturing rates: P=20, 15, 10, 5%
- Decoding algorithm: Log MAP decoder
- Turbo interleaver: PIL
- Number of iterations: 8
- Number of frame errors: greater than 100
- Channel model: AWGN
- Algorithms: SEC & LGIC puncturing

In the following figures, _20, _15, _10, and _5 mean puncturing with P=20, 15, 10, and 5, respectively[1],[2]. Notation of (a,b,a,b) means the following parameters for each rate matching block (RMB).

(a,b,a,b)	RMB1	RMB2	RMB3
(2,1,2,1)	Not used	(a,b)=(2,1)	(a,b)=(2,1)
(2,1,1,1)	Not used	(a,b)=(2,1)	(a,b)=(1,1)

3. Results and conclusion

In Figure 1, 2, and 3, with interleaver sizes of 324, 644, and 964, the performance decrease in proportion to the puncturing parameter p. In the figures, (a,b) parameters are fixed to (2,1,2,1). According to simulation results, it was shown that the proposed rate matching scheme provides similar performance in uplink compared with performance in downlink. Also, the performance of high rate code decreases in proportion to the puncturing parameter p. In Figure 4, 5, and 6, with interleaver sizes of 324, 644, and 964, the performance decrease in proportion to the puncturing parameter p. In the figures, (a,b) parameters are fixed to (2,1,1,1). It is shown that performance with (2,1,1,1) is slightly better than the performance with (2,1,2,1).

4. References

- [1] "Unified rate matching scheme for Turbo/convolutional codes and up/down links", Samsung Electronics Co., TSGR1#6(99)919
- [2] "Unified rate matching scheme for turbo codes in both uplink and downlink", Samsung Electronics Co. and LGIC, TSGR1#6(99)a30

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interleaver size=324, PIL, iteration=8, Seg=8, Frame Error count=100, (2,1,2,1), Uplink

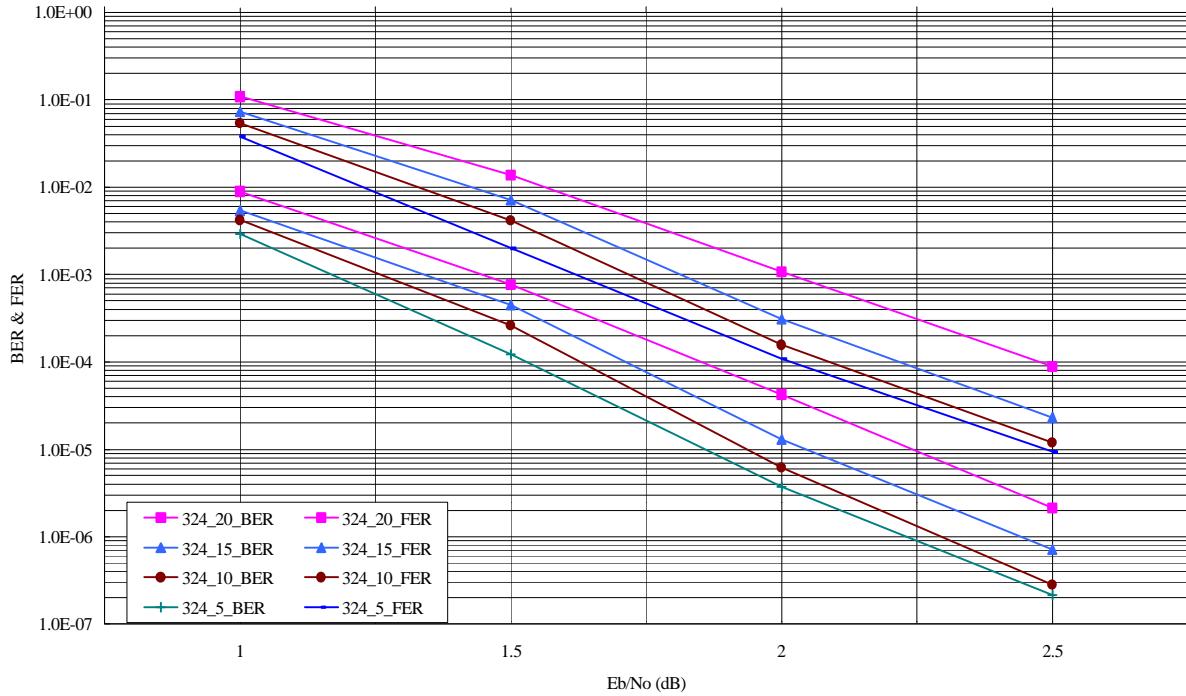


Fig. 1. BER and FER performance of turbo codes (2,1,2,1). (N=324, P= 20,1 5, 10, 5%).

interleaver size=644, PIL, iteration=8, Seg=8, Frame Error count=100,(2,1,2,1), Uplink

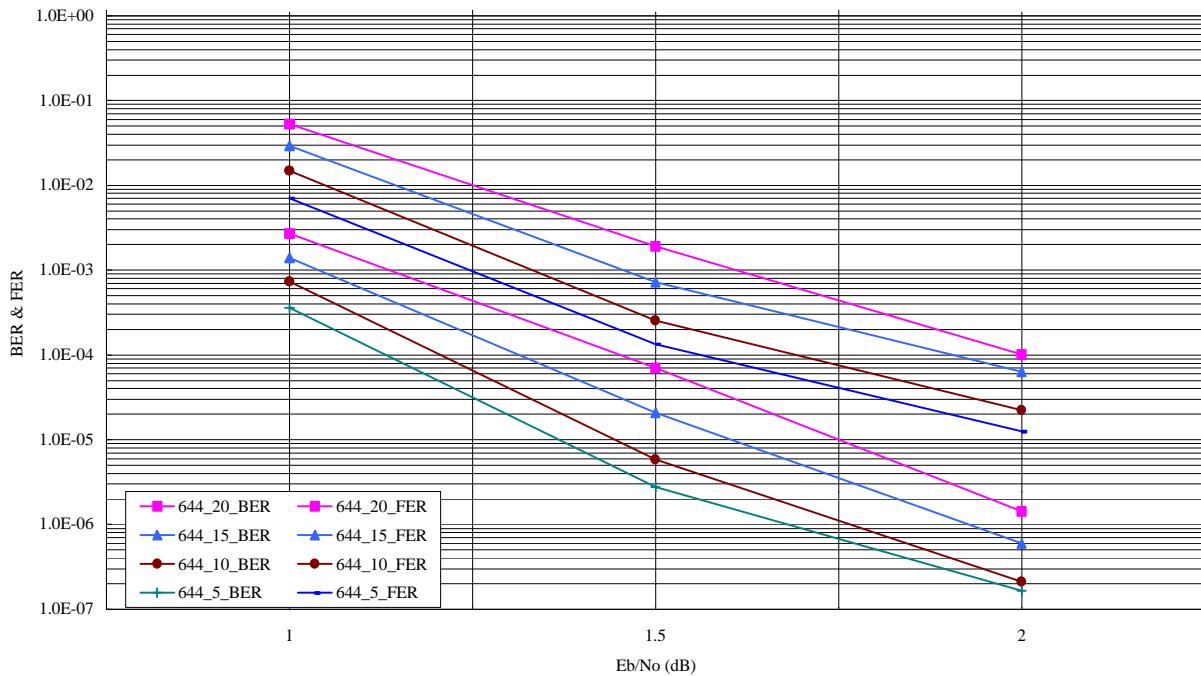


Fig. 2. BER and FER performance of turbo codes (2,1,2,1). (N=644, P= 20,1 5, 10, 5%)..

interleaver size=964, PIL, iteration=8, Seg=8, Frame Error count=100, (2,1,2,1), Uplink

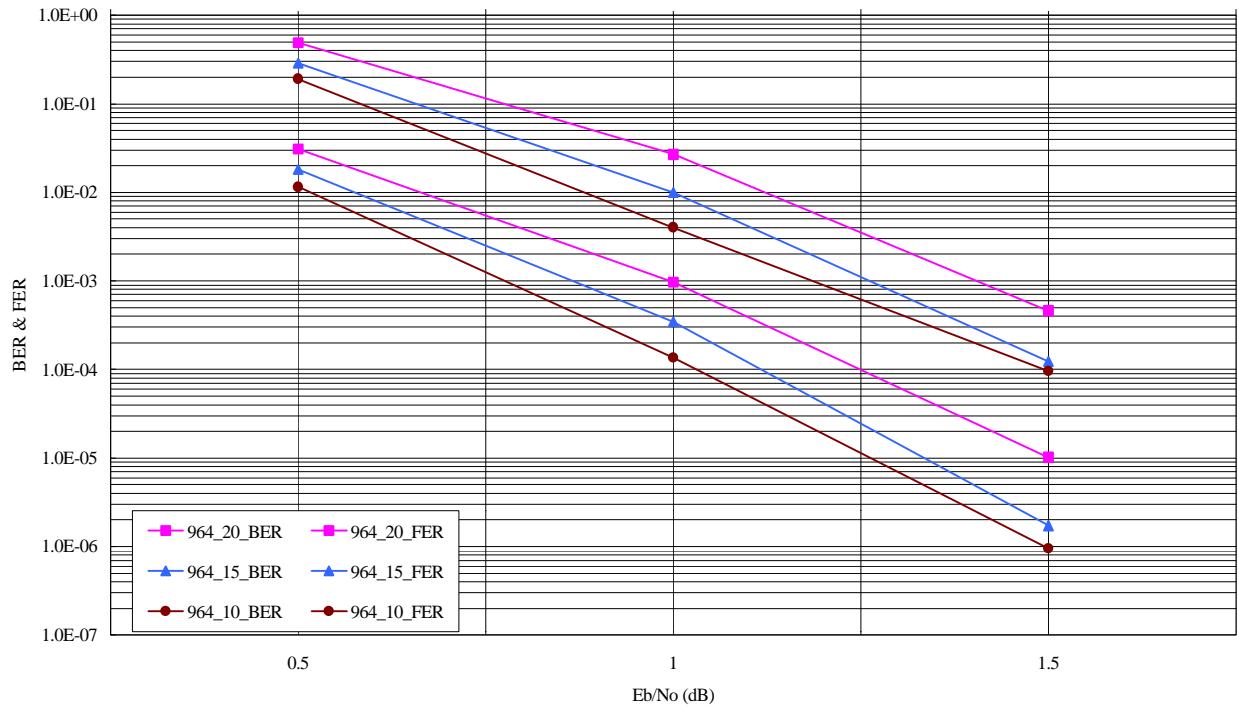


Fig. 3. BER and FER performance of turbo codes (2,1,2,1). (N=964, P= 20,1 5, 10%).

interleaver size=324, PIL, iteration=8, Span=80msec, Frame Error count=100, (2,1,1,1), Uplink

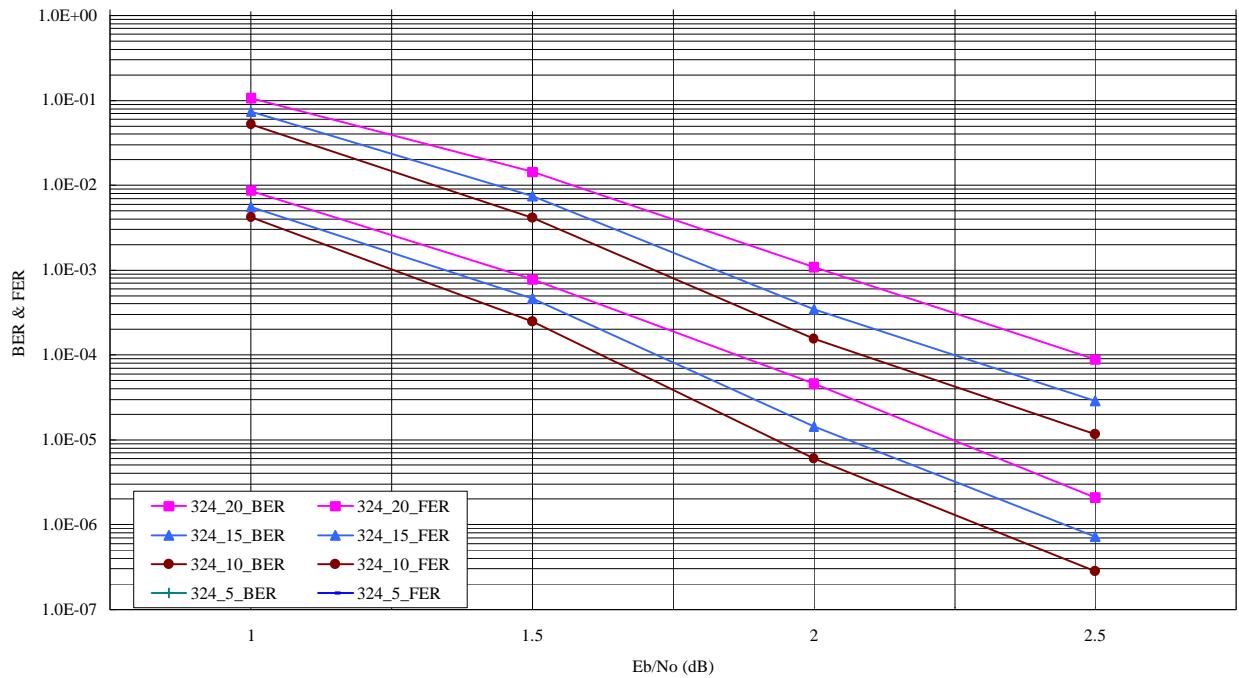


Fig. 4. BER and FER performance of turbo codes (2,1,1,1). (N=324, P= 20,1 5, 10%).

interleaver size=644, PIL, iteration=8, Span=80msec, Frame Error count=100,(2,1,1,1), Uplink

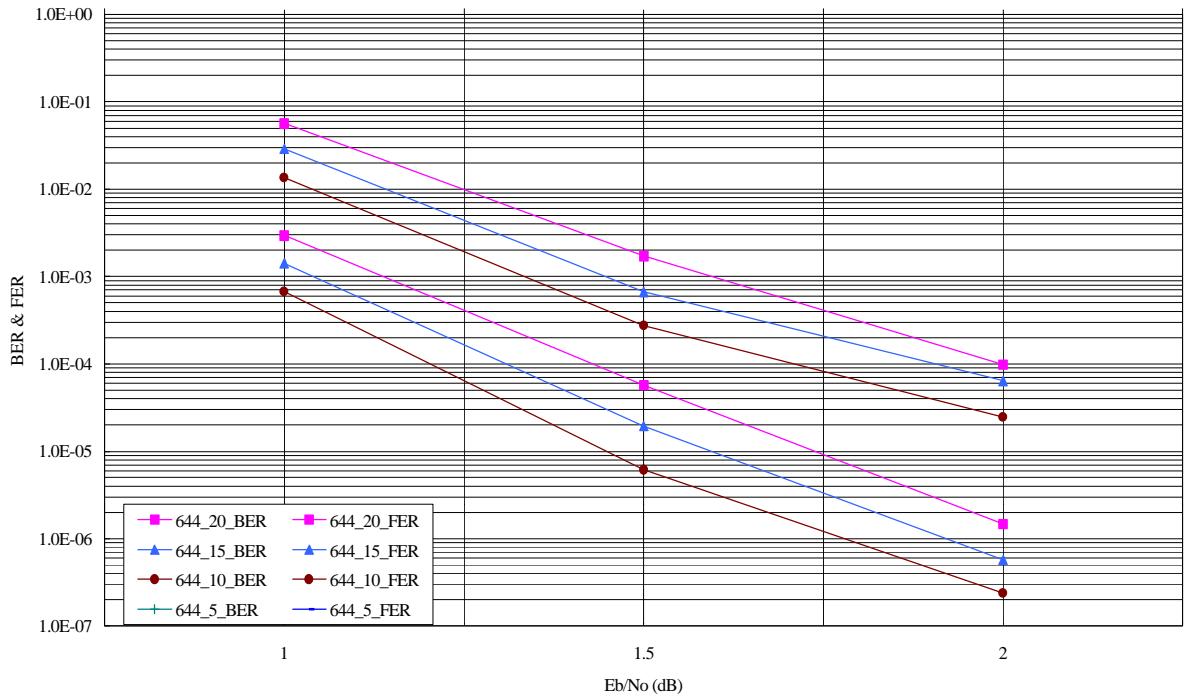


Fig. 5. BER and FER performance of turbo codes (2,1,1,1). (N=644, P= 20,1 5, 10%).

interleaver size=964, PIL, iteration=8, Span=80msec, Frame Error count=100, (2,1,1,1), Uplink

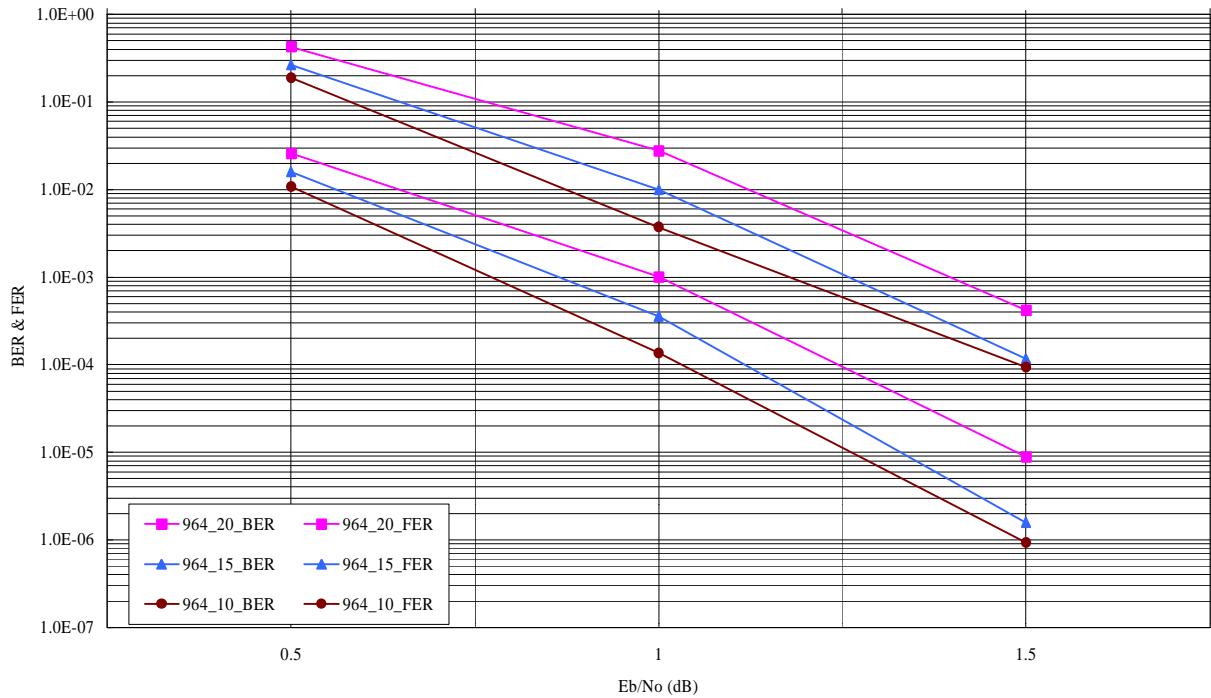


Fig. 6. BER and FER performance of turbo codes (2,1,1,1). (N=644, P= 20,1 5, 10%).