TSG RAN 1#7 TSG R1#7(99)B96 Hannover, Germany Aug 30 – Sep 3, 1999

Agenda Item:

Source: CCL/ITRI

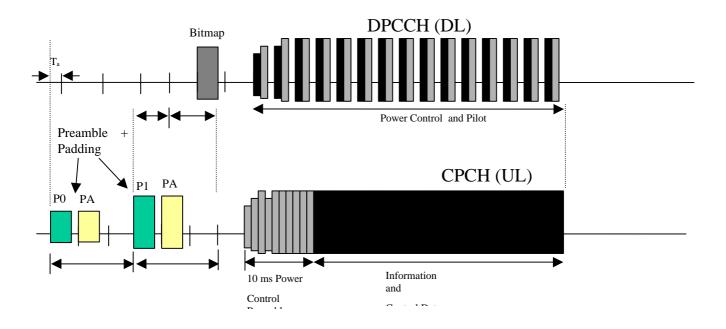
Title: Questions & Answers of CCL/ITRI's MAC Procedures for CPCH

**Document for:** Discussion and Decision/Information

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Abstract: This contribution describes the questions and answers of CCL/ITRI's MAC scheme for random packet data access over CPCH. Details of the MAC scheme and the physical layer supporting for the MAC procedures are described in TSG R1#7(99)B03 and TSG R1#7(99)B95, respectively.

- Q1. What is the difference between the approaches proposed by CCL/ITRI and GBT?
- **A1:** The timing diagram of the MAC procedures proposed by CCL/ITRI and GBT are shown in Fig.1 and Fig. 2, respectively. Fig. 3 depicts the timing diagram of MAC procedures regarding the handshake after the power ramp-up and before data transmission. GBT's procedures involve 4-way handshake while CCL/ITRI's proposal is a 2-way handshake.



**Figure 1.** The timing diagram of the CCL/ITRI's MAC protocol.

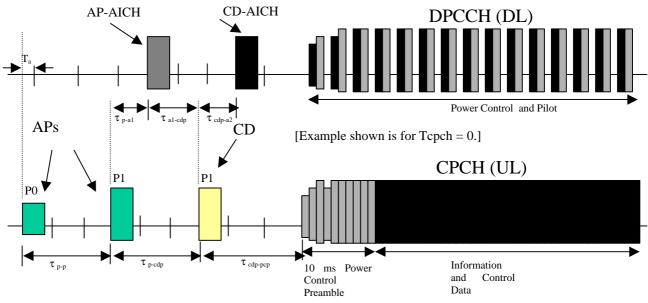
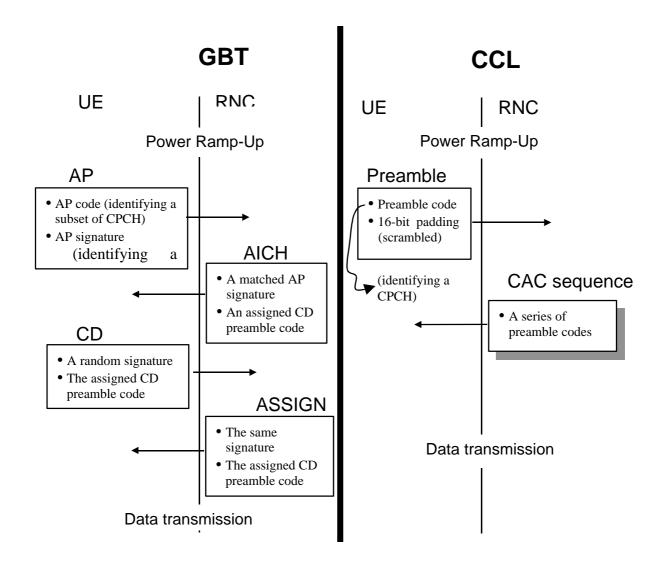


Figure 2. The timing diagram of the GBT's MAC protocol.

Both approaches use CPCH for uplink access and AICH for downlink acknowledgment. The power ramping procedure and the data transmission procedure of the two approaches are identical. Therefore, the same procedures applicable in GBT's approach would be applicable in CCL/ITRI's approach.

The major difference between CCL/ITRI's approach and GBT's approach is that the former uses 2-way handshake while the latter requires 4-way to complete handshake. Therefore, CCL/ITRI's approach greatly reduces the access time. The overhead introduced by CCL/ITRI's approach is the use of padding for contention resolution.



**Figure 3.** Timing diagram of two MAC procedures.

## **Q2.** What is the padding?

## A2: The padding is 16-bit in length and is used for contention resolution.

Figure 4 shows the structure of the 16-bit padding. Each padding consists of two parts, a data part that carries padding information and a control part that carries pilot bits. The data and control parts are transmitted in parallel. In the data part, a 12-bit random number in associated with a 4-bit CRC are used for contention resolution.

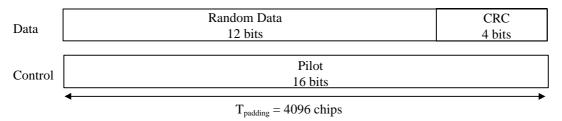


Figure 4. Structure of the 16-bit padding.

The data part consists of 16 bits. The spreading factor of the data part is 256. This corresponds to a total length of 16\*256 = 4096 chips. The control part consists of 16 known pilot bits to support channel estimation for coherent detection. The spreading factor of the control part is 256. This corresponds to the

same total length of 4096 chips. The 16 pilot bits are block repetition of two identical 8-bit pilot used in uplink DPCCH (see TS 25.211 for more detail).

- **Q3.** What is the scrambling code for padding?
- A3: The scrambling code used for the padding is cell-specific and has a one-to-one correspondence to the spreading code used for the preamble. This corresponds to sixteen scrambling codes for each cell. The scrambling codes used are the same set of codes as is used for the other dedicated uplink channels when the long scrambling codes are used for these channels. The first 256 of the long scrambling codes are used for the random access channel. The phases 4096..8192 of the codes are used for the padding (phases 0..4095 of c1 are used in preamble spreading) with the chip rate of 3.84 Mchips/s (See TS 25.213 for detail description of these codes).
- **Q4.** Does the padding affect the power ramping procedure?
- A4: The answer to this question is 'No.'

The length of the padding is 16-bit. Therefore, the transmission of the padding is equal to the duration of an access slot (the duration is named a time offset). In the power ramping procedure using RACH or CPCH, the time duration between two access preamble is at least  $T_{BO1}$ , which should be larger than one time offset. Thus, the power ramping procedure will not be affected.

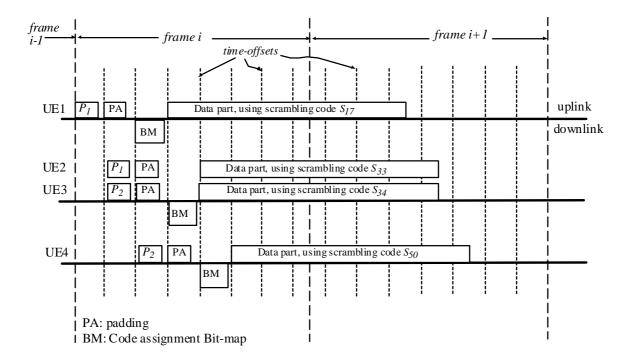
- Q5. Could the BS send 'Nack' message using CCL/ITRI's approach?
- A5. The answer to this question is 'Yes.'

After UTRAN has determined all the successful Random-Access attempts, it will use Acquisition Indicator Channel (AICH) to notify the UE of its success or failure. A code-assignment bitmap will be used for advertising the successful attempts. The bitmap consists of 16 acquisition indicator (AIi, i=1..16) transported by AICH, as shown in Figure 2. The acknowledgement represented by this bitmap reflects three conditions. AIi=+1 indicates that the RNC has successfully received preamble Pi and its following padding scrambled by Si. Similarly, AIi=-1 indicates that the RNC did not correctly received preamble Pi and its following padding scrambled by Si. If an UE first chooses preamble Pi for contention, and later in the data transmission phase, if an UE detects in the bitmap that the corresponding bit position i is +1(That is, AIi=+1), then this UE is permitted to send its data part in the data transmission phase. Otherwise, if AIi in the bitmap is -1, or this UE does not receive the sequence of bitmap correctly, it assumes that it fails in this frame and will make a retry in one of the coming frames. Since a failed Random-Access attempt will not transmit its data part, there is no unnecessary interference to the normal data transmission. Finally, AIi=0 indicates that there is no Random-Access attempt on preamble Pi in this time-offset.

- **Q6.** Who is responsible for sending the 'Code Assign Bitmap' via AICH as shown in Fig. 1?
- A6: The node-B is responsible for the acknowledgment to minimize the access delay.
- Q7. Does CCL/ITRI's approach supports parallel data transmission?
- A7: The answer to this question is 'Yes.'

In GBT's approach, the node-B can only acknowledge one successful UE via AICH. The same process should be repeated to support multiple UEs transmitting at the same time.

On the contrary, CCL/ITRI's approach can support parallel data transmission by sending the group acknowledgment via 'Code Assign Bitmap.' An example parallel data transmission using CCL/ITRI's apporach is shown in Fig. 5



**Figure 5.** Parallel data transmission in CCL/ITRI's MAC protocol.