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Title: A Modified Mapping Rule for Multiple-Scrambling Codes

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Introduction

In the current 3GPP specification [1], the downlink scrambling code number is defined directly by the initialisation value of the scrambling code generator, which was introduced in [2]. This makes the initial value loading very easy. However, in a case where UE has to generate two scrambling codes in order to receive a common pilot channel with primary scrambling code (PSC) and data channel with secondary scrambling code (SSC), it is desirable that multiple scrambling codes are generated simultaneously by using a single generator with a simple masking function. For this purpose, the contribution of [3] proposes the mapping rule where the initial state of n:th scrambling code is calculated by (n-1) phase shifts of first scrambling code. But, this mapping rule makes the initialisation somewhat complex.

This paper proposes a new mapping rule that takes advantages of the previous two methods. The proposed method assumes that the number of SSC's per PSC is approximately 16. In the proposed mapping rule, the initial state of generator for PSC is related to the PSC number and the initial state of m:th SSC corresponding to n:th PSC is calculated by m phase shifts of n:th PSC.

The proposed method makes the loading of initial value easier and only requires a single generator for generating PSC and SSC, simultaneously. Moreover, this method needs only a small change from the current scheme.

Generation of scrambling code

There are a total 512*(M+1) scrambling codes. The scrambling codes are divided into 512 sets each of which comprises one PSC and M SSC's.

The PSC's are numbered by n=0, 1, 2, …, 511. The n:th set of SSC's that corresponds to n:th PSC are numbered by $n^{(1)}$, $n^{(2)}$, $n^{(3)}$, …. , $n^{(M)}$.

In the proposed method, the initial conditions for generating n:th PSC (n=0,1,2 , … ,511) and $n^{(m)}$:th SSC (m=1,2, … ,M) are defined by table 1 (option 1) or table 2 (option 2) in case of M=16.

In the tables, n_8 n_7 n_6 … n_0 is the binary representation of the number n.

It should be noted that 512*17 scrambling codes obtained by the tables are all distinct.

The initial conditions for PSC in these tables can be also used in case of M=24. In which case, 512*25 scrambling codes are all distinct. There are many initial patterns for PSC that satisfy this property. As other example, the initial pattern for PSC in table 3 (option 3) can be used until M < 71. However, The simple initial pattern in table 1 is preferred if the required number of SSC's per PSC is 16.

In conclusion, the proposed mapping rule of scrambling codes makes the initialisation of the generator easier as in the current specification. Also, multiple scrambling codes in one cell can be generated simultaneously by using a single generator shown in Figure1 with simple masking functions shown in Table 4 as in [3].

Reference

[1] TS 25.213 V2.1.2: 'Spreading and modulation (FDD)', Source: Editor

[2] Tdoc 3GPP WG1 TSGR1#6 (99)724 : 'Multiple Scrambling Codes', Source: Ericsson

[3] Tdoc 3GPP WG1 TSGR1#6 (99)915 : 'Multiple-Scrambling Code', Source: Samsung

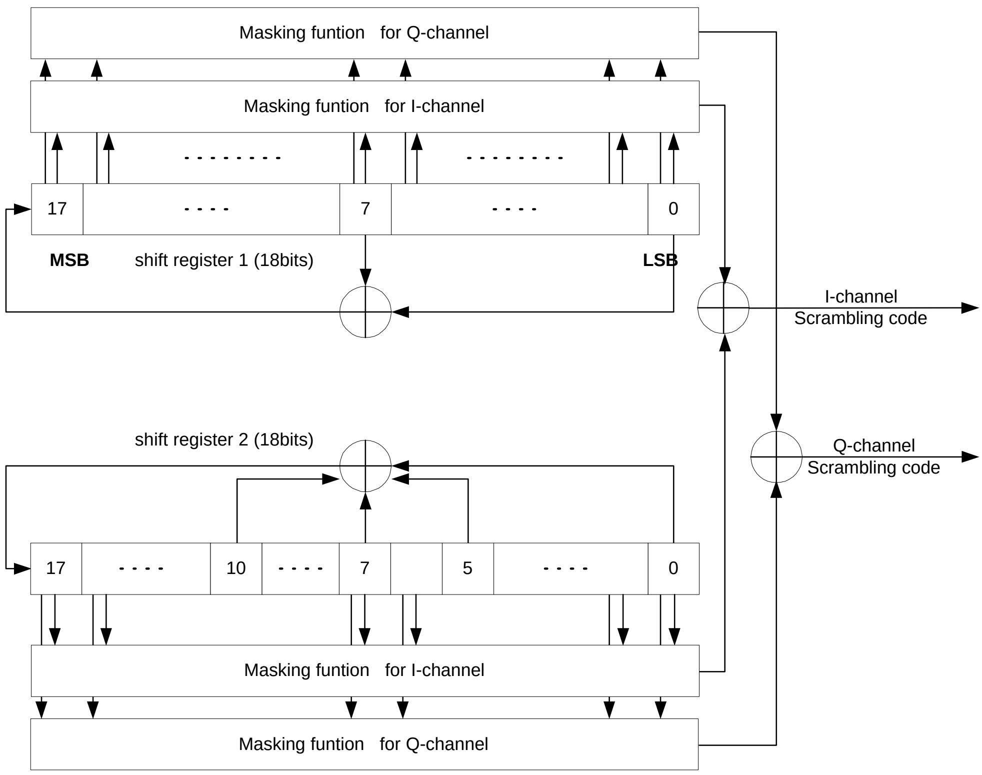

Figure 1. Structure of multiple scrambling code generator

Table 1. Initial Condition (option 1)

	x_{17}	x_{16}	x_{15}	x_{14}	x_{13}	x_{12}	x_{11}	x_{10}	x_9	x_8	x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0
P	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2	n_1	n_0	0	0	0	0	0	0	0
S_1	n_0	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2	n_1	n_0	0	0	0	0	0	0
S_2	n_1	n_0	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2	n_1	n_0	0	0	0	0	0
S_3	n_2	n_1	n_0	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2	n_1	n_0	0	0	0	0
S_4	n_3	n_2	n_1	n_0	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2	n_1	n_0	0	0	0
S_5	n_4	n_3	n_2	n_1	n_0	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2	n_1	n_0	0	0
S_6	n_5	n_4	n_3	n_2	n_1	n_0	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2	n_1	n_0	0
S_7	1	n_5	n_4	n_3	n_2	n_1	n_0	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2	n_1	n_0
S_8	$n_0 \oplus n_6$	1	n_5	n_4	n_3	n_2	n_1	n_0	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2	n_1
S_9	$n_1 \oplus n_7$	$n_0 \oplus n_6$	1	n_5	n_4	n_3	n_2	n_1	n_0	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2
S_{10}	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	1	n_5	n_4	n_3	n_2	n_1	n_0	1	n_8	n_7	n_6	1	n_5	n_4	n_3
S_{11}	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	1	n_5	n_4	n_3	n_2	n_1	n_0	1	n_8	n_7	n_6	1	n_5	n_4
S_{12}	$n_4 \oplus n_0$	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	1	n_5	n_4	n_3	n_2	n_1	n_0	1	n_8	n_7	n_6	1	n_5
S_{13}	$n_5 \oplus n_1$	$n_4 \oplus n_0$	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	1	n_5	n_4	n_3	n_2	n_1	n_0	1	n_8	n_7	n_6	1
S_{14}	$1 \oplus n_2$	$n_5 \oplus n_1$	$n_4 \oplus n_0$	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	1	n_5	n_4	n_3	n_2	n_1	n_0	1	n_8	n_7	n_6
S_{15}	$n_6 \oplus n_3$	$1 \oplus n_2$	$n_5 \oplus n_1$	$n_4 \oplus n_0$	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	1	n_5	n_4	n_3	n_2	n_1	n_0	1	n_8	n_7
S_{16}	$n_7 \oplus n_4$	$n_6 \oplus n_3$	$1 \oplus n_2$	$n_5 \oplus n_1$	$n_4 \oplus n_0$	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	1	n_5	n_4	n_3	n_2	n_1	n_0	1	n_8

Table 2. Initial Condition (option 2)

	x_{17}	x_{16}	x_{15}	x_{14}	x_{13}	x_{12}	x_{11}	x_{10}	x_9	x_8	x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0
P	0	0	0	0	0	0	0	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2	n_1	n_0
S_1	$n_0 \oplus n_6$	0	0	0	0	0	0	0	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2	n_1
S_2	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0	0	0	0	1	n_8	n_7	n_6	1	n_5	n_4	n_3	n_2
S_3	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0	0	0	0	1	n_8	n_7	n_6	1	n_5	n_4	n_3
S_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0	0	0	0	1	n_8	n_7	n_6	1	n_5	n_4
S_5	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0	0	0	0	1	n_8	n_7	n_6	1	n_5
S_6	n_5	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0	0	0	0	1	n_8	n_7	n_6	1
S_7	1	n_5	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0	0	0	0	1	n_8	n_7	n_6
S_8	n_7	1	n_5	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0	0	0	0	1	n_8	n_7
S_9	n_6	n_7	1	n_5	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0	0	0	0	1	n_8
S_{10}	n_8	n_6	n_7	1	n_5	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0	0	0	0	1
S_{11}	1	n_8	n_6	n_7	1	n_5	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0	0	0	0
S_{12}	$n_0 \oplus n_6$	1	n_8	n_6	n_7	1	n_5	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0	0	0
S_{13}	$n_1 \oplus n_7$	$n_0 \oplus n_6$	1	n_8	n_6	n_7	1	n_5	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0	0
S_{14}	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	1	n_8	n_6	n_7	1	n_5	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0	0
S_{15}	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	1	n_8	n_6	n_7	1	n_5	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0	0
S_{16}	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	1	n_8	n_6	n_7	1	n_5	n_4	$n_3 \oplus 1$	$n_2 \oplus n_8$	$n_1 \oplus n_7$	$n_0 \oplus n_6$	0	0

Table 3. Initial Condition (option 3)

	x_{17}	x_{16}	x_{15}	x_{14}	x_{13}	x_{12}	x_{11}	x_{10}	x_9	x_8	x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0
P	1	0	n_8	1	0	n_7	n_6	1	0	n_5	n_4	0	n_3	n_2	n_1	0	n_0	0

Table 4. Masking functions for generating multiple scrambling codes in one cell

	masking function for I code in upper LFSR	masking function for Q code in upper LFSR	masking function for I code in lower LFSR	masking function for Q code in lower LFSR
PSC	000000000000000001	001000000001010000	000000000000000001	001111111101100000
1st SSC	000000000000000010	010000000010100000	000000000000000001	001111111101100000
2nd SSC	000000000000000100	100000000101000000	000000000000000001	001111111101100000
3rd SSC	000000000000001000	000000001000000001	000000000000000001	001111111101100000
4th SSC	000000000000010000	000000010000000010	000000000000000001	001111111101100000
5th SSC	000000000000100000	000000100000000100	000000000000000001	001111111101100000
6th SSC	000000000001000000	000001000000001000	000000000000000001	001111111101100000
7th SSC	000000000010000000	000010000000010000	000000000000000001	001111111101100000
8th SSC	000000000100000000	000100000000100000	000000000000000001	001111111101100000
9th SSC	000000001000000000	001000000001000000	000000000000000001	001111111101100000
10th SSC	000000010000000000	010000000010000000	000000000000000001	001111111101100000
11th SSC	000000100000000000	100000000100000000	000000000000000001	001111111101100000
12th SSC	000001000000000000	000000001010000001	000000000000000001	001111111101100000
13th SSC	000010000000000000	000000010100000010	000000000000000001	001111111101100000
14th SSC	000100000000000000	000000101000000100	000000000000000001	001111111101100000
15th SSC	001000000000000000	000001010000001000	000000000000000001	001111111101100000
16th SSC	010000000000000000	000010100000010000	000000000000000001	001111111101100000