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Agenda item:

Source: Ericsson

Title: DPCH synchronisation

Document for: Decision

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1 Introduction

The information on the DPCH synchronisation procedure between NodeB (NB) and UE is at present somewhat unclear in the 3GPP documentation. In particular, issues relating to the steady-state TX and RX transmission timings of NB and UE have not been described in sufficient detail. In this paper, we discuss issues related to TPC loop delay and DPCH synchronisation, and propose the following:

- The UE shall be allowed to adjust its DPCH TX timing at a certain maximum rate of change, at least when not in soft Handover. We propose that this maximum rate of change is 1/4 chip over a 10 ms period.
- There is a need for a procedure where the UE or NB requests an adjustment of the NB DPCH TX timing by a certain number of symbols. The adjustment needs to be done in a synchronised manner, i.e. by using a counter. This proposal is in line with [2].

2 Notations

$T_{NB,TX,i}$: Time instant of the beginning of a Radio Frame transmitted from NB antenna of cell *i*.

$T_{NB,RX,i}$: Time instant of the beginning of a Radio Frame received at NB antenna (first significant path) of cell *i*.

$T_{UE,TX}$: Time instant of the beginning of a Radio Frame transmitted from UE antenna.

$T_{UE,RX,i}$: Time instant of the beginning of a Radio Frame received from cell *i* at UE antenna (first significant path).

$T_{NB,TX.-RX,i}$: $T_{NB,TX,i} - T_{NB,RX,i}$

$T_{UE,TX.-RX,i}$: $T_{UE,TX} - T_{UE,RX,i}$

T_o : A constant value = 1024 chips [1]

3 DPCH Synchronisation

3.1 Scenario

Assume that the UE sets up a first DPCH to cell *i*, and subsequently two more DPCHs to cells *j* and *k*. Figure 1 shows the resulting timing situation in the UE.

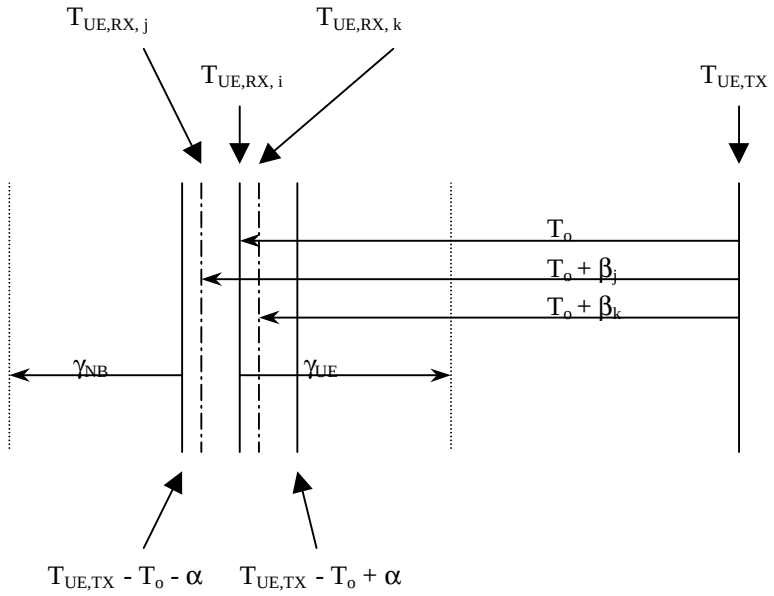

Figure 1: UE Timing.

The first added cell, *i*, will be received exactly T_o prior to $T_{UE,TX}$, since the UE actually sets $T_{UE,TX}$ so that this condition is fulfilled. We denote this time instant the "nominal" timing. Every added cell after this will end up within the window $T_{UE,TX,} - T_o \pm \alpha$, where α is 128 chips (32 μs).
Due to UE movement and NB-UE frequency errors, the timings $T_{UE,RX,n}$, $n=i,j,k$ will now move in relation to $T_{UE,TX}$.
If $T_{UE,TX} - T_{UE,RX,n} \leq \gamma_{UE}$ for any *n*, then the processing budget in the UE for keeping a 1-slot TPC loop delay is threatened. The UE then has to disregard the TPC symbol from that cell, or else a 1-slot UL TPC loop delay cannot be maintained for the radio link.
Similarly, if $T_{UE,TX} - T_{UE,RX,n} \geq \gamma_{NB}$ for any *n*, then the processing budget in the NB controlling that cell will be threatened. The exact values of γ_{UE} and γ_{NB} depend on UE and NB implementation.

There is thus a need for some kind of timing adjustment mechanism in order to keep $T_{UE,RX,n}$ reasonably close to the nominal timing for all the cells in the active set.

3.2 Solutions

There are in principle two possible solutions:

1. **Adjustment of $T_{UE,TX}$.**
   Pros: Does not require any L3 signalling or specific synchronisation procedure, since the UE could change the timing in such small steps that the NB searcher can take care of the change.
   Cons: Can probably not be used if the active set consists of cells controlled by two or more NBs, since if the UE adjusts the timing for one cell, it may make it worse for another cell.

2. **Adjustment of $T_{NB,TX,n}$.**
   Pros: Can be used for any active set size.
   Cons: Requires L3 signalling over U_u and I_{ub}, and a synchronisation procedure between NB and UE, since the NB can only change the timing in steps of whole channel symbols.

It can be assumed that at least 50% of the UEs in DCH connected state do not have an active set consisting of cells controlled by two or more NBs. Therefore, there is a potential gain in reduced signalling if solution 1 is used for these cases. The gain from this depends on cell sizes, handover algorithm thresholds and requirements on frequency synchronisation, including the maximum periodicity of the frequency jitter. Until it has been shown that the gain from reduced signalling is negligible, we propose that solution 1 should be allowed for UEs that do not have an active set consisting of cells controlled by two or more NBs. A maximum rate of change of $T_{UE,TX}$ must then be specified in 25.214.

For solution 2, which was also proposed in [2], a synchronised mechanism is needed so that the time instant and size of the shift is known by the UE. The request for a timing change can be triggered by the UE (when the UE processing budget is threatened) or by the NB (when the NB processing budget is threatened). There is thus a need for new L3 messages, both on U_u and I_{ub}/I_{ur}.

4 Proposal

We propose the following:

DPCH timing adjustment in order to maintain a 1-slot TPC loop delay shall be possible through the use of two mechanisms:

- Adjustment of $T_{NB,TX,n.}$, triggered by UE or NB controlling cell *n* (for all cases)
- Adjustment of $T_{UE,TX}$, triggered by UE (at least when not in soft handover)

The first mechanism requires the following:

- Criteria for triggering (NB, UE): Not specified in WG1 specifications.
- Signalling procedure for NB triggered adjustment (NB-RNC, RNC-UE): Not specified in WG1 specifications.
- Signalling procedure for UE triggered adjustment (UE-RNC, RNC-NB): Not specified in WG1 specifications.

The second mechanism requires the following:

- Maximum allowed rate of change of $T_{UE,TX}$ (UE): Specified in TS 25.214.

A text proposal for 25.211 and 25.214 is included in the next sections. The text proposal also tries to improve the readability of the synchronization section in general.

5 Text proposal for 25.211 V2.2.1

7.1 DPCCH/DPDCH timing relations

7.1.1 Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

7.1.2 Downlink

In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

7.1.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of T_0 can be found in TS 25.214 section 4.5.

6 Text proposal for 25.214 V1.1.1

Below is a text proposal. Note that the figures have been modified to not be in contradiction to the text. In our view the figures can be removed from the specification, if they are not removed they need some polishing to look nice and be correct.

4.5.2 No existing uplink dedicated channel

The assumption for this case is that a DPCCH/DPDCH pair shall be set up in both uplink and downlink, and that there exist no uplink DPCCH/DPDCH already. This corresponds to the case when a dedicated physical channel is initially set up on a frequency.

The ~~outline of~~ synchronization establishment procedures of the dedicated physical channel is described below. The ~~detailed~~ synchronization establishment process flow is shown in Figure 2.

a) UTRAN~~The network~~ starts the transmission of downlink DPCCH/DPDCHs~~channels~~. ~~The TPC commands transmitted by the network follows a predetermined pattern,~~ .The DPDCH is transmitted only when there is data to be transmitted to the UE.

b) The UE establishes downlink chip synchronization and frame synchronization based on the ~~Primary CCPCH~~CPICH ~~synchronization~~ timing and timing offset information~~the frame offset group, slot offset group~~ notified from UTRAN~~the network~~. F~~The f~~rame synchronization can~~ould~~ be confirmed using the Frame Synchronization Word. Successful frame synchronization is confirmed and reported to the higher layers ~~The success of the frame synchronization confirmation is determined~~ when ~~the successive~~ S_R successive frames have been confirmed to be frame synchronized~~ation is confirmed~~. Otherwise, ~~the~~ frame synchronization ~~confirmation~~ failure is ~~determined. Then this synchronization status information is~~ reported to the higher~~upper~~ layers.

c) The UE starts the transmission of the uplink DPCCH/DPDCHs ~~channels~~ at ~~the~~ a frame timing ~~delayed by the slot offset~~exactly T_0 chips after ~~from~~ the frame timing of the received downlink ~~channel~~DPCCH/DPDCH. The DPDCH is transmitted only when there is data to be transmitted~~ to the network~~. The UE immediately starts closed loop power control as described in sections 5.1.2 and 5.2.3, i.e. ~~The~~ the transmission power of the uplink DPCCH/DPDCH~~uplink channels~~ follows the TPC commands ~~transmitted by the network~~generated by UTRAN, and the UE performs SIR estimation ~~.~~to generate TPC commands transmitted to UTRAN.~~by the UE are based on downlink SIR measurements.~~

d) UTRAN~~The network~~ establishes uplink channel chip synchronization and frame synchronization~~. based on the frame offset group and slot offset group~~. Frame synchronization can~~ould~~ be confirmed using the Frame Synchronization Word. Successful frame synchronization is confirmed and reported to the higher layers when S_R successive frames have been confirmed to be frame synchronized. Otherwise, frame synchronization failure is reported to the higher layers.~~The success of the frame synchronization confirmation is determined when the successive S_R frame synchronization is confirmed. Otherwise, the frame synchronization confirmation failure is determined. Then this synchronisation status information is reported to the upper layer. The transmission power of the downlink channels follow the TPC commands transmitted by the UE.~~

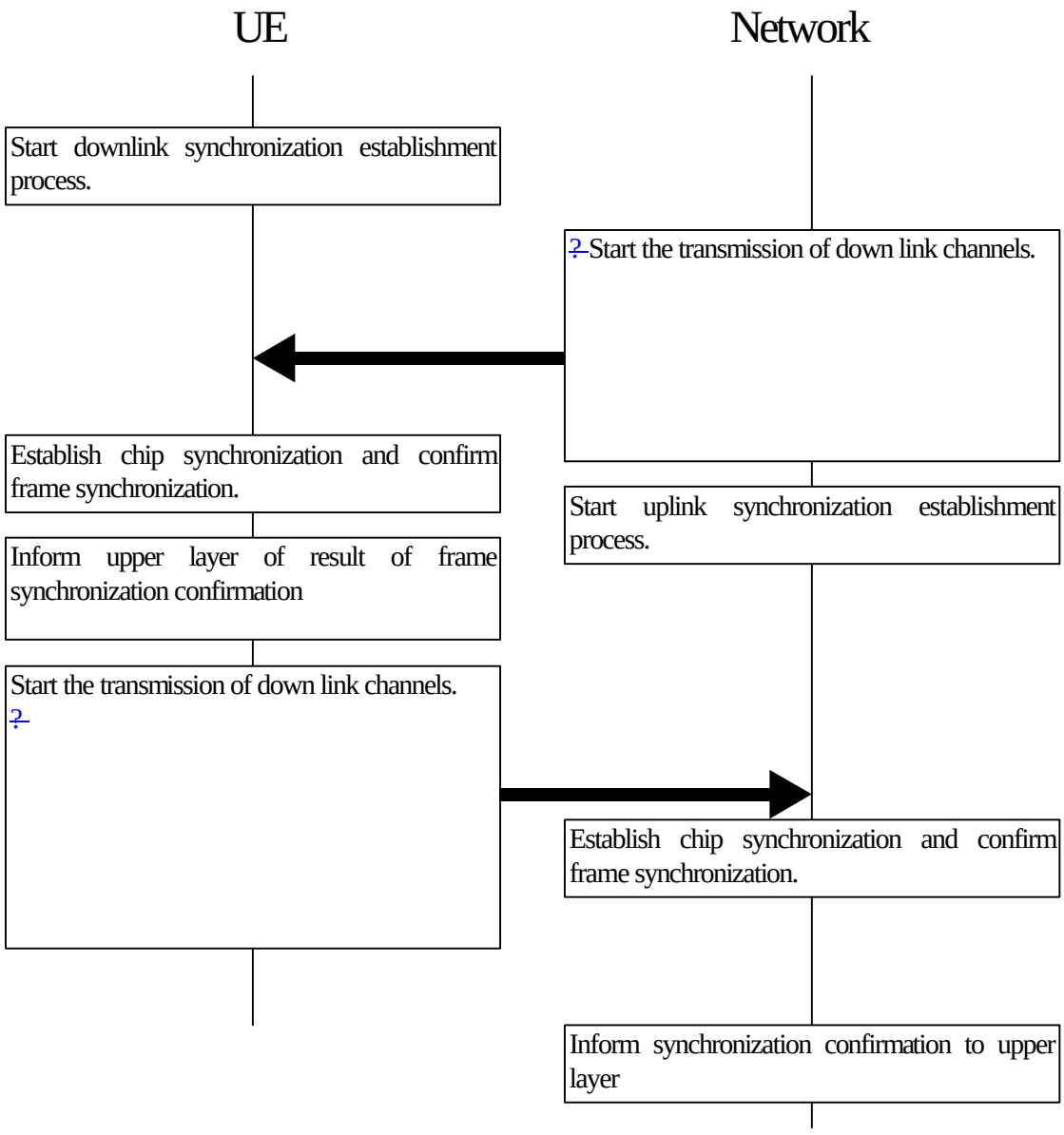

Figure 2: Synchronization eEstablishment fFlow of dDedicated cChannels.

4.5.3 With existing uplink dedicated channel

The assumption for this case is that there already exist DPCCH/DPDCHs in the uplink, and a corresponding dedicated physical channel shall be set up in the downlink. This corresponds to the case when a new cell has been added to the active set in soft handover and shall begin its downlink transmission.

< Editor's note: The actual procedure below is based on the material in Volume 3 section 3.2.6.6.1. Material not relevant for L1 has been removed. The terminology should be updated in accordance with the rest of the specification. The figure should also be updated. This will be done in the next version of this document. The criteria for synchronisation cinfirmation should be considered informative, and should be moved to an informative annex >

At the start of diversity soft handover, the uplink dedicated physical channel transmitted by the UE, and the downlink dedicated physical channel transmitted by the softdiversity handover source node Bcell continues transmitting as usual. will have their radio frame number and scrambling code phase counted up continuously as usual, and they will not change at all.

The synchronisation establishment flow upon intra/inter-cell diversity soft handover is described in Figure 3.

a) The UE starts the chip synchronisation establishment process of downlink channels from the handover destination. The uplink channels being transmitted shall continue transmission as beforewithout any operations performed.

b) ~~The network~~UTRAN starts the transmission of the downlink ~~dedicated physical channels~~DPCCH/DPDCH at a frame timing such that the frame timing received at the UE will be within $T_0 \pm 128$ chips prior to the frame timing of the uplink DPCCH/DPDCH at the UE. UTRAN then~~and~~ starts the synchronization establishment process of the uplink ~~dedicated physical channel~~DPCCH/DPDCH transmitted by the UE. -Frame synchronization ~~could~~ can be confirmed using the Frame Synchronization Word. Successful frame synchronization is confirmed and reported to the higher layers when S_R successive frames have been confirmed to be frame synchronized. Otherwise, frame synchronization failure is reported to the higher layers.~~The success of the frame synchronization confirmation is determined when the successive S_R frame synchronization is confirmed. Otherwise, the frame synchronization confirmation failure is determined. Then this synchronization status information is reported to the upper layer.~~

c) Based on the handover destination ~~Primary CCPCH~~CPICH reception timing, the UE establishes chip synchronisation of downlink channels from handover destination ~~node B~~cell. Frame synchronization ~~could~~ can be confirmed using the Frame Synchronization Word. Successful frame synchronization is confirmed and reported to the higher layers when S_R successive frames have been confirmed to be frame synchronized. Otherwise, frame synchronization failure is reported to the higher layers.~~The success of the frame synchronization confirmation is determined when the successive S_R frame synchronization is confirmed. Otherwise, the frame synchronization confirmation failure is determined. Then this synchronization status information is reported to the upper layer.~~

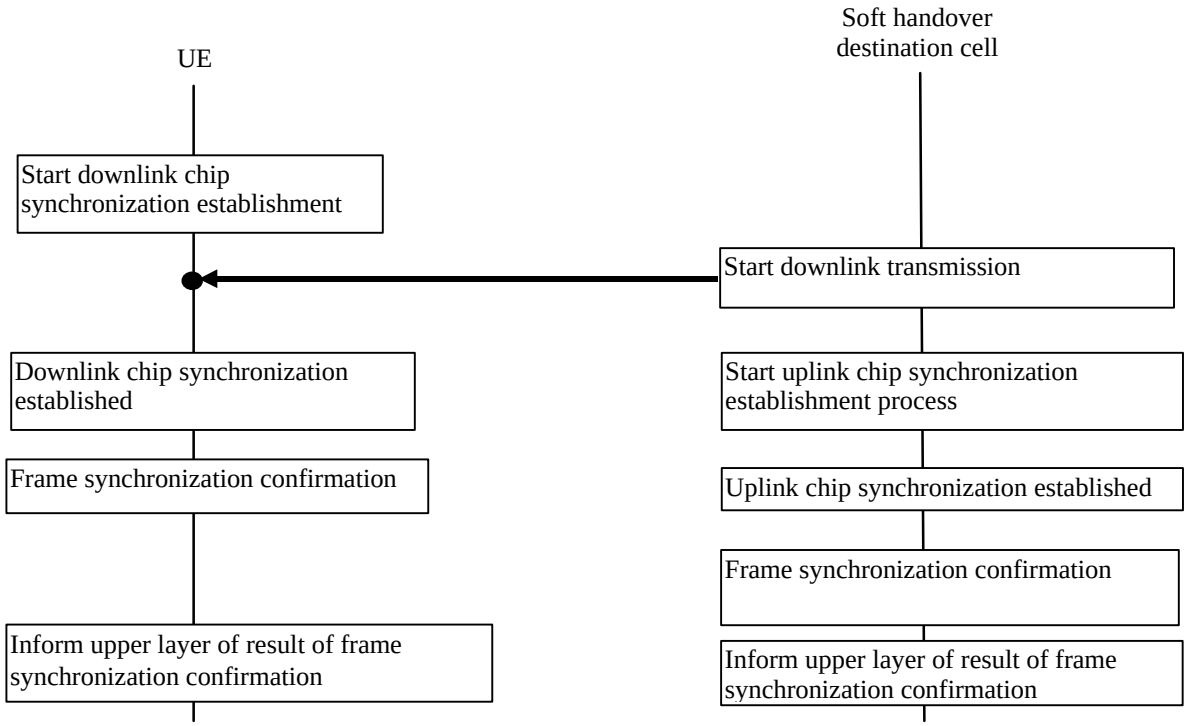

Figure 3: Synchronization ~~e~~Establishment ~~f~~Flow ~~u~~Upon ~~i~~Intra/~~i~~Inter-cell ~~Diversity~~soft ~~H~~handover

During a connection, in some cases the UE is allowed to change its transmission timing. When the UE is in soft handover with cells that all are known to have the same timing reference, the UE may adjust its DPDCH/DPCCH transmission time instant by at most ¼ chip during any 10 ms period. Otherwise, the UE may not adjust its DPDCH/DPCCH transmission time instant.

References

[1] TSG RAN WG1 TS 25.211 V2.1.0 (1999-06), “Physical (FDD)”

[2] TSGR3#5(99)685, “Radio Interface Synchronisation…”, Alcatel