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Hannover, Germany, 30 August – 3 September 1999

Agenda Item: **17**

Source: **Alcatel**

Title: **Radio Interface Synchronisation Issues**

Document for: **Decision**

Introduction

In TSG-RAN **WG3** meeting #5 in Helsinki, some issues related to timing have been addressed in Tdoc R3-99685 to complete/improve the current standard. The following issues have been identified as **WG1** issues (see liaison statement from WG3):

1. Need of a procedure to adjust T_d during connection (for completion of the standard)
2. Definition of a margin ΔT_o (for completion of the standard)

1. Adjustments of T_d During Connection

In order to guarantee a power control delay of one slot in both uplink and downlink and to limit buffering size inside UE, it is required that all DL signals from different SHO branches are received by the UE within a finite time window (size TBD). In other words, the time offset between reception of a DPCH (of any cell in the active set) and transmission of a DPCH at the UE is limited to "$T_o \pm \Delta T_o$", where ΔT_o is some margin TBD (T_o is defined in [2][1]).

At initialisation of a new leg (SHO, "add branch"), this requirement is met by means of the UE
$_m$" and signaling it to the UTRAN.

Note that the procedure to measure T_m would not be needed if the Node Bs were synchronised (phase locked) to each other at an accuracy of some µs, because then the resulting T_d-value would always be 0 (differences of propagation delays are negligible, since they are much less than 256/2 chips=33 µs for realistic cell sizes).
However, in the UTRAN, Node Bs are generally unsynchronised, i.e. neighbouring Node Bs might drift relative to each other at a maximum rate of 2*0.05ppm = 0.1ppm.

Hence, it is evident that for the same reason for which T_m measurements by the UE are needed, also adjustments of T_d <u>during</u> SHO are needed, in case that two legs from different Node Bs remain in the active set for a "longer" period of time (e.g. a minute or so).

But even for the non-SHO case, a procedure to adjust the T_d-value might be useful, see below.

Non-SHO and SHO cases are analysed in more detail in the following:

<u>Non-SHO</u>
According to [1], "*the UE modulated carrier frequency shall be accurate to within ±0.1 PPM compared to carrier frequency received from the BS. These signals will have an apparent error due to BS frequency error and Doppler shift. In the later case, signals from the BS must be averaged over sufficient time that errors due to noise or interference are allowed for within the above ±0.1PPM figure.*"

[1] From [2]: "T_o: This constant timing offset is used to set up the transmission frame timing of an uplink DPCCH/DPDCH in the UE. The value is TBD. The starting phase of the uplink scrambling code is synchronised with the uplink DPCCH/DPDCH frame timing."

In other words, the UE locks its clock to the NodeB's downlink signal only in frequency, but not in time, i.e. only AFC is applied, but time of arrival (TOA) measurements of the received DPCH are not used by the UE for adjusting its local oscillator frequency.
As a result, the UE clock might drift relative to the NodeB clock on the long term (even if the UE does not move). The time difference between reception of a downlink DPCH frame and transmission of a DPCH frame in uplink (which is T_o in the optimum case) will increase or decrease due to this drift. To restrict the difference to T_o ± some margin "ΔT_o", basically three solutions are possible:

a) The NodeB changes the downlink DPCH transmission time, i.e. change of T_d.
b) The UE changes its uplink DPCH transmission time.
c) A third possibility would be to completely avoid a long term drift between UE and NodeB by means of a control loop inside the UE that adjusts the local oscillators frequency as a function of the TOA of the received DPCH. However, such a loop might introduce quite high frequency offsets to the UE oscillators for fast moving UEs, which might conflict with the "±0.1PPM" requirement given in [1]. To avoid this, the frequency source for clocking the UE's time base would have to be different from the frequency source for RF frequency generation.

SHO with different NodeBs
In SHO, the UE cannot lock its clock to all NodeBs at the same time, since the NodeB's oscillators drift relative to each other. As a result, the UE clock drifts relative to at least one NodeB's clock. The time difference between reception of this NodeB's downlink DPCH frame and transmission of a DPCH frame in uplink (which is T_o in the optimum case) will increase or decrease due to this drift. To keep the difference at T_o (±some margin "ΔT_o"), only one solution is possible:

- The NodeB has to change the downlink DPCH transmission time, i.e. change of T_d.

Conclusion
The method to change the T_d values for the downlink DPCH signals is the only solution to cope with clock drifts in SHO. Assuming a frequency drift of the UE of 0.1ppm relative to the NodeB, such an adjustment would occur roughly once every 5 minutes, hence the signaling overhead is negligible.

Proposal
A procedure is proposed that adjusts these T_d offsets upon request by the UE. To avoid the danger of the UE going out-of-sync (possible loss of data, additional layer 1 processing inside the UE), the reconfiguration of T_d shall be "synchronised", i.e. both Node B and UE shall know exactly at what CFN the change of T_d takes effect (compare "synchronised radio link reconfiguration", TS25.433/TS25.423). If T_d crosses a frame boundary due to such an adjustment, the corresponding OFF value (see TS25.401) has to be in- or decreased accordingly.
When such a T_d-adjustment procedure is specified, it is proposed that this procedure is allowed to operate in non-SHO as well (see above, solution "a)"). This keeps the system as simple as possible because no further procedures "b) or "c)" are needed.

It is proposed to send the following **LS statement to WG3:**

> "WG1 requests WG3 to include appropriate signaling means in the WG3 standardisation documents, such that a synchronised reconfiguration of the transmit offset value T_d (+/- 256 chips) is possible. Here, 'synchronised' means that UE shall know the connection frame number (CFN) at which the new T_d value takes effect. A T_d-adjustment shall be triggert by the UE. "

2. Definition of the Margin ΔT_o

From the discussions above it is clear that the TOAs of the earliest received paths of DPCHs from different cells differ due to the granularity of T_d. Some maximum tolerated difference ΔT_o between any earliest received DPCH path and the optimum arrival time "$T_{TX,UL} - T_o$" for an earliest received DPCH path needs to be specified. ΔT_o has to be related to the granularity of T_d and should allow some margin for T_d adjustments.

Proposal

A value of ΔT_o = 256/2 chips + [5]µs = [38.33] µs is proposed, and the requirement would be:
"By means of appropriate T_d adjustments it shall be ensured that the earliest received DPCH path of any cell in the active set always arrives within the time interval [$T_{TX,UL} - T_o - \Delta T_o$; $T_{TX,UL} - T_o + \Delta T_o$] at the UE, where ΔT_o = 128 chips + [5]µs = [38.33] µs and $T_{TX,UL}$ is the time at which the UE transmits an uplink DPCH frame".

If the definition of ΔT_o belongs to a WG3 standardisation document, it is proposed to write the following **LS statement to WG3**:

> "WG1 proposes to introduce a further constant timing parameter, 'ΔT_o' in addition to 'T_o', where 'ΔT_o' is defined as follows:
> 'By means of appropriate T_d adjustments it shall be ensured that the earliest received DPCH path of any cell in the active set always arrives within the time interval [$T_{TX,UL} - T_o - \Delta T_o$; $T_{TX,UL} - T_o + \Delta T_o$] at the UE, where ΔT_o = 128 chips + 5µs = 38.33 µs and $T_{TX,UL}$ is the time at which the UE transmits an uplink DPCH frame.' "

Note: In the worst case, the time difference between the first and the last received path can be as much as 256 chips+2*5µs + $T_{DS,max}$, where $T_{DS,max}$ is the maximum delay spread of the radio channel between UE and a cell. Assuming $T_{DS,max}$ =20µs, this means that the UEs buffer needs to cover a time period of 96.56µs.

References

[1] TS25.101 v1.2.0
[2] TS25.211 v2.1.0
[3] TS25.401 v1.1.1
[4] TS25.423
[5] TS25.433