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Agenda Item :

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Title : Frame Synchronization Words on DPCHs and SCCPCH

Document for : Proposal of Pilot Patterns for Frame Synchronization

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Abstract:

This document proposes a new set of pilot patterns for frame synchronization on uplink DPCCH, downlink DPCCH, and SCPCH. It is shown that the proposed pilot patterns are suitable for frame synchronization since by simply adding autocorrelation functions of such sequences, we can obtain double maximum correlation values equal in magnitude and opposite polarity at zero and middle shifts. This property can be used to double-check frame synchronization timing and reduce the synchronization search time. We show that the performance of frame synchronization word of proposed pilot pattern is much better than that of current pilot pattern.

1. Introduction

In the previous doucument R1-160 [1], a new set of pilot patterns for 3GPP RAN S1.11 v.0.0.1 [2] has been proposed. In this document we propose additional pilot patterns for new frame formats such as Uplink DPCCH with N_{pilot2} = 5 and 7, which were added to S1.11 v1.1.0 [3]. The pilot pattern of [1] for Downlink DPCCH with N_{pilot} = 32 is removed since SF1 and SF2 of Downlink DPCCH were discarded in [3]. Thus, we rearragned and changed the pilot patterns of [1] according to [3].

The new frame synchronization words of the proposed pilot patterns have the lowest out-of-phase values of autocorrelation function with two peak values equal in magnitude and opposite in polarity at zero and middle shifts [4]. It is shown that the proposed frame synchronization words are suitable for frame synchronization confirmation since by simply adding autocorrelation functions of such words, we can obtain double maximum correlation values equal in magnitude and opposite polarity at zero and middle shifts. This property can be used to double-check frame synchronization timing and reduce the synchronization search time.

The UE establishes downlink chip synchronization and frame synchronization based on the Primary CCPCH synchronization timing and the frame offset group, slot offset group notified from the network [5]. The frame

synchronization shall be confirmed using the frame synchronization word [2][3][5]. The network establishes uplink channel chip synchronization and frame synchronization based on the frame offset group and slot offset group [5]. The frame synchronization shall also be confirmed using the frame synchronization word [2][3][5].

When long scarmbling code is used on uplink channels or downlink channels, failure in frame synchronization confirmation using frame synchronization words always means loosing frame and chip synchronizations since the phase of long scrambling code repeats every frame. Whereas in the case of short scrambling code on uplink DPCCH, failure in frame synchronization confirmation does not always implies losing chip synchronization since the lengh of short scrambling code is 256 and it corresponds to one symbol period of uplink DPCCH with SF = 256. Thus the frame synchronization word of pilot pattern can detect synchronization status and this information can be used in RRC Connection Establishment and Relaese Procedures of Layer 2 [6].

The performance of frame synchronization confirmation using current and proposed frame synchronization words of pilot pattern is dissussed over AWGN channel.

2. New Frame Synchronization Words proposal

Table 1 denotes new frame synchronization words and they can be divided into 4 classes according to the autocorrelation function of the synchronization words as follows:

$$E = \{C_1, C_5\}$$

$$F = \{C_2, C_6\}$$

$$G = \{C_3, C_7\}$$

$$H = \{C_4, C_8\}$$

Table 1. New frame synchronization words

Frame Synchronization Words
C_1 = (1 1 0 1 1 1 1 1 0 0 1 0 0 0 0 0)
C_2 = (1 0 0 0 1 0 1 0 0 1 1 1 0 1 0 1)
C_3 = (1 1 0 1 1 1 0 0 0 0 1 0 0 0 1 1)
C_4 = (0 1 1 1 0 1 1 0 1 0 0 0 1 0 0 1)
C_5 = (1 0 1 1 0 0 0 0 0 1 0 0 1 1 1 1)
C_6 = (1 1 1 0 0 1 0 1 0 0 0 1 1 0 1 0)
C_7 = (0 1 0 0 0 0 1 1 1 0 1 1 1 1 0 0)
C_8 = (1 1 1 0 1 0 0 1 0 0 0 1 0 1 1 0)

Table 2. Autocorrelation functions of sequences of the classes E, F, G, and H.

$R(t)$ t	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$R_E(t)$	16	4	0	4	0	-4	0	-4	-16	-4	0	-4	0	4	0	4
$R_F(t)$	16	-4	0	-4	0	4	0	4	-16	4	0	4	0	-4	0	-4
$R_G(t)$	16	4	0	-4	0	4	0	-4	-16	-4	0	4	0	-4	0	4
$R_H(t)$	16	-4	0	4	0	-4	0	4	-16	4	0	-4	0	4	0	-4

Table 2 denotes the autocorrelation functions of sequences of the classes E, F, G, and H. From table 1 and 2, we find that each class contains 2 sequences, and sequences of the same class have the same autocorrelation function. From table 2, we see that the proposed synchronization words have the lowest out-of-phase values of autocorrelation function with two peak values equal in magnitude and opposite in polarity at zero and middle shifts [4]. We also find the following relationships between the autocorrelation functions:

$$R_E(t) = R_F(t) = R_G(t) = R_H(t)\ ,\ t \text{ is even} \tag{1}$$

$$R_E(t) = -R_F(t)\ ,\ t \text{ is odd} \tag{2}$$

$$R_G(t) = -R_H(t)\ ,\ t \text{ is odd} \tag{3}$$

$$R_i(\tau) + R_i(t + 8) = 0\ ,\ i \in \{E,F,G,H\}, \text{ for all } t \tag{4}$$

From (1), (2), and (3), we can easily obtain the following equation.

$$R_E(t) + R_F(t) = R_G(t) + R_H(t)\ , \text{ for all } t \tag{5}$$

The addition of two autocorrelation functions $R_E(t)$ and $R_F(t)$, or $R_G(t)$ and $R_H(t)$ becomes the function with two peak values equal in magnitude and opposite in polarity at zero and middle shifts, and all zero values except the zero and middle shifts, which is depicted in figure 1. The other combinations such as $(R_E(t) + R_G(t))$, $(R_E(t) + R_H(t))$, $(R_F(t) + R_G(t))$, and $(R_F(t) + R_H(t))$ do not have the same value as in Fig. 1. By using the derived properties of the proposed frame synchronization words, we see that

$$\sum_{i=1}^{2a} R_i(t) = a \cdot (R_E(t) + R_F(t)), 1 \le a \le 4 \tag{6}$$

where $R_i(t)$ is the autocorrelation function of sequence C_i , $1 \le i \le 8$.

$(R_E(t) + R_F(t))$, or $(R_G(t) + R_H(t))$

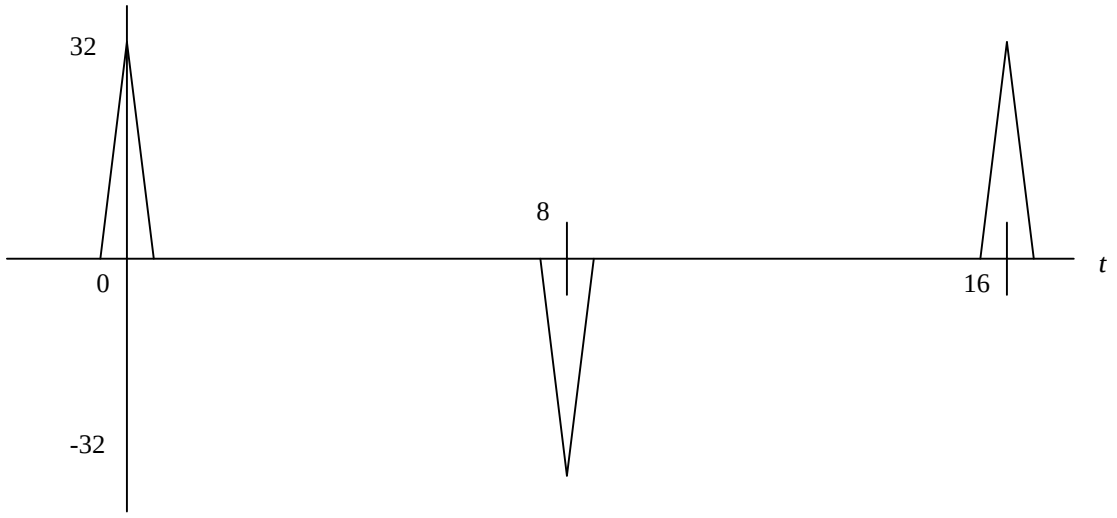


Fig. 1. Addition of two autocorrelation functions $R_E(t)$ and $R_F(t)$, or $R_G(t)$ and $R_H(t)$.

The addition of the four autocorrelation functions becomes figure 2, which is the same as figure 1 except the fact that the maximum value is doubled since $(R_E(t) + R_F(t) + R_G(t) + R_H(t)) = 2\ (R_E(t) + R_F(t))$ by (5) and (6).

$R_E(t) + R_F(t) + R_G(t) + R_H(t)$

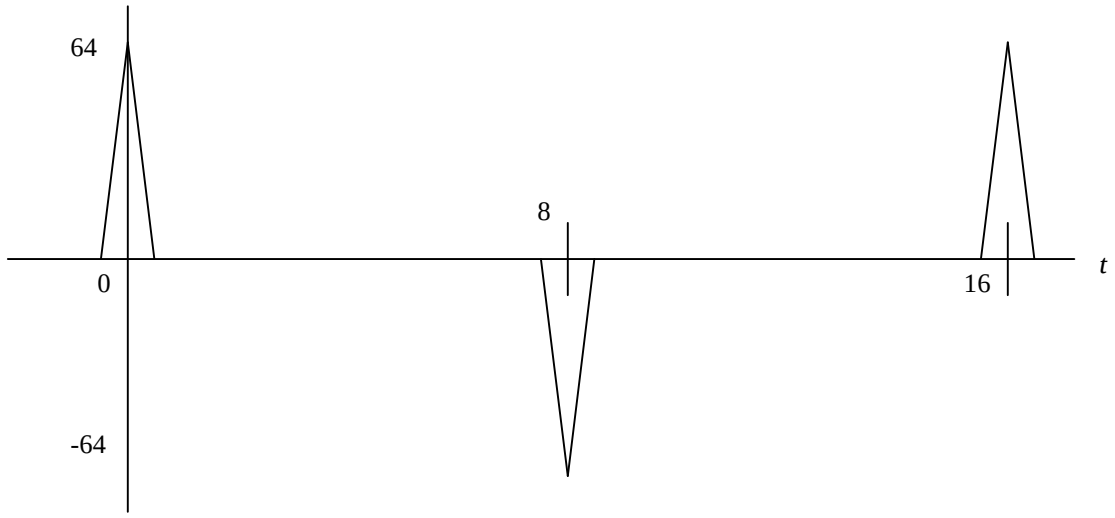


Fig. 2. Addition of four autocorrelation functions $R_E(t)$, $R_F(t)$, $R_G(t)$, and $R_H(t)$.

This property is very important for frame synchronization since it allows us to double-check frame synchronization timing and reduce the synchronization search time.

3. New pilot patterns for uplink DPCCH, downlink DPCCH, and SCCPCH

In this section new pilot patterns for uplink DPCCH, downlink DPCCH, and SCCPCH are proposed.

3.1 Uplink DPCCH

Table 3 and table 4 show the proposed new pilot patterns on uplink DPCCH with N_{pilot2} = 5, 6, 7, and 8. The shadowed parts of the table 3 and 4 can be used for frame synchronization words, and the value of pilot bit other than the frame synchronization words is "1". Table 5 describes the mapping relationship between the 8 words of table 1 and shadowed column pilot bit patterns of table 3 and 4. We know that the sequences C_1, C_2, C_3, and C_4 are the elements of the set E, F, G, and H, respectively.

Table 3. New pilot bit patterns for uplink DPCCH with N_{pilot2} = 5 and 6.

	N_{pilot2} = 5					N_{pilot2} = 6					
Bit #	0	1	2	3	4	0	1	2	3	4	5
Slot #1	1	1	1	1	0	1	1	1	1	1	0
2	1	0	1	1	1	1	1	0	1	1	1
3	0	0	1	0	1	1	0	0	1	0	1
4	1	0	1	1	1	1	1	0	1	1	1
5	1	1	1	1	0	1	1	1	1	1	0
6	1	0	1	1	1	1	1	0	1	1	1
7	1	1	1	0	1	1	1	1	1	0	1
8	1	0	1	0	0	1	1	0	1	0	0
9	0	0	1	0	1	1	0	0	1	0	1
10	0	1	1	0	0	1	0	1	1	0	0
11	1	1	1	1	0	1	1	1	1	1	0
12	0	1	1	0	0	1	0	1	1	0	0
13	0	0	1	0	1	1	0	0	1	0	1
14	0	1	1	0	0	1	0	1	1	0	0
15	0	0	1	1	0	1	0	0	1	1	0
16	0	1	1	1	1	1	0	1	1	1	1

Table 4. New pilot bit patterns for uplink DPCCH with N_{pilot2} = 7 and 8.

	N_{pilot2} = 7							N_{pilot2} = 8							
Bit #	0	1	2	3	4	5	6	0	1	2	3	4	5	6	7
Slot #1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
2	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
3	1	0	0	1	0	1	1	1	0	1	0	1	0	1	1
4	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
5	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
6	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
7	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1
8	1	1	0	1	0	0	1	1	1	1	0	1	0	1	0
9	1	0	0	1	0	1	1	1	0	1	0	1	0	1	1
10	1	0	1	1	0	0	1	1	0	1	1	1	0	1	0
11	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
12	1	0	1	1	0	0	1	1	0	1	1	1	0	1	0
13	1	0	0	1	0	1	1	1	0	1	0	1	0	1	1
14	1	0	1	1	0	0	1	1	0	1	1	1	0	1	0
15	1	0	0	1	1	0	1	1	0	1	0	1	1	1	0
16	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1

Table 5. Mapping relationship between the words of table 1 and shadowed column pilot bit patterns of table 3 and 4 on uplink DPCCH

N_{pilot2}	Pilot bit position #	Corresponding column sequence of length 16
5	0	C_1
	1	C_2
	3	C_3
	4	C_4
6	1	C_1
	2	C_2
	4	C_3
	5	C_4
7	1	C_1
	2	C_2
	4	C_3
	5	C_4
8	1	C_1
	3	C_2
	5	C_3
	7	C_4

We obtain Fig. 1 and Fig. 2 by letting α = 1 and 2 of (6), respectively. This enables us to double-check frame synchronization timing and reduce the synchronization time on uplink DPCCH with N_{pilot2} = 5, 6, 7, and 8.

3.2 Downlink DPCCH

Table 6 shows the proposed new pilot symbol patterns on uplink DPCCH with 8, 16, 32, 64, 128, 256, 512, and 1024ksps. The shadowed parts of the table can be used for frame synchronization words, and the value of pilot symbol other than the frame synchronization word is “1”. Table 7 describes the mapping relationship between the 8 words of table 1 and shadowed column pilot symbol patterns of table 6. Similarly, by using the autocorrelation property of proposed pilot symbol patterns and equation (6), we can double-check frame synchronization timing and reduce the frame synchronization search time.

For example, we obtain Fig. 1 by letting Fo= 1 of (6) for downlink DPCCH with 8ksps and Fig. 2 = (2×Fig. 1) by letting Fi= 2 for 16, 32, 64, 128ksps. Similarily, we can also obtain 4×Fig. 1 by setting Fi= 4 of (6) for 256, 512, 1024ksps.

Table 6. New pilot symbol patterns for downlink DPCCH with 8, 16, 32, 64, 128, 256, 512, and 1024ksps

Symbol rate	8ksps		16,32,64,128ksps				256,512,1024ksps							
Symbol #	0	1	0	1	2	3	0	1	2	3	4	5	6	7
Slot # 1	11	11	11	11	11	10	11	11	11	10	11	11	11	01
2	11	10	11	10	11	11	11	10	11	11	11	01	11	11
3	11	00	11	00	11	01	11	00	11	01	11	11	11	01
4	11	10	11	10	11	11	11	10	11	11	11	10	11	00
5	11	11	11	11	11	10	11	11	11	10	11	00	11	01
6	11	10	11	10	11	11	11	10	11	11	11	01	11	00
7	11	11	11	11	11	01	11	11	11	01	11	00	11	10
8	11	10	11	10	11	00	11	10	11	00	11	01	11	11
9	11	00	11	00	11	01	11	00	11	01	11	00	11	10
10	11	01	11	01	11	00	11	01	11	00	11	10	11	00
11	11	11	11	11	11	10	11	11	11	10	11	00	11	10
12	11	01	11	01	11	00	11	01	11	00	11	01	11	11
13	11	00	11	00	11	01	11	00	11	01	11	11	11	10
14	11	01	11	01	11	00	11	01	11	00	11	10	11	11
15	11	00	11	00	11	10	11	00	11	10	11	11	11	01
16	11	01	11	01	11	11	11	01	11	11	11	10	11	00

Table 7. Mapping relationship between the words of table 1 and shadowed column pilot symbol patterns of table 6 on downlink DPCCH with 8, 16, 32, 64, 128, 256, 512, and 1024ksps

Symbol rate	Symbol #	Channel	Corresponding column sequence of length 16
8ksps	1	I-CH	C_1
		Q-CH	C_2
16, 32, 64, 128ksps	1	I-CH	C_1
		Q-CH	C_2
	3	I-CH	C_3
		Q-CH	C_4

256, 512, 1024ksps	1	I-CH	C_1
		Q-CH	C_2
	3	I-CH	C_3
		Q-CH	C_4
	5	I-CH	C_5
		Q-CH	C_6
	7	I-CH	C_7
		Q-CH	C_8

3.3 SCCPCH

Table 8 shows the proposed new pilot patterns on Secondary CCPCH. The shadowed parts of the table can be used for frame synchronization words, and the value of pilot symbol other than the frame synchronization word is "1". Table 9 shows the mapping relationship between the words of table 1 and shadowed column pilot symbol patterns of table 8. Similarly, we can double-check frame synchronization timing and reduce the synchronization search time of Secondary CCPCH by letting α = 1 or 2 of (6).

Table 8. New pilot symbol patterns for Secondary CCPCH

Symbol #	0	1	2	3

Slot #1	11	11	11	10
2	11	10	11	11
3	11	00	11	01
4	11	10	11	11
5	11	11	11	10
6	11	10	11	11
7	11	11	11	01
8	11	10	11	00
9	11	00	11	01
10	11	01	11	00
11	11	11	11	10
12	11	01	11	00
13	11	00	11	01
14	11	01	11	00
15	11	00	11	10
16	11	01	11	11

Table 9. Mapping relationship between the words of table 1
and shadowed column pilot patterns of table 8 on SCCPCH.

Symbol #	Channel	Corresponding column Sequence of length 16
1	I-CH	C_1
	Q-CH	C_2
3	I-CH	C_3
	Q-CH	C_4

4. Property of autocorrelation function

As has been described in the previous section, the pilot pattern consists of all “1” words and shodowed frame synchronization words. The shodowed words of the pilot pattern are used for frame synchronization confirmation and thus summation of autocorrelated values for each column shadowed frame sychronization words is required. Hence the property of summation of autocorrelated values of frame synchronization words is very important. The addition of autocorrelation functions of frame synchronization word for DPCCHs and SCCPCH are depicted in Fig. 10, 11, and 12.

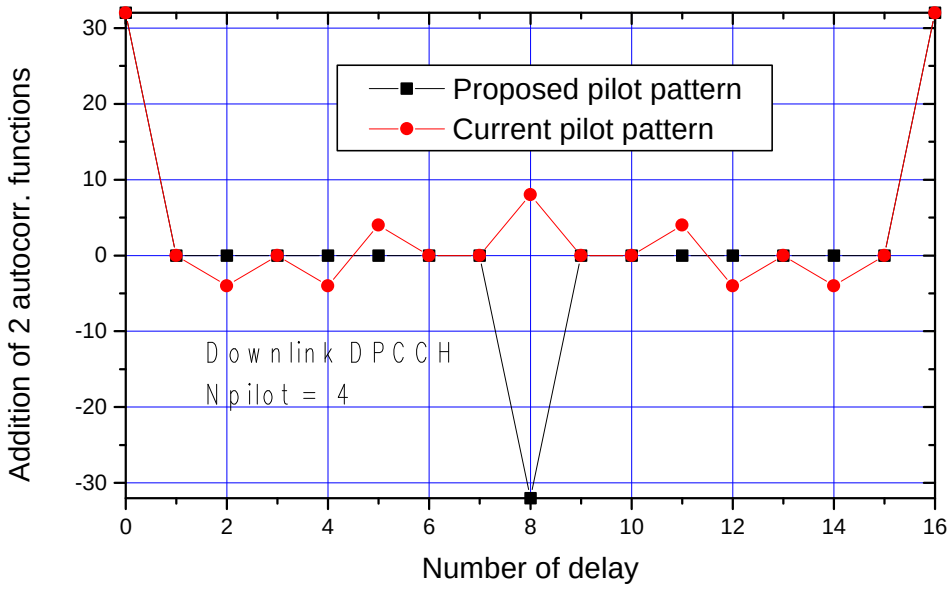


Fig. 10. The addition of 2 autocorrelation functions on downlink DPCCH with $N_{pilot} = 4$.

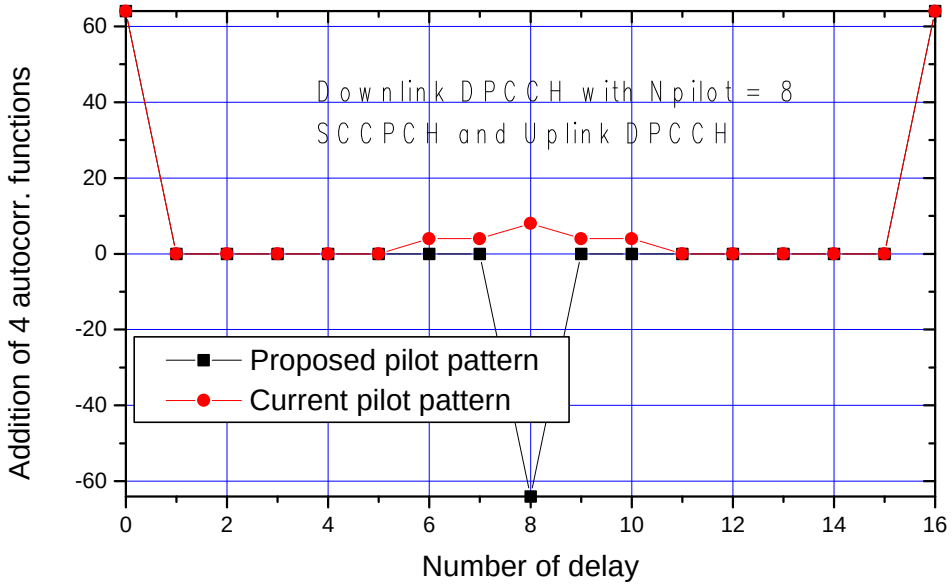


Fig. 11. The addition of 4 autocorrelation functions on downlink DPCCH with N_{pilot} = 8, uplink DPCCH, and SCCPCH.

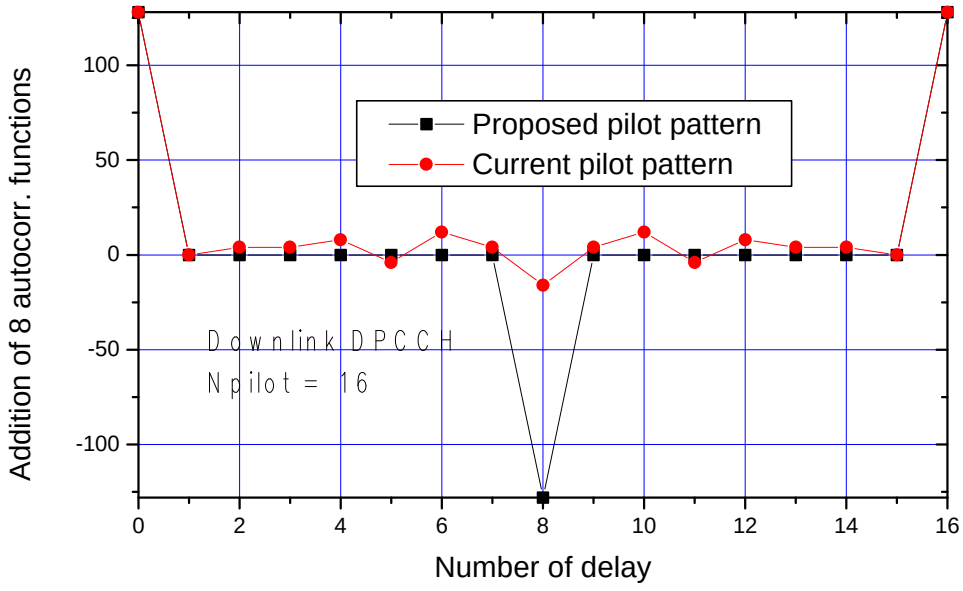


Fig. 12. The addition of 8 autocorrelation functions on downlink DPCCH with N_{pilot} = 16.

From Fig. 10, 11, and 12, we can easily find that current frame synchronization word has the non-zero out-of-phase autocorrelation function with peak value at zero shift. Wherease the proposed frame synchronization word has the zero out-of-phase autocorrelation function with two peak values equal in magnitude and opposite in polarity at zero and middle shifts.

5. Simulation performance

Correlation to the known frame synchronization word is optimum method for frame synchronization. Since the frame synchronization word of pilot pattern is used for frame synchronization confirmation [2][3][5], we first define the following events and parameters to be used to evaluate the performance of frame synchronization confirmation using the proposed and current frame synchronization words:

H_1 : The event that the correlator output exceeds the predetermined threshold when the code phase offset between the received shadowed column frame synchronization word and its corresponding receiver stored frame synchronization word is zero.

H_2 : The event that the correlator output exceeds the predetermined threshold when the code phase offset between the received shadowed column frame synchronization word and its corresponding receiver stored frame synchronization word is not zero.

H_3 : One event of H_1 and no event of H_2 for one frame

H_4 : The event that the correlator output exceeds the predetermined threshold or is smaller than –1×(predetermined threshold) when the code phase offset between the received shadowed column frame synchronization word and its corresponding receiver stored frame synchronization word is 0 or 8, respectively.

H_5 : The event that the correlator output exceeds the predetermined threshold or is smaller than –1×(predetermined threshold) when the code phase offset between the received shadowed column frame synchronization word and its corresponding receiver stored frame synchronization word is not 0 and 8.

H_6 : One event of H_4 and no event of H_5 for one frame

P_D : Probability of a detection

P_{FA} : Probability of a false alarm

P_S : Probability of a frame synchronization confirmation success for one frame

From the above definitions, when the conventional pilot pattern is used for frame synchronization confirmation, the probability of a detection and a false alarm can be expressed as:

$$P_D = \text{Prob}(H_1) \tag{7}$$

$$P_{FA} = \text{Prob}(H_2) \quad (8)$$

The probability of a frame synchronization confirmation success for one frame becomes $P_S = \text{Prob}(H_3)$ and it can be expressed as

$$P_S = P_D(1-P_{FA})^{15} \quad (9)$$

Whereas in the case of proposed pilot pattern, as has been stated in the previous sections, we know that double thresholds are needed for double-check frame synchronization, and thus the probability of a detection and a false alarm can be expressed as:

$$P_D = \text{Prob}(H_4) \quad (10)$$

$$P_{FA} = \text{Prob}(H_5) \quad (11)$$

Similarly, in the case of proposed pilot pattern, the probability of a frame confirmation success for one frame becomes $P_S = \text{Prob}(H_6)$ and it is given by

$$P_S = P_D(1-P_{FA})^{14} \quad (12)$$

Form (9) and (12), the probability of a frame synchronization confirmation is greately affected by the probability of a false alarm since P_S is propotional to P_D and $(1-P_{FA})^{14}$ or $(1-P_{FA})^{15}$. For example, assume that $P_{FA} = 10^{-1}$, then $(1-P_{FA})^{14} = 0.2288$ and $(1-P_{FA})^{15} = 0.2059$. Now let $P_{FA} = 10^{-3}$, then $(1-P_{FA})^{14} = 0.9861$ and $(1-P_{FA})^{15} = 0.9851$. We can sufficiently evaluate the performance of frame synchronization by selecting the threshold so that the P_{FA} is much smaller than $(1-P_D)$.

The following parameters are used for obtaining P_D, P_{FA}, and P_S on uplink DPCH and downlink DPCH over AWGN. The P_D, P_{FA}, and P_S are given as a function of E_b/N_0 ratio (E_b = energy per bit, N_0 = noise power spectral density).

Table 10. Parameters for simulation performance evaluation over AWGN channel

Parameters	Downlink
Slot per frame	16
Number of bits in the DPCCH (Pilot/TPC/TFCI)	4/2/0
Number of bits in the DPDCH per each slot	4
Spreding factor (DPDCH)	512
Spreding factor (DPCCH)	512
Modulation	QPSK
3dB bandwidth	4.096MHz
Shaping filter	Root raised cosine (roll off 0.22)
Power amplifier	Ideal
Propogation channel	AWGN

5.1 Downlink

The following figures show P_D, P_{FA}, and P_S as a function of E_b/N_0 on downlink DPCH with N_{pilot} = 4 over AWGN channel.

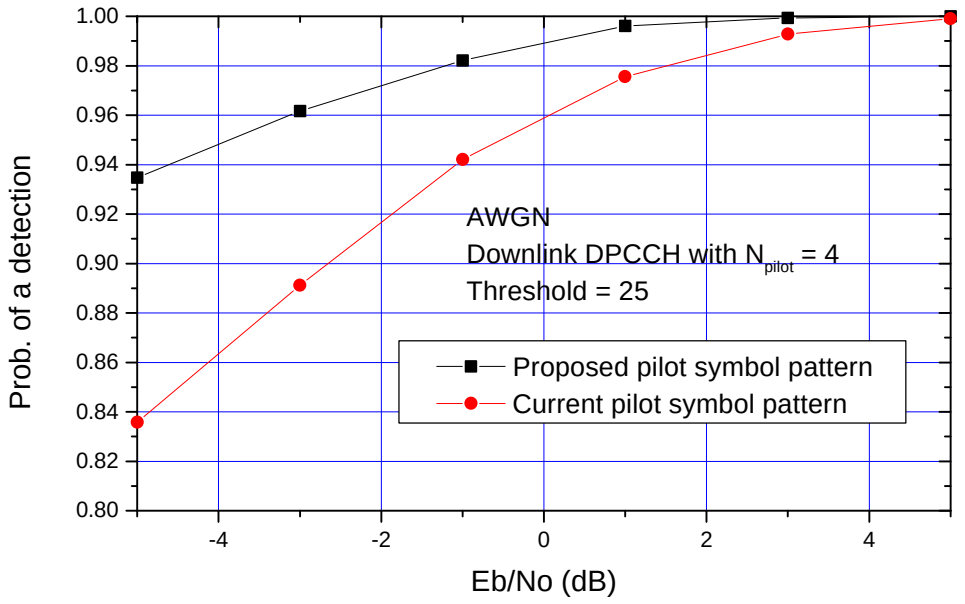


Fig. 13. Probability of a detection on downlink DPCCH with N_{pilot} = 4 over AWGN channel.

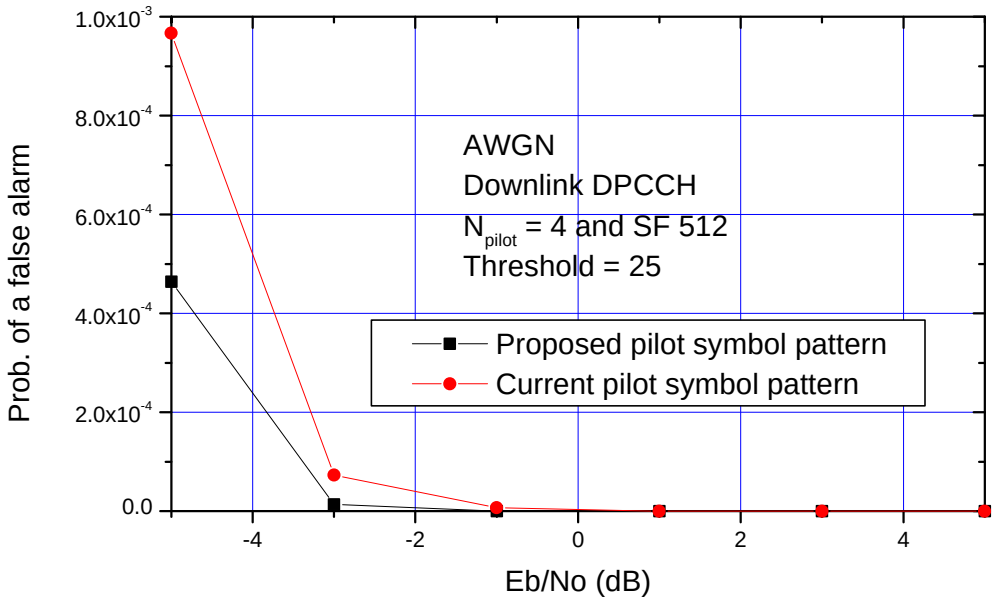
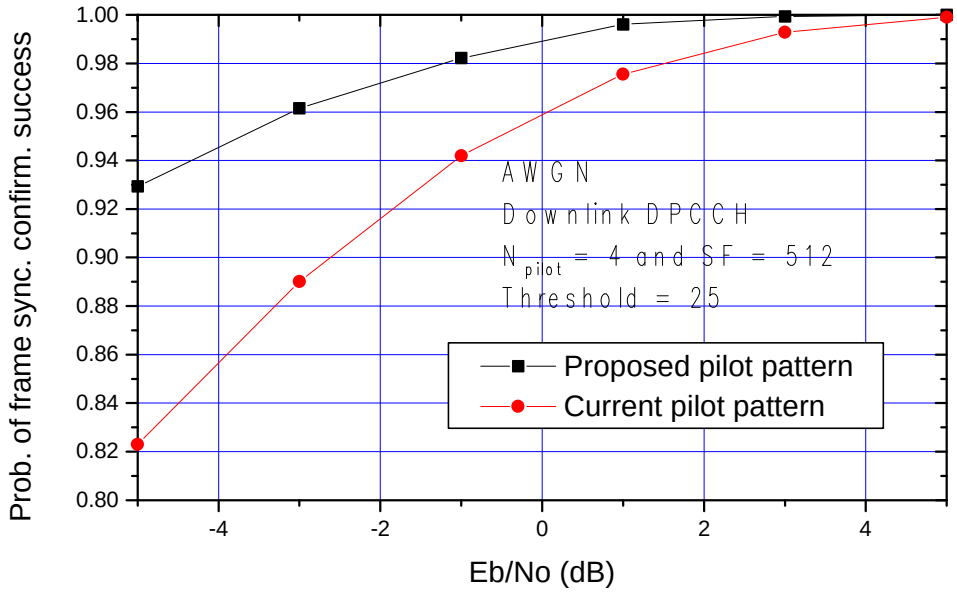


Fig. 14. Probability of a false alarm on downlink DPCCH with N_{pilot} = 4 over AWGN channel.

Fig. 15. Probability of a frame synchronization confirmation success on downlink DPCCH with N_{pilot} = 4 over AWGN channel.



The P_D and P_S of proposed pilot patterns are greater than that of current pilot pattern. Furthermore, the P_{FA} of

proposed pilot pattern is also smaller than that of current pilot pattern. We also see that the theoretical equation (9) and (12) are exactly identical to simulation result of Fig. 15. Therefore, we can easily find that there is significiant difference bewteen the frame synchronization performance of proposed pilot pattern and that of current pilot pattern. For example, from Fig. 15 we see there is 3dB gain at $P_S = 0.93$ by employing proposed new pilot pattern.

6. Conclusion

In this document we proposed a new set of pilot pattern for frame synchronization on uplink DPCCH, downlink DPCCH, and SCCPCH. We showed that the proposed synchronization words are especially suitable for frame synchronization confirmation on those channels since, by adding the autocorrelation functions of shadowed column frame synchronization words, we can obtain double maximum values equal in magnitude and opposite polarity at zero and middle shifts. This property can be used to double-check frame synchronization timing and reduce the synchronization search time. The performance of frame synchronization confirmation over AWGN using pilot pattern was described, and we found that there is significant difference between the frame synchronization performance of the new pilot pattern and that of current pilot pattern.

7. Reference

[1] "Pilot Pattterns for Frame Synchronization", *3GPP TSGR1#3(99)160*.

[2] "UTRA FDD; Transport channels and physical channels (FDD)", *3GPP RAN S1.11 v0.0.1 (1999-02), TSGR1#2 (99)049*.

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