TSG-RAN Working Group1 meeting #2
Yokohama 22-25, February 1999

TSGR1#2(99)0xx

Agenda Item:

Source: Lucent Technologies

Title: A quantitative measure of the VLSI implementation complexity versus block size for 4-state SCCC and 8-state PCCC

Document for: Discussion

Introduction

In [1] and [2] we presented a detailed analysis of the VLSI implementation complexity based on arithmetic and memory requirements for parallel and serial concatenation.

In this document, based on the architectural assumption made in [1] and [2] (one single SISO decoder and one single memory buffer for internal Log-Likelihood ratios), we present tables and graphs showing the partial and overall complexity, measured in terms of required ASIC area for 0.5 μm technology, versus the information block size.

Complexity comparison

In the following three tables two tables we show the partial and overall complexity of 8-state PCCC and 4-state SCCC , expressed in ASIC area (square mm) for the three information block sizes of 320, 640 and 5120. We also the percentage increasing in the overall complexity of PCCC versus SCCC. In deriving the numbers based on the architectural solution we assumed an eight bit quantization of the soft demodulator samples entering the decoder.

Table 1: ASIC complexity in square mm for 8-state PCCC with 8 bit quantization

Information block size	***PCCC***				
	Memory	*SISO with ripple carry*	*SISO with carry look ahead*	***Total with ripple carry***	***Total with carry look ahead***
320	1.87	9.84	12.51	**11.71**	**14.38**
640	3.52	9.84	12.51	**13.36**	**16.03**
5120	24.9	9.84	12.51	**34.74**	**37.41**

Table 2: ASIC complexity in square mm for 4-state SCCC with 8 bit quantization

Information block size	***SCCC***				
	Memory	*SISO with ripple carry*	*SISO with carry look ahead*	***Total with ripple carry***	***Total with carry look ahead***
320	2.07	4.98	6.29	**7.05**	**8.36**
640	3.86	4.98	6.29	**8.84**	**10.15**
5120	27.2	4.98	6.29	**32.18**	**33.49**

Table 3:

Information block size	***Percentage increase of PCCC over SCCC (carry look ahead – 8 bits)***
320	**72%**
640	**58%**
5120	**12%**

In the next three tables we show the analogous results as the previous ones for the case of five bit quantized soft demodulator outputs.

Table 4: ASIC complexity in square mm for 8-state PCCC with 5 bit quantization

Information block size	***PCCC***				
	Memory	*SISO with ripple carry*	*SISO with carry look ahead*	***Total with ripple carry***	***Total with carry look ahead***
320	1.27	9.84	12.51	**11.11**	**13.78**
640	2.36	9.84	12.51	**12.2**	**14.87**
5120	15.51	9.84	12.51	**25.35**	**28.02**

Table 5: ASIC complexity in square mm for 4-state SCCC with 5 bit quantization

Information block size	***SCCC***				
	Memory	*SISO with ripple carry*	*SISO with carry look ahead*	***Total with ripple carry***	***Total with carry look ahead***
320	1.41	4.98	6.29	**6.39**	**7.7**
640	2.6	4.98	6.29	**7.58**	**8.89**

5120		4.98	6.29		**24.19**

Table :

Information block size	***PCCC over SCCC (carry look ahead – 5 bits)***
	79%
640	
5120	**16%**

the cases of 320 and 640 block sizes, and a non negligible reduction for the case N=5120.

To give a visual evidence to the relative weight of memory and arithmetic complexity for the two decoders we

cases we see that the curves of PCCC and SCCC increases with the block size with a different slope, larger for SCCC because of the larger memory requirements.

complexity) occurs at block sizes larger than 10000. In particular, figures 1 and 2 refer to the case of 8-bit quantization and ripple carry and carry look ahead respectively. Figures 3 to 4 refer to the case of 5-bit

for block sizes up to 2 000. On the right hand side of Figures 4 and 5 we also reported the percentage increase of PCCC over SCCC.

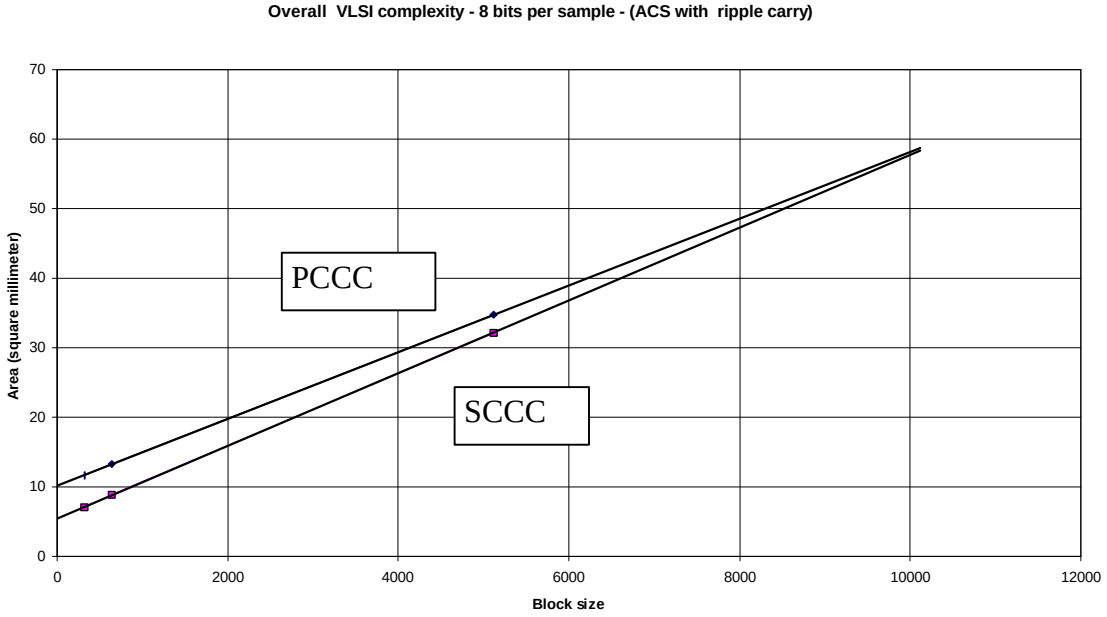

Figure 1: Overall implementation complexity in terms of ASIC area (square mm) versus information block size (ripple carry, 8-bit quantization) .

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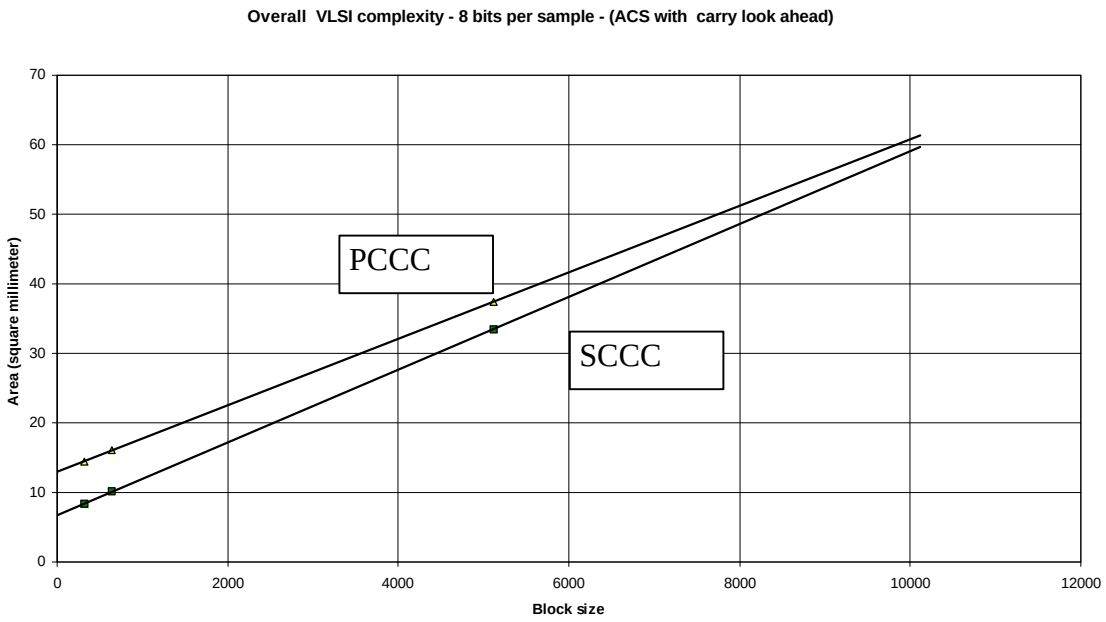

Figure 2: Overall implementation complexity in terms of ASIC area (square mm) versus information block size (carry look ahead, 8-bit quantization) .

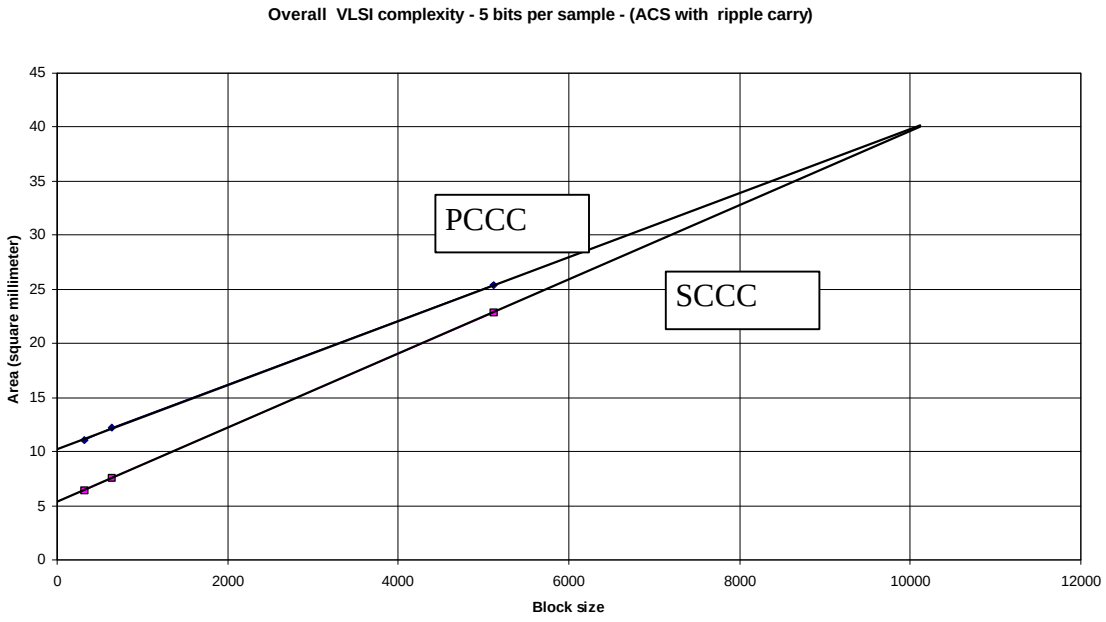

Figure 3 Overall implementation complexity in terms of ASIC area (square mm) versus information block size (ripple carry, 5-bit quantization) .

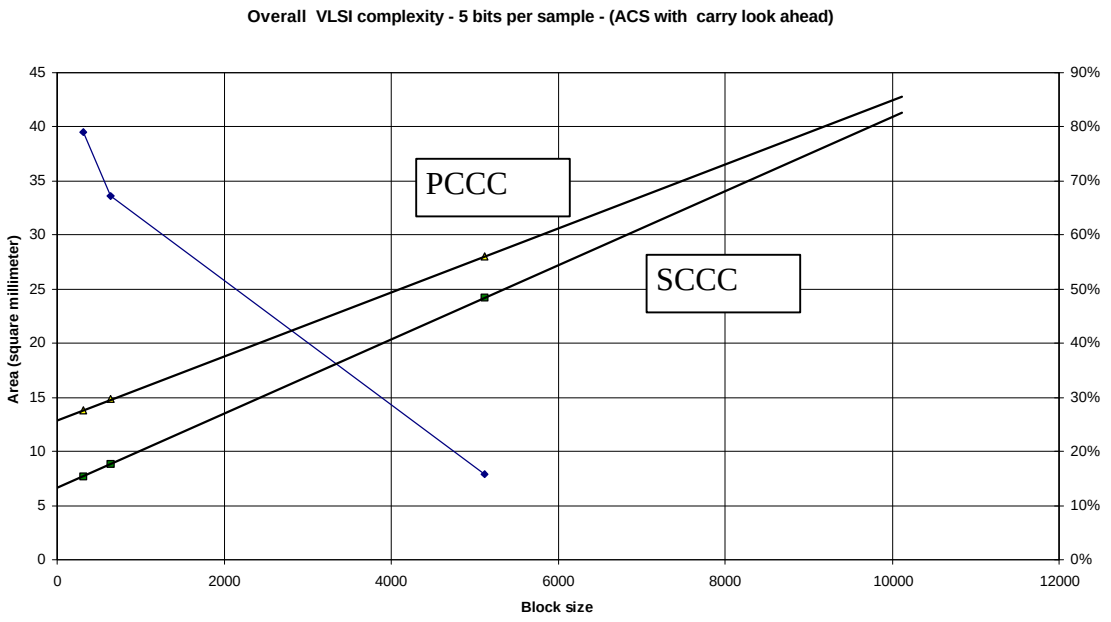

Figure 4: Overall implementation complexity in terms of ASIC area (square mm) versus information block size (carry look ahead, 5-bit quantization).

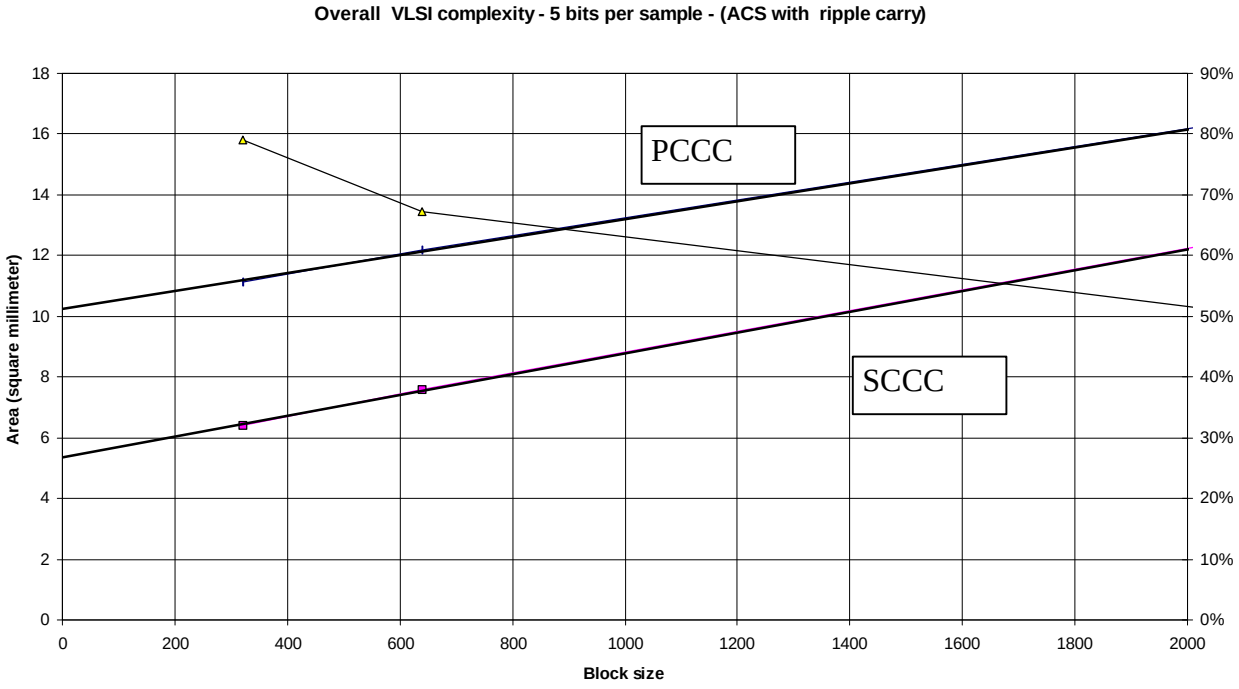

Figure 5: Overall implementation complexity in terms of ASIC area (square mm) versus information block size (carry look ahead, 5-bit quantization). Magnification of Figure 4 up to a block size of 2000.

Conclusions

Based on the detailed analysis performed in [1] and [2] on the the VLSI implementation complexity based on arithmetic and memory requirements for parallel and serial concatenation, we presented tables and graphs showing the partial and overall complexity, measured in terms of required ASIC area for 0.5 μm technology, versus the information block size.

The results show that the solution based on 4-state SCCC yields a large reduction of implementation complexity for the cases of 320 (72-79%) and 640 (58-67%) block sizes, and a non negligible reduction for the case N=5120 (12-16%).

References

[1] Lucent Tdoc SMG2 UMTS-L1 2x99-033.

[2] Lucent TSGR1#2(99)038