TSG-RAN Working Group1 meeting #2
Yokohama 22-25, February 1999

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Agenda Item: **4**

Source: **NTT DoCoMo**

Title: **Fixed block-Shape Multi-stage Interleaver (FS-MIL) for Channel Interleaver**

Document for:

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1. Introduction

Reference [1] described that concept of Multi-stage Interleaver (MIL) can apply not only to turbo internal interleaving but also channel interleaving. This document proposes Fixed-shape MIL (FS-MIL) for channel interleaving, and describes overview of FS-MIL.

FS-MIL generates interleaving pattern using multiple block interleavers similar with turbo internal MIL. But FS-MIL does not include shape modification, which is included in Turbo internal MIL. Complexity of FS-MIL is much smaller than that of Turbo internal MIL.

Reference [2] contains a discussion on how the 2-step channel interleaving, inter-frame and intra-frame interleaving, can be implemented. This document shows that FS-MIL can be applied the 2-step interleaving.

Finally, simulation results of required Eb/Io for FS-MIL and comparison with that for normal block interleaver are shown in this document.

2. Overview of FS-MIL

FS-MIL generates interleaving pattern using multiple block interleavers similar with turbo internal MIL. But FS-MIL does not include block-shape modification, which is included in Turbo internal MIL. Complexity of FS-MIL is much smaller than that of Turbo decoder.

3. 2-step FS-MIL processing

Reference [2] contains a discussion on how the 2-step channel interleaving, inter-frame and intra-frame interleaving, can be implemented.

Fig. 1 shows an example of FS-MIL processing for 64 bits sequence.

The 64 bits sequence is applied the first stage block interleaving at first. MIL processing mainly consist of 2 steps; row by row processing and column by column processing. Due to the row by row processing, bit sequence in each row of the 1^{st} stage block interleaver are randomized. Due to fixed shape processing, bit sequence after the row by row processing is corresponding to block interleaver randomizing the columns. Next, column by column processing is applied. Bit sequence in each column is randomized. The randomizing pattern of each column is same as that of the other column.

If the number of column of the first stage block interleaver is set to the number of interleaving size (frames), 1^{st} step processing becomes inter-frame interleaving (row by row processing in MIL). Furthermore, 2^{nd} step processing becomes intra-frame interleaving (column by column processing in MIL). We only have to specify an inter-frame interleaving pattern for each interleaving size (frames) and specify an intra-frame interleaving pattern for each physical channel (symbol rate).

We have already confirmed that relationship between the number of rows and columns of the first stage block interleaver is not related to MIL transmission characteristics. Therefore, there is no problem to set the number of column of the first stage block interleaver to the number of interleaving size (frames).

Annex shows draft description of FS-MIL interleaving pattern. As you can see, we only have to specify inter-frame interleaving patterns corresponding to interleaving size (frames) and intra-frame interleaving patterns corresponding to physical channel symbol rate.

4. Simulation results

Table 1 shows simulation results of required Eb/Io of FS-MIL and normal block interleaver.
Simulation parameters are followings;

- Vehicular-B delay profile
- 2 antenna space diversity, 2 finger RAKE per antenna.
- 128 ksps DPCH, 64kbps data transmission
- 80 msec interleaving size
- Turbo internal interleaver:MIL
- Turbo code K=3 with 8th iteration Soft-in/Soft-out Viterbi decoding (SOVA)

As the table shows, FS-MIL has better performance than normal block interleaving.

Table 1 Simulation results of required Eb/Io of FS-MIL and normal block interleaver

	with TPC, f_D=80 Hz		w/o TPC, f_D=5 Hz	
	BER=10^{-3}	FER=10^{-2}	BER=10^{-3}	FER=10^{-2}
Normal block interleaver	1.6 dB	2.0 dB	5.5 dB	6.1 dB
FS-MIL	1.4 dB	1.8 dB	5.3 dB	5.2 dB

5. Conclusion

This document proposed FS-MIL for channel interleaving. It is shown that FS-MIL can apply to 2-step interleaving and that interleaving pattern of FS-MIL can be described for each interleaving size and each physical channel symbol rate. Furthermore, it is shown that FS-MIL has better performance than normal block interleaver from required Eb/Io point of view.

Reference

[1] NTT DoCoMo, “Multi-stage interleaving (MIL) method for Turbo codes”, Tdoc SMG2 UMTS-L1 273/98
[2] Ericsson, “Transport channel multiplexing – comments on interleaving”, Tdoc SMG2 UMTS-L1 706/98

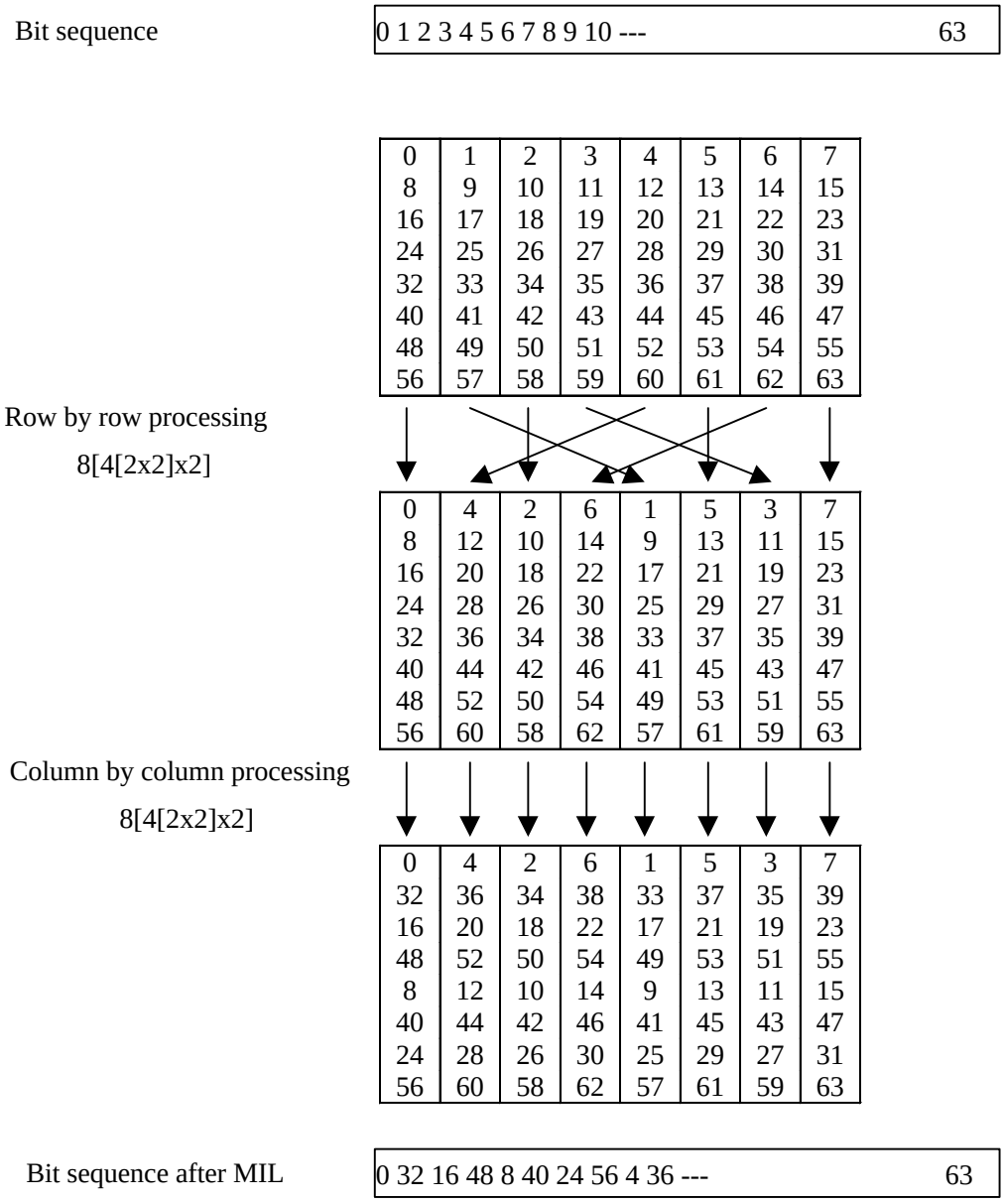


Fig. 1 An example of FS-MIL processing for 64 bits sequence.

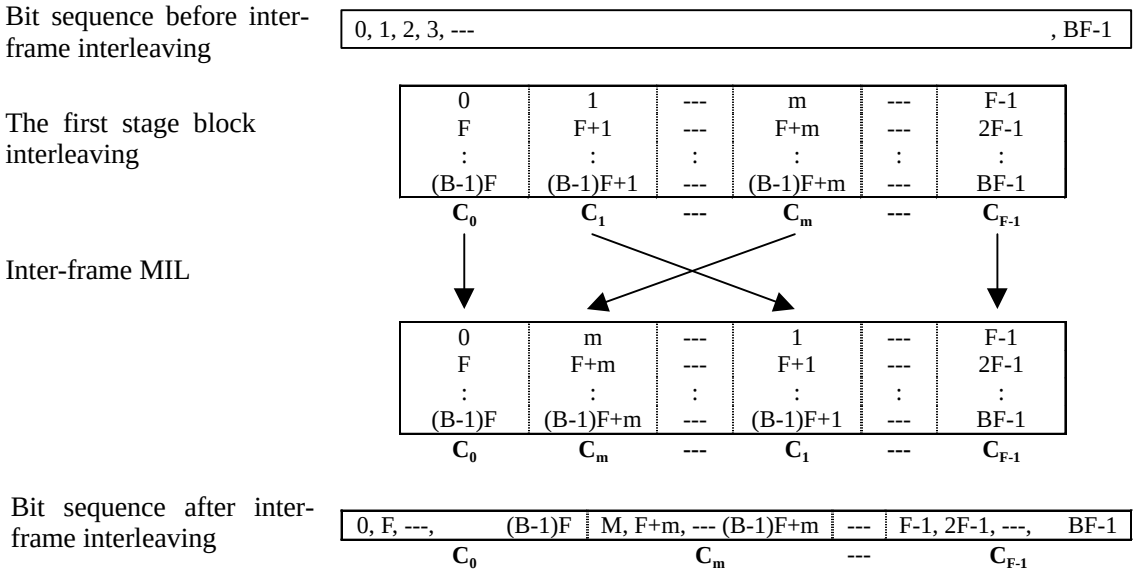
Annex

1. Channel Interleaving

The channel interleaver has the interleaving pattern obtained by using Fixed-shape Multi-stage Interleaving Method (FS-MIL). FS- MIL consists of two-step interleaving process; inter-frame FS-MIL and intra-frame FS-MIL. In the transmitter side, the inter-frame FS-MIL is processed in advance of the intra frame FS-MIL.

1.1. Inter-frame FS-MIL

Inter-frame FS-MIL pattern corresponds to interleaving size [frames]. Overview of the inter-frame FS-MIL is shown in Fig. 1-1. Table 1-1 shows the inter-frame FS-MIL pattern for each interleaving size [frames].



F: the number of radio frames corresponding to interleaving size
B: the number of bits in a radio frame for a inter-frame interleaving unit

Fig. 1-1 Overview of the inter-frame MIL

Table 1-1 the inter-frame FS-MIL pattern for each interleaving size [frames]

Interleaving size [frames]	Interleaving pattern of the inter-frame FS-MIL
1	$\mathbf{C_0}$
2	$\mathbf{C_0, C_1}$
4	$\mathbf{C_0, C_2, C_1, C_3}$
8	$\mathbf{C_0, C_4, C_2, C_6, C_1, C_5, C_3, C_7}$

1.2. Intra-frame FS-MIL

Intra-frame FS-MIL pattern corresponds to physical channel [symbol rate]. Table 1-2 shows examples of the intra-frame FS-MIL pattern for each interleaving size [frames].

Table 1-2 Example of the intra-frame FS-MIL pattern for each physical channel [symbol rate]

Physical channel	Symbol rate [ksps]	The number of bits in a frame [bits]	Interleaving pattern of the intra-frame FS-MIL
Downlink DPCH	8	64	64[4[2x2]x16[4[2x2]x4[2x2]]]
	16	160	160[10[5[3x2]x2]x16[4[2x2]x4[2x2]]]
	32	480	480[30[6[3x2]x5[2x3]]x16[4[2x2]x4[2x2]]]
	64	1120	1120[70[10[5[3x2]x2]x7[3x3[2x2]]]x16[4[2x2]x4[2x2]]]
	128	2400	2400[150[15[5[2x3]x3]x10[5[3x2]x2]]x16[4[2x2]x4[2x2]]]
	256	4832	4832[302[19[5[2x3]x4[2x2]]x16[4[2x2]x4[2x2]]]x16[4[2x2]x4[2x2]]]
	512	9952	9952[622[32[8[4[2x2]x2]x4[2x2]]x20[4[2x2]x5[3x2]]]x16[4[2x2]x4[2x2]]]
	1024	20192	20192[1262[40[8[4[2x2]x2]x5[2x3]]x32[8[4[2x2]x2]x4[2x2]]]x16[4[2x2]x4[2x2]]]
	2048	40416	40416[2526[79[10[5[3x2]x2]x8[4[2x2]x2]]x32[8[4[2x2]x2]x4[2x2]]]x16[4[2x2]x4[2x2]]]
	4096	81376	81376[5086[80[10[5[3x2]x2]x8[4[2x2]x2]]x64[8[4[2x2]x2]x8[4[2x2]x2]]]x16[4[2x2]x4[2x2]]]
Uplink DPCH	16	160	160[10[5[3x2]x2]x16[4[2x2]x4[2x2]]]
	32	320	320[20[4[2x2]x5[3x2]]x16[4[2x2]x4[2x2]]]
	64	640	640[40[8[4[2x2]x2]x5[2x3]]x16[4[2x2]x4[2x2]]]
	128	1280	1280[80[10[5[3x2]x2]x8[4[2x2]x2]]x16[4[2x2]x4[2x2]]]
	256	2560	2560[160[16[4[2x2]x4[2x2]]x10[5[3x2]x2]]x16[4[2x2]x4[2x2]]]
	512	5120	5120[320[20[4[2x2]x5[3x2]]x16[4[2x2]x4[2x2]]]x16[4[2x2]x4[2x2]]]
	1024	10240	10240[640[32[8[4[2x2]x2]x4[2x2]]x20[4[2x2]x5[3x2]]]x16[4[2x2]x4[2x2]]]
	2048	20480	20480[1280[40[8[4[2x2]x2]x5[2x3]]x32[8[4[2x2]x2]x4[2x2]]]x16[4[2x2]x4[2x2]]]
Defin L 0, 1, 2, ...	4096	40960	40960[2560[80[10[5[3x2]x2]x8[4[2x2]x2]]x32[8[4[2x2]x2]x4[2x2]]]x16[4[2x2]x4[2x2]]]