April 15, 2019

Ms. Susanna Kooistra
Mr. Maurice Pope
3GPP Mobile Competence Centre (ETSI)
650, Route Des Lucioles
06921 Sophia-Antipolis
France

Subject: **Nomination of Mr. Puneet Jain as candidate for 3GPP TSG SA WG2 Chairman**

Dear Susanna, Dear Maurice,

On behalf of Intel (ATIS member), I am pleased to nominate Mr. Puneet Jain as candidate for the position of 3GPP TSG SA WG2 Chairman.

Mr. Puneet Jain has 21 years of experience in standardization, research and product development in telecom and wireless industry. He currently serves as the Vice Chairman of TSG SA WG2, since 2015. With strong experience in standards as well as knowledge of mobile systems and terminals, we are confident that Mr. Puneet Jain will bring very positive influence and contributions to 3GPP TSG SA WG2.

Mr. Puneet Jain is informed about and aware of the antitrust/competition laws and regulations of relevant jurisdictions, and he shall comply with such laws while acting in his capacity as TSG SA WG2 Chairman.

Intel is fully committed to provide the necessary support and resources to ensure that Puneet accomplishes the duties and carries out his responsibilities as the Chairman of 3GPP TSG SA WG2 if elected.

Yours sincerely,

Asha R Keddy
Corporate Vice President
General Manager, Next Generation and Standards (NGS)

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Position of candidacy: 3GPP TSG SA WG2 Chairman

Candidate Name: Puneet Jain

Member: Intel

Partner Organization: ATIS

Brief Curriculum Vitae:

Puneet Jain is a Principal Engineer in Next Generation and Standards (NGS) at Intel Corporation since March, 2001. At Intel he is driving research and standardization on MAC, RAN, and end-to-end network system architecture for mobile broadband technologies such as 4G LTE and 5G.

Puneet has 21+ years of rich experience in standardization, research and product development in telecom and wireless industry. He has participated in various global standardization bodies that includes 3GPP, WiMAX Forum, IEEE 802.16j, ETSI TC M2M, oneM2M, GSMA, NPF, and ATIS. Puneet currently serves as the Vice Chairman of TSG SA WG2, since 2015. As TSG SA WG2 Vice Chairman, Puneet has chaired numerous sessions on 3GPP, non-3GPP and 5G tracks.

Puneet is head of Intel delegation in 3GPP SA WG2 since 2010 and active contributor to SA WG2 and TSG SA since 2006. He has served as Rapporteur of several study/work items - SIMTC, MTCe-SDDTE, AESE, MONTE, FS_AE_CIoT, CIoT, FS_CIoT_Ext, CIoT_Ext on Machine Type Communication (MTC)/Cellular Internet of Things (CIoT) since 3GPP Rel-11 in SA WG2 and has chaired many drafting and breakout sessions.

Puneet has also served as oneM2M Steering Committee Vice Chairman (2014–2016). He was active contributor to oneM2M functional Architecture and oneM2M-3GPP interworking aspects.

In his previous roles at Intel, he was chairman of WiMAX-3GPP interworking subteam at WiMAX Forum, involved in design and development of ATM RAN reference implementation for Intel Network Processors, design and development for Modular Building Blocks for IP/UDP Header compression/decompression in 3G Networks and standardization of ATM Functional API at Network Processing Forum.

Prior to Intel, he worked at Centre for Development of Telematics (C-DoT) in India where he led a team for design and development for Mobility Management and BSS Application Protocol for GSM MSC/VLR and was key contributor to technical evaluation and network configuration of C-DoT MSC/VLR during launch of Indian Mobile Personal Communication Services (IMPCS) by Department of Telecommunications, Government of India.

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