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Title: Impact of OHG harmonization recommendation on UTRA/FDD and UTRA/TD

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1 Introduction

The Operators Harmonization Group (OHG) has recommended a harmonization of the two main CDMA-based 3G concepts, UTRA and cdma2000, into a common concept based on three modes; Direct-spread/FDD (DS), Multi-carrier FDD (MC), and TDD. The OHG recommendation includes specific proposals regarding chip rate, pilot, and synchronization for the DS mode. These proposals imply the following modifications to the physical layer of UTRA/FDD:

- A change of chip rate from 4.096 Mcps to 3.84 Mcps to allow for easier dual-mode implementation with 3.6864 Mcps MC mode.

- Modification of the common pilot structure of UTRA/FDD from a TDM common pilot to a CDM common pilot

- More flexibility in the number of pilot symbols for dedicated channels

The chip rate of the TDD mode is also recommended to be changed to 3.84 Mcps, i.e. the same as for the Direct-spread mode.

We support these proposals and recommend that WG1 should, without delay, initiate studies how the modifications can be incorporated in the specification documents .

In this paper we identify parts of the current UTRA/FDD specification that need to be modified in order to implement the OHG recommendation. It should be noted that the list may not necessarily be complete. We also outline proposals how these modifications can be implemented. The main proposal is to reduce the number of slots per frame from 16 to

15. Further proposals for some more detailed modifications are also given. These proposals should be seen as a starting point for the WG1 discussions.

A short discussion on the impact of a change of chip rate for the TDD mode is also given.

It should be noted that the more detailed comments and proposals outlined in this paper are assuming the current state of the specification. Some parts of the specification are still under discussion. If modifications are made to the specification based on these discussions, the related proposals in this paper obviously need to be modified as well.

2   Effects of 3.84 Mcps on the FDD mode

With a chip rate of 3.84 Mcps, the number of chips per second is reduce by 15/16, compared to a chip rate of 4.096 Mcps. A modified chip rate can affect the basic L1 structure in different ways:

 The frame size can be increased with a factor 16/15, keeping the number of slots per frame, number of symbols per slot, and number of chips per symbol constant. The frame length would then no longer be 10 ms. However, source coders typically output information blocks at multiples of 10 ms. Most notably, the AMR speech codec has a 20 ms frame length, i.e. data is delivered down to L1 every20 ms for transmission in the radio frames. Consequently, modifying the frame length is not a good solution.

* The slot structure (number of symbols per slot) can be changed, keeping the frame length, number of slots per frame, and number of chips per symbol constant However, this is not a good solution either since the number of symbols per frame cannot be divided evenly by 15, so the number of symbols per slots will not be constant.

* The spreading factors (number of chips per symbol) can be changed, keeping the frame length, number of slots per frame, and number of symbols per slot constant However, this is not a good solution either, because this would mean moving away from the orthogonal variable spreading factor codes that need lengths of the form 2^n.

* The number of slots per frame can be changed from 16 to 15, keeping the frame length, slot structure, and number of chips per frame constant. In our view, this leads to the minimum changes at layer 1. We thus propose that a change of chip rate to 3.84 Mcps should e based on a reduction of the number of slots per frame from 16 to 15. In the following, the impacts of this are analyzed.

2.1   Scrambling codes

The length of both the uplink and downlink scrambling codes are 10 ms, corresponding to one frame. With the current chip rate of 4.096 Mcps, the scrambling codes are implemented as much longer codes, terminated after 40960 chips. For a chip rate of 3.84 Mcps, the codes should simply be terminated after 38400 chips instead. This is a very minor change, affecting 25.213 clauses 4.3.2.2 and 5.2.2.

2.2   TFCI coding

The current TFCI coding is dependent on a 16 slot structure, using (16, 5) or (32, 6) codes, with possible equal repetition of the coded bits before distributing them evenly over the 16 slots. For a 15 slot frame structure the TFCI code should be of the form (n, k), where n is instead a multiple of 15 and k takes the values 5 or 6.

The current TFCI code allows for very simple decoding using a fast Hadamard transform. It is important that a new TFCI code is equally simple to decode.

The most straightforward solution is to shorten the existing codes, i.e. the last one or two bits are removed. The punctured symbols are then just replaced with zeros in the fast Hadamard transform decoding. With this approach the following codes are obtained:

-    The (32, 6) code is shortened with two bits, i.e. the new code is (30, 6). In the current code, all code words has a Hamming distance of 16 to 62 code word, and the distance 32 to one code word, i.e. the weight enumerator $W(X) = 62X^{16} + X^{32}$. For the new shortened code this will become $W(X) = 15X^{14} + 32X^{15} + 15X^{16} + X^{30}$.

-    The (16, 5) code is shortened with one bit, i.e. the new code is (15, 5). The current code has the weight enumerator $W(X) = 30X^8 + X^{16}$. For the new shortened code this will become $W(X) = 15X^7 + 15X^8 + X^{15}$.

As can be seen, the distance properties of the codes are not drastically affected, and it is believed that the new codes will have similar error rate performance as the old codes, possibly with a loss of a few tenths of dB in required SIR to obtain a certain error rate.

2.3 Secondary SCH search codes

Currently, the secondary SCH search code are comma free codes of length 16, over GF(17). Changing to 15 slots per 10 ms frame, means that the second search code needs to be of length 15 symbols over some alphabet.

One solution is to replace the RS(16, 3) code over GF(17) with a RS(15, 3) code over $GF(2^4)$. An additional advantage of the new code is that it is more suited for on-line computation than the GF(17) code which needs modulo 17 arithmetic implemented.

The primary SCH code is kept as before, while there will now be 16 (17 before) secondary SCH codes of length 256 chips. Hence, one of the 17 secondary SCH codes is dropped. The Hadamard transform receiver can be kept for the secondary SCH.

The RS(15, 3) code over $GF(2^4)$ contains 272 cyclically distinct (comma-free) code words. From these we pick 32 different code words to represent the 32 different code groups. One such set of 32 code words is listed below:

```
13,  5, 15,  6, 13, 13, 15,  8, 10,  7, 16, 12,  2,  1,  1
12,  9, 16, 11, 12, 12, 16, 15,  2, 13, 14,  6,  3,  1,  1
 8, 13,  2, 16,  8,  8,  2, 10,  9, 11,  3, 15,  4,  1,  1
 6,  4, 14,  8,  6,  6, 14, 16,  3, 12, 10, 11,  5,  1,  1
10,  8,  4,  3, 10, 10,  4,  9, 12, 14,  7,  2,  6,  1,  1
15, 12,  3, 14, 15, 15,  3,  2,  4,  8,  5, 16,  7,  1,  1
 3, 16, 13,  9,  3,  3, 13,  7, 11,  2, 12,  5,  8,  1,  1
11,  7, 10, 15, 11, 11, 10, 14,  5,  6,  2,  8,  9,  1,  1
 7,  3,  8, 12,  7,  7,  8, 11, 14,  4, 15, 13, 10,  1,  1
 2, 15,  7,  5,  2,  2,  7,  4,  6, 10, 13,  3, 11,  1,  1
14, 11,  9,  2, 14, 14,  9,  5, 13, 16,  4, 10, 12,  1,  1
16,  6,  5, 10, 16, 16,  5,  3,  7, 15,  9, 14, 13,  1,  1
 4,  2, 11, 13,  4,  4, 11,  6, 16,  9,  8,  7, 14,  1,  1
 5, 14, 12,  4,  5,  5, 12, 13,  8,  3,  6,  9, 15,  1,  1
 9, 10,  6,  7,  9,  9,  6, 12, 15,  5, 11,  4, 16,  1,  1
14,  7, 13, 16,  9,  2,  5, 11, 12,  7,  6,  7,  1,  2,  1
 2,  3,  3, 11,  5, 14, 11, 14,  3,  1, 11, 14,  2,  2,  1
 7, 15,  4,  6,  4, 11, 12,  5, 11, 11,  9,  4,  3,  2,  1
11, 11, 14,  1, 16,  7,  6,  4,  4, 13,  8,  9,  4,  2,  1
 9,  6,  2,  9, 14,  5, 10,  6, 10, 14, 13, 13,  5,  2,  1
 5,  2, 16, 14,  2,  9,  8,  3,  1, 12,  4,  8,  6,  2,  1
 4, 14, 15,  3,  7, 16,  7, 12,  9,  2,  2, 10,  7,  2,  1
16, 10,  1,  8, 11,  4,  9, 13,  2,  8, 15,  3,  8,  2,  1
 8,  1,  6,  2,  3, 12, 14,  8, 16,  4,  5,  2,  9,  2,  1
12,  5, 12,  5, 15,  8,  4,  1,  7,  6, 12, 11, 10,  2,  1
13,  9, 11, 12, 10,  1,  3, 10, 15, 16, 10,  5, 11,  2,  1
 3,  4,  9,  7,  8, 15,  1,  9, 14,  9, 14, 12, 13,  2,  1
15,  8,  7,  4, 12,  3, 15, 16,  5, 15,  3,  1, 14,  2,  1
10, 12,  8, 13, 13,  6, 16,  7, 13,  5,  1, 15, 15,  2,  1
 6, 16, 10, 10,  1, 10,  2,  2,  6,  3, 16,  6, 16,  2,  1
10, 13, 12, 14,  4,  3,  9,  8,  6, 13, 11, 13,  1,  3,  1
 6,  9,  6,  9, 16, 15,  7,  1, 13, 11,  6,  8,  2,  3,  1
```

There has been a proposal from Ericsson to increase the number of code groups to 256. That would also be possible since there are 272 code words to choose from, and only 256 of them need to be picked.

Since the codes are shorter, this will lead to somewhat degraded code distance properties. However, it is believed that the difference is small enough to only have negligible impact on performance.

2.4 Paging channel

The current paging channel uses an intricate interleaving of paging flags and message. Changing the interleaving of paging flags and message is not straightforward. On the other hand, there is no direct correspondence between the slot structure and frame structure on the paging channel, so letting the frame structure "slip" is not a problem. This means that the current slot structure for the PCH can be maintained even with the new chip rate. That would mean that instead of the current 288 paging instants per 720 ms super frame, there will be 288×15/16 = 270 groups per 720 ms super frame.

2.5   Random access channel

On the random access channel, there are currently 8 access slots per frame, where one access slot is equal to two ordinary slots. The same structure can be used also for a chip rate of 3.84 Mcps and 15 slots per frame. The difference is that the access slots will then only be time aligned to the frame boundaries of every second frame, e.g. every odd frame. As there is anyway no other relation between the random access timing and the ordinary frame timing, this does not cause any problems.

The timing of the preamble and acquisition indicator will be affected as well since the access slots will be 1.333 ms instead of 1.25 ms. If the structure of the preamble and acquisition indicator is maintained (i.e. the number of chips is kept constant), the length measured in time for these signals increases. Maintaining the offset $T_a = 0.5$ ms, the lower chip rate leads to slightly increased processing times, which obviously is an advantage. The slightly increased delay is not seen as having significant impact on the random access scheme.

2.6   Channel interleaver

The final selection of the channel interleaver has not yet been done. Before the selection is done, it should be verified that the output of the 2nd step channel interleaving can be mapped onto 15 slots, and that there is no fixed requirement to map it onto 16 slots. It should be noted that the output mapping should anyway not be fixed, in order to support compressed mode.

2.7   Compressed mode

One of the alternatives to create compressed frames in compressed mode is to reduce the spreading factor by a factor of two. With 16 slots per frame this results in 8 slots completely filled with data and 8 empty slots. With 15 slots per frame, there will be one slot filled with data to only 50%. However this is not seen as a big problem. It should be noted that the details of the mapping of data into the slots during compressed frames has anyway not yet finalised and remains as an open issue in 3GPP.

2.8   Coding for slow power control

The coding for the slow power control feedback signaling is related to the TFCI coding, since the same coding as for the TFCI is used. The current scheme used is dependent on 16 slots per frame. However, the same solution can be applied for this coding, i.e. the modified TFCI coding is used instead.

2.9   Feedback signalling for TX diversity

Currently, the feedback mode for TX diversity has signalling word update rates of 1600, 800, and 400 Hz (one word every 1, 2 and 4 slots respectively), i.e. the update rate fits nicely into the 16 slot frame structure. When 15 slots per frame is used instead, the signalling words will start to slip over the frame boundaries, i.e. the entire signalling word is not received within one 10 ms frame, but is split over two frames. It is believed that this does not have any serious effect on the implementation but is more of a "cosmetic" issue .

2.10   TPC puncturing for SSDT

In SSDT the primary cell ID code is transmitted using puncturing of TPC bits. The period of the primary cell update is 100, 200 or 400 Hz (every 16, 8 and 4 slots respectively), i.e. the update rate fits nicely into the 16 slot frame structure. When 15 frames per frame is used instead, a similar slip of the signalling over the frames as for the TX diversity feedback will happen. For SSDT this can be more of a problem, since it is then not as straightforward to determine from which frame the command should be applied. However, also for this case the problem is seen as more cosmetic.

2.11   Pilot patterns

The pilot patterns used for frame synchronization are optimised for 16 slots per frame. It my not be straightforward to shorten them. This means that new pilot patterns need to be found that are optimised for 15 slots per frame.

2.12 STTD encoding

When using STTD encoding for the open loop TX diversity, symbols are STTD encoded/decoded in pairs. If there are an odd number of data symbols in each slot, then the slots are grouped two and two, and the last symbol in the first slot is encoded together with the first symbol of the following slot. With 16 slots per frame this operation is rather straightforward. However, with 15 slots per frame, when the number of data symbols per slot is an odd number, then the last slot of a frame will need to be encoded together with the first slot of the following frame. This means that two consecutive 10 ms frames cannot be encoded/detected/decoded separately. This leads to increased delays in the receiver processing, and increased buffering requirements for the case when interleaving is carried out over only one 10 ms frame.

Another possibility would be to not STTD decode the final odd symbol, i.e. maximum one symbol per frame would not see the same diversity gain as the other symbols.

3 Effects of CDM common pilot on the FDD mode

Figure 1 illustrates the current structure of the primary CCPCH. It consists of three parts

- A data part carrying the BCH.

- A set of pilot symbols. These pilot symbols can be used to support coherent detection of channels transmitted with the same antenna pattern as the Primary CCPCH and can thus be seen as a common pilot time-multiplexed with the BCH.

- An unused part corresponding to the transmission of the SCH.

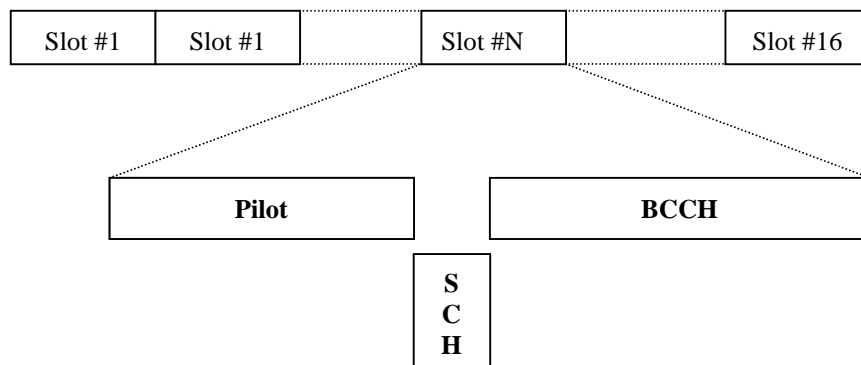The primary CCPCH is transmitted on a channelization code using a spreading factor of 256.

Figure 1: Current structure of Primary CCPCH with time multiplexed common pilot.

To implement a code-multiplexed common pilot, we propose that the common pilot is separated from the Primary CCPCH and transmitted on a separate code channel, see Figure 2. Both the pilot and the Primary CCPCH should be transmitted on channelization codes using a spreading factor of 256. It should be noted that the exact channelization codes of both the pilot and the Primary CCPCH need to be specified.
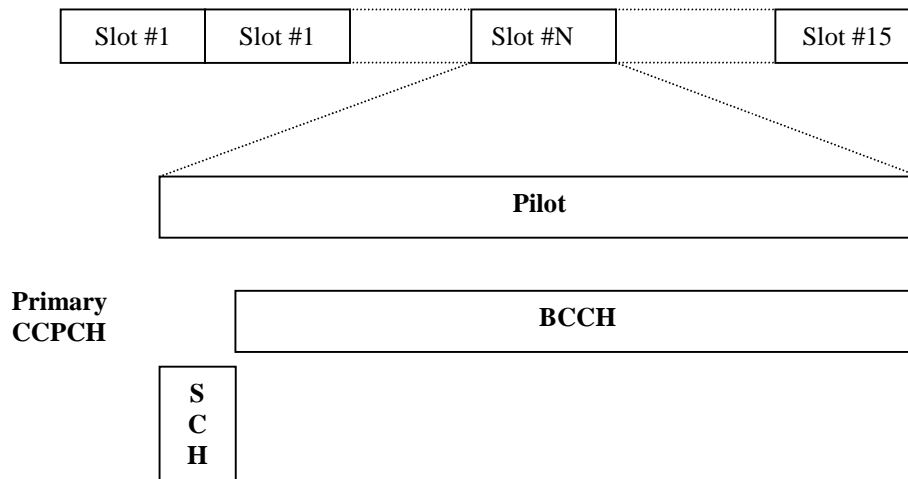
| Slot #1 | Slot #1 | | Slot #N | | Slot #15 |

Pilot

Primary CCPCH

BCCH

S C H

Figure 2: Proposed structure of Primary CCPCH with code-multiplexed common pilot.

The introduction of a CDM common pilot will have some impact on the downlink physical channels. The relevant sections of 25.211 therefore has to be somewhat revised. Some editorial adjustments might also be required in 25.214. There is no direct impact on the upper layer structure and procedures, however the payload and numerology of different channels are affected. Appropriate liaison to WG2 might therefore be necessary. The following sections describe the impact on the physical downlink channel structure.

Common Pilot Channel (CPICH)

The CPICH is a new unmodulated (SF=256) down-link physical channel used by the terminal equipment to perform searching and identification (3rd step) as well as channel tracking and channel estimation. The frame structure of the CPICH is illustrated in Figure 2. The CPICH is transmitted continuously (100% duty cycle).

The base station always transmits one CPICH using a unique pre-defined OVSF. The base station may transmit additional CPICH to be used in support of transmit antenna diversity techniques or spot beams. Note that the current scrambling principle and synchronisation procedure remain unchanged (i.e. different codes for different cell). In particular the 3rd step of synchronisation procedure (determination of long code) is preserved.

PCCPCH

The structure of the PCCPCH is derived from the current UTRA-FDD PCCPCH by removing the pilot bits. The frame structure of the modified PCCPCH is shown in Figure 2. This results in an extension of the PCCPCH/BCCH payload, assuming the same spreading factor as of today..

SCCPCH

The structure of the SCCPCH is derived from the current UTRA-FDD SCCPCH. The main difference is the addition of a new set of slot structures with Npilot=0 to be used when the SCCPCH is transmitted over the entire cell (broadcast) as opposed to a specific user (directive antenna). In this case, the SCCPCH payload is increased, assuming the same spreading factor.

PSCCCH

The structure of the PSCCCH is derived from the current UTRA-FDD PSCCCH by removing the pilot bits.

PDSCH, AICH, SCH

The PDSCH, AICH and SCH are not affected by the CDM common pilot. However, as described in Section 2, at least some of them are affected by the change of chip rate.

DPCH

The continuous common pilot can, in many cases, be used by the UE to perform part or all of the channel estimation. In these cases, the system can use a DCH frame format with a lower number or without dedicated pilot bits (the exact range of Npilot is TBD according to OHG report), resulting in a higher payload for a given spreading factor.. Note that when directive antennas are used the UE can only rely on dedicated pilot bits for all channel estimations and the current UTRA-FDD frame format shall be used.

4   Effect on TDD

In the present design of UTRA, the FDD and TDD modes are well harmonised. In particular, the chip rates in UTRA/FDD and UTRA/TDD have been chosen to be equal to allow easy dual mode implementation. Given that the chip rate of UTRA/FDD will change to 3.84 Mcps, the chip rate of UTRA/TDD should change to the same value. For the same reasons as mentioned in section 2 for UTRA/FDD, also for UTRA/TDD this change of the chip rate should be implemented by reducing the number of slots per 10 ms frame from 16 to 15. Using 15 slots per 10 ms frame for UTRA/TDD has impact on similar issues as listed above for UTRA/FDD. Ongoing studies show that viable solutions of these issues can be found requiring only minor changes in UTRA/TDD. In order to maintain the good harmonisation between UTRA/FDD and UTRA/TDD, it should be considered that the solutions for UTRA/TDD should, if possible, be well in line with the solutions for UTRA/FDD.