Technical Specification Group Services and System Aspects
Meeting #4, Miami, USA, 21-23 June 1999

TSGS#4(99)315

Source: **TSG-RAN**

Title: **Technical Discussion Materials related to OHG Proposal**

Document for: **Discussion/Information**

Agenda Item:

This document includes contributions related to the technical aspect of OHG proposals.

It includes input contributions;

PROPOSAL TO IMPLEMENT THE OHG PROPOSAL IN 3GPP (TSGR#4(99)402,

Impact of OHG harmonization recommendation on UTRA/FDD and UTRA/TDD (TSGR#4(99)320, Annex)

Liaison statement on Impact of OHG harmonization recommendation on UTRA/FDD and UTRA/TDD (TSGR#4(99)383)

Analysis of the OHG proposal (TSGR#4(99)398)

Based on above documents, TSG-RAN agreed on the proposal in TSGR#4(99)402.

TSG RAN
Meeting #4, Miami, USA, 17-19 June 1999

TSGR#4(99)402

Source:	**Alcatel, Ericsson, Fujitsu, Japan Telecom, Lucent Technologies, Mannesmann Mobilfunk, Mitsubishi, Motorola, NEC, Nokia, Nortel Networks, NTT DoCoMo, Omnitel, Panasonic, Qualcomm, Samsung, Siemens, Telia, TIM, T-Mobil, Vodafone**
Title:	**PROPOSAL TO IMPLEMENT THE OHG PROPOSAL IN 3GPP**
Document for:	**Decision**
Agenda Item:	

The source companies propose that TSG RAN implement the below modifications

- change of chip rate into 3.84 Mcps
- downlink pilot structure (CDM common pilot, TDM dedicated pilot (number of pilot bits to be decided))

and start on defining the hooks and extensions as proposed by OHG.

ANNEX 1. To Tdoc 320

TSG-RAN Working Group 1 meeting #5 *TSGR1#5(99)677*
Cheju Island, Korea
June 1-4, 1999

Agenda item: 3G Harmonization
Source: Alcatel, CSELT/TIM, DoCoMo, Ericsson, Fujitsu, InterDigital, Japan Telecom, LGIC, Lucent Technologies, Matsushita, Mitsubishi, Motorola, NEC, Nokia, Nortel Networks, Qualcomm, Panasonic, Samsung, Siemens, Telia, Texas Instrument, Toshiba, Vodafone
Title: Impact of OHG harmonization recommendation on UTRA/FDD and UTRA/TDD
Document for:

1 Introduction

The Operators Harmonization Group (OHG) has recommended a harmonization of the two main CDMA-based 3G concepts, UTRA and cdma2000, into a common concept based on three modes; Direct-spread/FDD (DS), Multi-carrier FDD (MC), and TDD. The OHG recommendation includes specific proposals regarding chip rate, pilot, and synchronization for the DS mode. These proposals imply the following modifications to the physical layer of UTRA/FDD:

- A change of chip rate from 4.096 Mcps to 3.84 Mcps to allow for easier dual-mode implementation with 3.6864 Mcps MC mode.
- Modification of the common pilot structure of UTRA/FDD from a TDM common pilot to a CDM common pilot
- More flexibility in the number of pilot symbols for dedicated channels

The chip rate of the TDD mode is also recommended to be changed to 3.84 Mcps, i.e. the same as for the Direct-spread mode. We support these proposals and recommend that WG1 should, without delay, initiate studies how the modifications can be incorporated in the specification documents .
In this paper we identify parts of the current UTRA/FDD specification that need to be modified in order to implement the OHG recommendation. It should be noted that the list may not necessarily be complete. We also outline proposals how these modifications can be implemented. The main proposal is to reduce the number of slots per frame from 16 to 15. Further proposals for some more detailed modifications are also given. These proposals should be seen as a starting point for the WG1 discussions. A short discussion on the impact of a change of chip rate for the TDD mode is also given.
It should be noted that the more detailed comments and proposals outlined in this paper are assuming the current state of the specification. Some parts of the specification are still under discussion. If modifications are made to the specification based on these discussions, the related proposals in this paper obviously need to be modified as well.

2 Effects of 3.84 Mcps on the FDD mode

With a chip rate of 3.84 Mcps, the number of chips per second is reduce by 15/16, compared to a chip rate of 4.096 Mcps. A modified chip rate can affect the basic L1 structure in different ways:
The frame size can be increased with a factor 16/15, keeping the number of slots per frame, number of symbols per slot, and number of chips per symbol constant. The frame length would then no longer be 10 ms. However, source coders typically output information blocks at multiples of 10 ms. Most notably, the AMR speech codec has a 20 ms frame length, i.e. data is delivered down to L1 every20 ms for transmission in the radio frames. Consequently, modifying the frame length is not a good solution.

- The slot structure (number of symbols per slot) can be changed, keeping the frame length, number of slots per frame, and number of chips per symbol constant However, this is not a good solution either since the number of symbols per frame cannot be divided evenly by 15, so the number of symbols per slots will not be constant.
- The spreading factors (number of chips per symbol) can be changed, keeping the frame length, number of slots per frame, and number of symbols per slot constant However, this is not a good solution either, because this would mean moving away from the orthogonal variable spreading factor codes that need lengths of the form 2^n.
- The number of slots per frame can be changed from 16 to 15, keeping the frame length, slot structure, and number of chips per frame constant. In our view, this leads to the minimum changes at layer 1. We thus propose that a change of chip rate to 3.84 Mcps should e based on a reduction of the number of slots per frame from 16 to 15. In the following, the impacts of this are analyzed.

2.1 Scrambling codes

The length of both the uplink and downlink scrambling codes are 10 ms, corresponding to one frame. With the current chip rate of 4.096 Mcps, the scrambling codes are implemented as much longer codes, terminated after 40960 chips. For a chip rate of 3.84 Mcps, the codes should simply be terminated after 38400 chips instead. This is a very minor change, affecting 25.213 clauses 4.3.2.2 and 5.2.2.

2.2 TFCI coding

The current TFCI coding is dependent on a 16 slot structure, using (16, 5) or (32, 6) codes, with possible equal repetition of the coded bits before distributing them evenly over the 16 slots. For a 15 slot frame structure the TFCI code should be of the form (*n*, *k*), where *n* is instead a multiple of 15 and *k* takes the values 5 or 6.
The current TFCI code allows for very simple decoding using a fast Hadamard transform. It is important that a new TFCI code is equally simple to decode.
The most straightforward solution is to shorten the existing codes, i.e. the last one or two bits are removed. The punctured symbols are then just replaced with zeros in the fast Hadamard transform decoding. With this approach the following codes are obtained:

- The (32, 6) code is shortened with two bits, i.e. the new code is (30, 6). In the current code, all code words has a Hamming distance of 16 to 62 code word, and the distance 32 to one code word, i.e. the weight enumerator $W(X) = 62X^{16} + X^{32}$. For the new shortened code this will become $W(X) = 15X^{14} + 32X^{15} + 15X^{16}+X^{30}$.

- The (16, 5) code is shortened with one bit, i.e. the new code is (15, 5). The current code has the weight enumerator $W(X) = 30X^{8} + X^{16}$. For the new shortened code this will become $W(X) = 15X^{7} + 15X^{8} + X^{15}$.

As can be seen, the distance properties of the codes are not drastically affected, and it is believed that the new codes will have similar error rate performance as the old codes, possibly with a loss of a few tenths of dB in required SIR to obtain a certain error rate.

2.3 Secondary SCH search codes

Currently, the secondary SCH search code are comma free codes of length 16, over GF(17). Changing to 15 slots per 10 ms frame, means that the second search code needs to be of length 15 symbols over some alphabet.
One solution is to replace the RS(16, 3) code over GF(17) with a RS(15, 3) code over $GF(2^4)$. An additional advantage of the new code is that it is more suited for on-line computation than the GF(17) code which needs modulo 17 arithmetic implemented.
The primary SCH code is kept as before, while there will now be 16 (17 before) secondary SCH codes of length 256 chips. Hence, one of the 17 secondary SCH codes is dropped. The Hadamard transform receiver can be kept for the secondary SCH.
The RS(15, 3) code over $GF(2^4)$ contains 272 cyclically distinct (comma-free) code words. From these we pick 32 different code words to represent the 32 different code groups. One such set of 32 code words is listed below:

```
13,  5, 15,  6, 13, 13, 15,  8, 10,  7, 16, 12,  2,  1,  1
12,  9, 16, 11, 12, 12, 16, 15,  2, 13, 14,  6,  3,  1,  1
 8, 13,  2, 16,  8,  8,  2, 10,  9, 11,  3, 15,  4,  1,  1
 6,  4, 14,  8,  6,  6, 14, 16,  3, 12, 10, 11,  5,  1,  1
10,  8,  4,  3, 10, 10,  4,  9, 12, 14,  7,  2,  6,  1,  1
15, 12,  3, 14, 15, 15,  3,  2,  4,  8,  5, 16,  7,  1,  1
 3, 16, 13,  9,  3,  3, 13,  7, 11,  2, 12,  5,  8,  1,  1
11,  7, 10, 15, 11, 11, 10, 14,  5,  6,  2,  8,  9,  1,  1
 7,  3,  8, 12,  7,  7,  8, 11, 14,  4, 15, 13, 10,  1,  1
 2, 15,  7,  5,  2,  2,  7,  4,  6, 10, 13,  3, 11,  1,  1
14, 11,  9,  2, 14, 14,  9,  5, 13, 16,  4, 10, 12,  1,  1
16,  6,  5, 10, 16, 16,  5,  3,  7, 15,  9, 14, 13,  1,  1
 4,  2, 11, 13,  4,  4, 11,  6, 16,  9,  8,  7, 14,  1,  1
 5, 14, 12,  4,  5,  5, 12, 13,  8,  3,  6,  9, 15,  1,  1
 9, 10,  6,  7,  9,  9,  6, 12, 15,  5, 11,  4, 16,  1,  1
14,  7, 13, 16,  9,  2,  5, 11, 12,  7,  6,  7,  1,  2,  1
 2,  3,  3, 11,  5, 14, 11, 14,  3,  1, 11, 14,  2,  2,  1
 7, 15,  4,  6,  4, 11, 12,  5, 11, 11,  9,  4,  3,  2,  1
11, 11, 14,  1, 16,  7,  6,  4,  4, 13,  8,  9,  4,  2,  1
 9,  6,  2,  9, 14,  5, 10,  6, 10, 14, 13, 13,  5,  2,  1
 5,  2, 16, 14,  2,  9,  8,  3,  1, 12,  4,  8,  6,  2,  1
 4, 14, 15,  3,  7, 16,  7, 12,  9,  2,  2, 10,  7,  2,  1
16, 10,  1,  8, 11,  4,  9, 13,  2,  8, 15,  3,  8,  2,  1
 8,  1,  6,  2,  3, 12, 14,  8, 16,  4,  5,  2,  9,  2,  1
12,  5, 12,  5, 15,  8,  4,  1,  7,  6, 12, 11, 10,  2,  1
13,  9, 11, 12, 10,  1,  3, 10, 15, 16, 10,  5, 11,  2,  1
 3,  4,  9,  7,  8, 15,  1,  9, 14,  9, 14, 12, 13,  2,  1
15,  8,  7,  4, 12,  3, 15, 16,  5, 15,  3,  1, 14,  2,  1
10, 12,  8, 13, 13,  6, 16,  7, 13,  5,  1, 15, 15,  2,  1
 6, 16, 10, 10,  1, 10,  2,  2,  6,  3, 16,  6, 16,  2,  1
10, 13, 12, 14,  4,  3,  9,  8,  6, 13, 11, 13,  1,  3,  1
 6,  9,  6,  9, 16, 15,  7,  1, 13, 11,  6,  8,  2,  3,  1
```

There has been a proposal from Ericsson to increase the number of code groups to 256. That would also be possible since there are 272 code words to choose from, and only 256 of them need to be picked.
Since the codes are shorter, this will lead to somewhat degraded code distance properties. However, it is believed that the difference is small enough to only have negligible impact on performance.

2.4 Paging channel

The current paging channel uses an intricate interleaving of paging flags and message. Changing the interleaving of paging flags and message is not straightforward. On the other hand, there is no direct correspondence between the slot structure and frame structure on the paging channel, so letting the frame structure "slip" is not a problem. This means that the current slot structure for the PCH can be maintained even with the new chip rate. That would mean that instead of the current 288 paging instants per 720 ms super frame, there will be 288×15/16 = 270 groups per 720 ms super frame.

2.5 Random access channel

On the random access channel, there are currently 8 access slots per frame, where one access slot is equal to two ordinary slots. The same structure can be used also for a chip rate of 3.84 Mcps and 15 slots per frame. The difference is that the access slots will then only be time aligned to the frame boundaries of every second frame, e.g. every odd frame. As there is anyway no other relation between the random access timing and the ordinary frame timing, this does not cause any problems.
The timing of the preamble and acquisition indicator will be affected as well since the access slots will be 1.333 ms instead of 1.25 ms. If the structure of the preamble and acquisition indicator is maintained (i.e. the number of chips is kept constant), the length measured in time for these signals increases. Maintaining the offset T_a = 0.5 ms, the lower chip rate leads to slightly increased processing times, which obviously is an advantage. The slightly increased delay is not seen as having significant impact on the random access scheme.

2.6 Channel interleaver

The final selection of the channel interleaver has not yet been done. Before the selection is done, it should be verified that the output of the 2nd step channel interleaving can be mapped onto 15 slots, and that there is no fixed requirement to map it onto 16 slots. It should be noted that the output mapping should anyway not be fixed, in order to support compressed mode.

2.7 Compressed mode

One of the alternatives to create compressed frames in compressed mode is to reduce the spreading factor by a factor of two. With 16 slots per frame this results in 8 slots completely filled with data and 8 empty slots. With 15 slots per frame, there will be one slot filled with data to only 50%. However this is not seen as a big problem. It should be noted that the details of the mapping of data into the slots during compressed frames has anyway not yet finalised and remains as an open issue in 3GPP.

2.8 Coding for slow power control

The coding for the slow power control feedback signaling is related to the TFCI coding, since the same coding as for the TFCI is used. The current scheme used is dependent on 16 slots per frame. However, the same solution can be applied for this coding, i.e. the modified TFCI coding is used instead.

2.9 Feedback signalling for TX diversity

Currently, the feedback mode for TX diversity has signalling word update rates of 1600, 800, and 400 Hz (one word every 1, 2 and 4 slots respectively), i.e. the update rate fits nicely into the 16 slot frame structure. When 15 slots per frame is used instead, the signalling words will start to slip over the frame boundaries, i.e. the entire signalling word is not received within one 10 ms frame, but is split over two frames. It is believed that this does not have any serious effect on the implementation but is more of a “cosmetic” issue .

2.10 TPC puncturing for SSDT

In SSDT the primary cell ID code is transmitted using puncturing of TPC bits. The period of the primary cell update is 100, 200 or 400 Hz (every 16, 8 and 4 slots respectively), i.e. the update rate fits nicely into the 16 slot frame structure. When 15 frames per frame is used instead, a similar slip of the signalling over the frames as for the TX diversity feedback will happen. For SSDT this can be more of a problem, since it is then not as straightforward to determine from which frame the command should be applied. However, also for this case the problem is seen as more cosmetic.

2.11 Pilot patterns

The pilot patterns used for frame synchronization are optimised for 16 slots per frame. It my not be straightforward to shorten them. This means that new pilot patterns need to be found that are optimised for 15 slots per frame.

2.12 STTD encoding

When using STTD encoding for the open loop TX diversity, symbols are STTD encoded/decoded in pairs. If there are an odd number of data symbols in each slot, then the slots are grouped two and two, and the last symbol in the first slot is encoded together with the first symbol of the following slot. With 16 slots per frame this operation is rather straightforward. However, with 15 slots per frame, when the number of data symbols per slot is an odd number, then the last slot of a frame will need to be encoded together with the first slot of the following frame. This means that two consecutive 10 ms frames cannot be encoded/detected/decoded separately. This leads to increased delays in the receiver processing, and increased buffering requirements for the case when interleaving is carried out over only one 10 ms frame.
Another possibility would be to not STTD decode the final odd symbol, i.e. maximum one symbol per frame would not see the same diversity gain as the other symbols.

3 Effects of CDM common pilot on the FDD mode

Figure 1 illustrates the current structure of the primary CCPCH. It consists of three parts

- A data part carrying the BCH.
- A set of pilot symbols. These pilot symbols can be used to support coherent detection of channels transmitted with the same antenna pattern as the Primary CCPCH and can thus be seen as a common pilot time-multiplexed with the BCH.
- An unused part corresponding to the transmission of the SCH.

The primary CCPCH is transmitted on a channelization code using a spreading factor of 256.

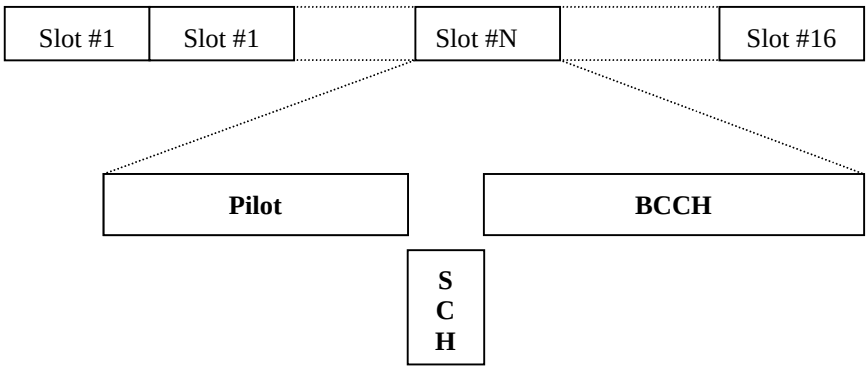

Figure 1: Current structure of Primary CCPCH with time multiplexed common pilot.

To implement a code-multiplexed common pilot, we propose that the common pilot is separated from the Primary CCPCH and transmitted on a separate code channel, see Figure 2. Both the pilot and the Primary CCPCH should be transmitted on channelization codes using a spreading factor of 256. It should be noted that the exact channelization codes of both the pilot and the Primary CCPCH need to be specified.

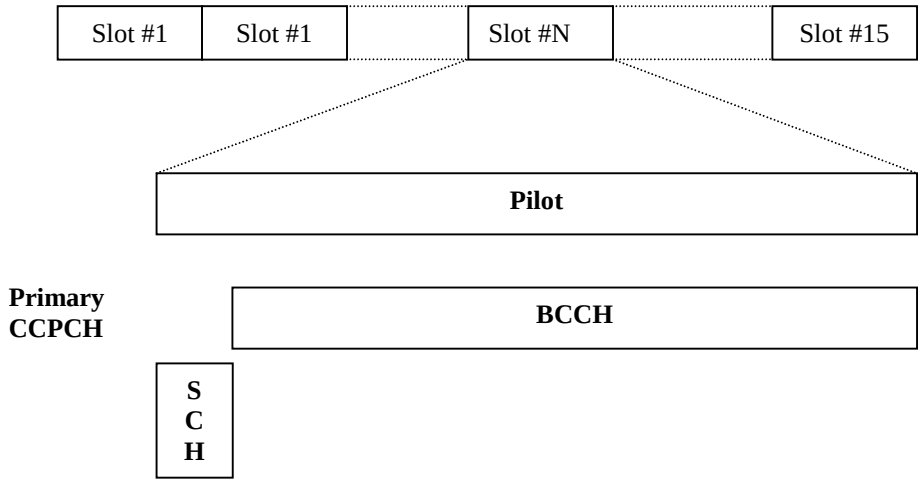

Figure 2: Proposed structure of Primary CCPCH with code-multiplexed common pilot.

The introduction of a CDM common pilot will have some impact on the downlink physical channels. The relevant sections of 25.211 therefore has to be somewhat revised. Some editorial adjustments might also be required in 25.214. There is no direct impact on the upper layer structure and procedures, however the payload and numerology of different channels are affected. Appropriate liaison to WG2 might therefore be necessary. The following sections describe the impact on the physical downlink channel structure.

Common Pilot Channel (CPICH)

The CPICH is a new unmodulated (SF=256) down-link physical channel used by the terminal equipment to perform searching and identification (3rd step) as well as channel tracking and channel estimation. The frame structure of the CPICH is illustrated in Figure 2. The CPICH is transmitted continuously (100% duty cycle).
The base station always transmits one CPICH using a unique pre-defined OVSF. The base station may transmit additional CPICH to be used in support of transmit antenna diversity techniques or spot beams. Note that the current scrambling principle and synchronisation procedure remain unchanged (i.e. different codes for different cell). In particular the 3rd step of synchronisation procedure (determination of long code) is preserved.

PCCPCH

The structure of the PCCPCH is derived from the current UTRA-FDD PCCPCH by removing the pilot bits. The frame structure of the modified PCCPCH is shown in Figure 2. This results in an extension of the PCCPCH/BCCH payload, assuming the same spreading factor as of today..

SCCPCH

The structure of the SCCPCH is derived from the current UTRA-FDD SCCPCH. The main difference is the addition of a new set of slot structures with Npilot=0 to be used when the SCCPCH is transmitted over the entire cell (broadcast) as opposed to a specific user (directive antenna). In this case, the SCCPCH payload is increased, assuming the same spreading factor.

PSCCCH

The structure of the PSCCCH is derived from the current UTRA-FDD PSCCCH by removing the pilot bits.

PDSCH, AICH, SCH

The PDSCH, AICH and SCH are not affected by the CDM common pilot. However, as described in Section 2, at least some of them are affected by the change of chip rate.

DPCH

The continuous common pilot can, in many cases, be used by the UE to perform part or all of the channel estimation. In these cases, the system can use a DCH frame format with a lower number or without dedicated pilot bits (the exact range of Npilot is TBD according to OHG report), resulting in a higher payload for a given spreading factor.. Note that when directive antennas are

used the UE can only rely on dedicated pilot bits for all channel estimations and the current UTRA-FDD frame format shall be used.

4 Effect on TDD

In the present design of UTRA, the FDD and TDD modes are well harmonised. In particular, the chip rates in UTRA/FDD and UTRA/TDD have been chosen to be equal to allow easy dual mode implementation. Given that the chip rate of UTRA/FDD will change to 3.84 Mcps, the chip rate of UTRA/TDD should change to the same value. For the same reasons as mentioned in section 2 for UTRA/FDD, also for UTRA/TDD this change of the chip rate should be implemented by reducing the number of slots per 10 ms frame from 16 to 15. Using 15 slots per 10 ms frame for UTRA/TDD has impact on similar issues as listed above for UTRA/FDD. Ongoing studies show that viable solutions of these issues can be found requiring only minor changes in UTRA/TDD. In order to maintain the good harmonisation between UTRA/FDD and UTRA/TDD, it should be considered that the solutions for UTRA/TDD should, if possible, be well in line with the solutions for UTRA/FDD.

TSG-RAN meeting #4
Miami, 17th – 19 th June, 1999

TSG RAN#4 (99)383

Agenda Item:

Source: **RAN WG4**

To: **TSG RAN**

Title: **Liaison statement on Impact of OHG harmonization recommendation on UTRA/FDD and UTRA/TDD**

Document for: **Discussion and Information**

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1 Introduction

At its meeting in Miami on 14th – 16th June, RAN WG4 commenced discussions about the implications of the OHG Recommendation on harmonisation of the two main CDMA-based proposals for IMT 2000 (UTRA and cdma2000) on its work. WG4 concluded that the change of chip rate proposed by OHG will have an impact on its specifications. WG4 has noted that work on reviewing the changes proposed by OHG has already started in WG1. In order to initiate similar progress in TSG-RAN WG4 without impacting the WG4 work plan (TSGR4#4(99)190, approved in WG4 #4 meeting at Stockholm) have been started.

In this liaison statement, WG4 identifies some of the key parameters of the current UTRA/FDD and UTRA/TDD specifications which need to be modified to implement the OHG recommendation. This liaison statement from RAN WG4 provides TSG RAN with the opinion of RAN WG4 on the impact of harmonisation, to assist TSG RAN in making a decision to endorse the change of the chip rate.

2 Procedure of WG4

In order to progress this issue in WG4, the following procedure is proposed:

- As the number of affected parameters are few in WG4, this LS to TSG-RAN includes information on both the current chip rate 4.096 Mcps and 3.84 Mcps wherever possible.
- If TSG-RAN decides to change the chip rate then the agreed parameters in the specifications will be modified by their editors before the next meeting of WG4.
- Some parameters like reference sensitivity will require further simulation. As soon as these are available they should be discussed in WG4 for incorporation in the WG4 specifications.

3 Effects of 3.84 Mcps on the FDD mode

3.1 Channel spacing

This items refers to TS25.101 (v1.2.0) section 5.4.1.

It is proposed that the chip rate change should not impact the current agreed channel spacing. Therefore the nominal channel spacing should still be maintained as 5 MHz , but can be adjusted to optimise performance in a particular deployment.

3.2 Roll-Off Factor

This item refers to TS25.101(v1.2.0) section 6.8.1 Pulse shaping and TS25.201(v2.0.0) 7.2.3 Modulation & spreading.

The current roll-off factor is derived from the channel spacing and chip rate. Although it is possible to change the roll-off factor it is felt the current roll-factor should be maintained in order to provide the flexibility in the allocation of channel spacing for inter operator and intra-operator spacing. Either the channels can be pushed closer together or left at the same frequency offset and

compatibility improved. It is felt this flexibility would be more useful in addressing the various deployment scenarios. Therefore the roll-off factor of 0.22 should be retained.

Maintaining the existing roll off factor will have a small impact on the transmitter performance in particular the ACLR value and a slightly larger impact on the receiver performance in terms of the ACS value. The impact on these parameters are reviewed in sections 3.3 and 3.4.

3.3 ACLR

Computer simulation have be performed on the impact of ACIR for both UL and DL with the new chip rate and are presented in Annex A. Simulations are also provided showing the impact of the change of chip rate from 4,096 to 3,84 Mchip/s and the change of roll-off factor.

From the results presented in figure 3 we can conclude that the ACLR value will be improved by 0,5 to 0,7 dB with new chip rate of 3,84 Mchip/s. Also can be seen that the roll-off factor change from 0,22 to 0,3 does not bring any significant impact to the performance of ACLR.

Hence it can be stated that from an implementation perspective and with new chip rate the ACLR performance can be improved <1dB compared to chip rate of 4.096Mcps.

3.4 ACS

The chip rate change will have a positive impact to receiver sensitivity performance. By keeping the 5 MHz channel spacing and roll-off 0,22 the simulated improvement of adjacent channel selectivity is in the range of 2 dB depending on actual filter response. If the roll-off is changed to 0,3 all this gain can not be utilized, and the performance would be unchanged. This result also supports retaining the current roll-off in order to achieve a higher ACS value to improve system performance.

Hence it can be stated that from an implementation perspective and with new chip rate the ACS performance can be improved 2 dB compared to chip rate of 4.096Mcps.

3.5 Reference Sensitivity

This item refers to TS25.101(v1.0.0) 7.3 Static reference sensitivity level, as well as TS25.104, the equivalent for BTS.

TSGR1#5(99)677 is proposing modification of the frame structure from 16 slots per frame to 15, keeping the frame length, slot structure, and number of chips per symbol constant, as well as changing the chip rate from 4.096Mcps to 3.84Mcps. In theory the chip rate change does not have any impact to reference sensitivity due the fact that both processing gain and noise BW will be affected by the same amount, and hence they cancel each others impacts. Changing frame structure may affect the required Eb/No of each service, and this requires computer simulation with new parameters. After finishing the computer simulation, specification of sensitivity should be fixed according to the same way as proposed in TSGR4#1(99)012 and TSGR4#4(99)204.

4 Effects of 3.84 Mcps on the TDD mode

Following the general philosophy of harmonisation between the FDD and TDD mode most changes mentioned in section 3 are also applicable to the TDD mode.

4.1 Channel spacing

Refer to section 3.1.

4.2 Roll-Off Factor

Refer to section 3.2

4.3 ACLR

Computer simulations to determine the ACLR requirements for the TDD mode are ongoing. However it is anticipated that the change in the chip rate will not lead to any significant change in the results (as already shown for the FDD mode). ACLR requirements for the TDD mode will be defined in the ongoing standardisation process off WG4.

4.4 ACS

Refer section 3.4, although the performance gains may not be numerically the same as stated in section 3.4.

4.5 Reference Sensitivity

Refer section 3.5.

Annex A

Figure 1 and figure 2 show the UL and DL capacity loss with respect to ACIR

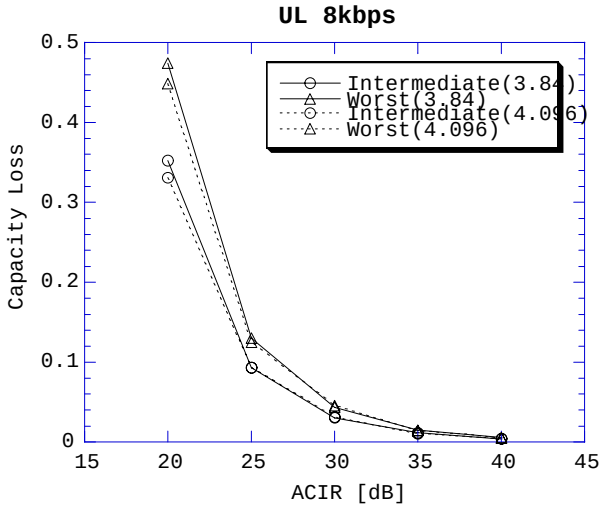

Fig. 1 Up-Link Capacity Loss with respect to ACIR

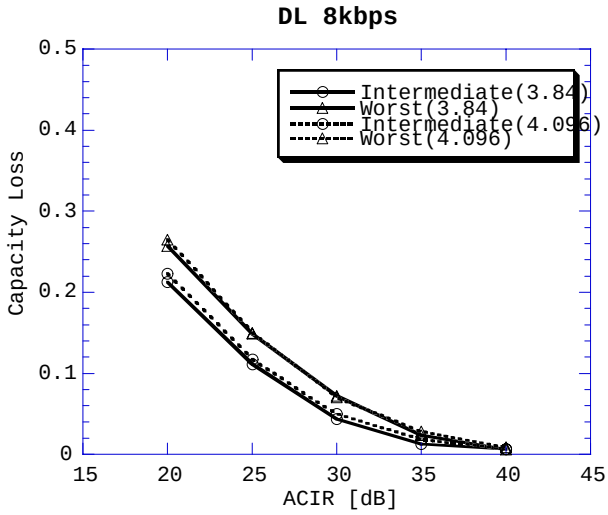

Fig. 2 Down-Link Capacity Loss with respect to ACIR

Figure 3 shows the impact of ACLR on the roll-off factor.

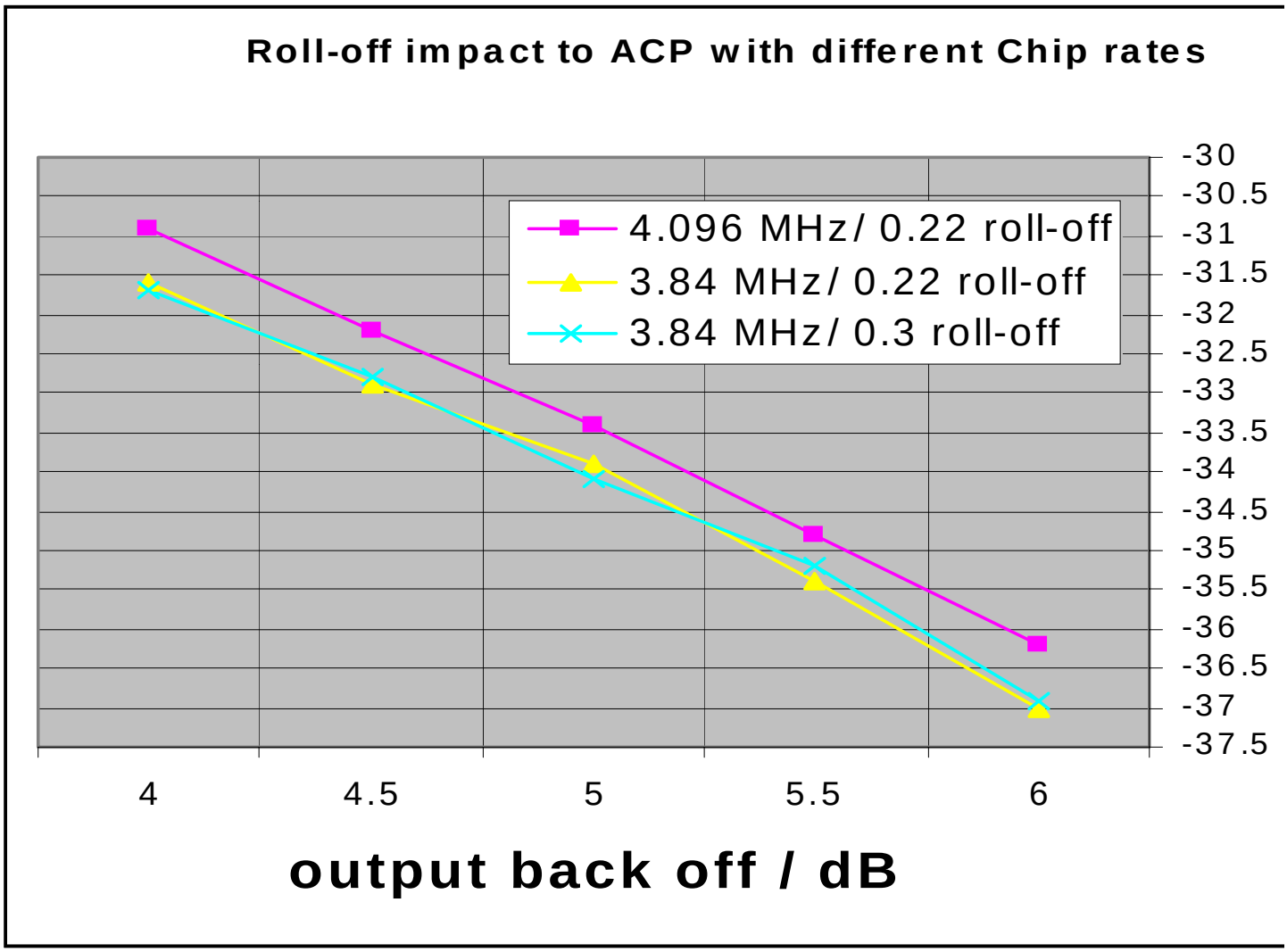

Fig. 3 Impact of chip rate change and different roll-off to ACLR

Table 1 and 2 are the parameters used in the UL and DL simulations.

Table 1 Up-Link Simulation Parameters

MCL	70 dB
BS antenna gain	11 dBi
MS antenna gain	0 dBi
Log normal shadowing	Standard Deviation of 10 dB
# of snapshot	3000
Handover threshold	3 dB
Noise figure of BS receiver	5 dB
Thermal noise (NF included)	-103.16 dBm@3.84MHz
Max TX power of MS	21 dBm
Power control dynamic range	65 dB
Cell radius	577 m (for both systems)
Inter-site distance	1000 m (for both systems)
BS offset between two systems (x, y)	Intermediate: (0.25 km, 0.14425 km) -> 0.289 km shift Worst: (0.5 km, 0.2885 km) -> 0.577 km shift
User bit rate	8 kbps
Activity	100%
Target Eb/I0	6.1 dB
ACIR	20, 25, 30, 35, 40 dB

Table 2 Down-Link Simulation Parameters

MCL	70 dB
BS antenna gain	11 dBi
MS antenna gain	0 dBi
Log normal shadowing	Standard Deviation of 10 dB
# of snapshot	3000
Handover threshold	3 dB
Noise figure of MS receiver	9 dB
Thermal noise (NF included)	-99.16 dBm@3.84MHz
Max TX power of BS	43 dBm (30 dBm for each traffic channel)
Power control dynamic range	25 dB
Cell radius	577 m (for both systems)
Inter-site distance	1000 m (for both systems)
BS offset between two systems (x, y)	Intermediate: (0.25 km, 0.14425 km) -> 0.289 km shift Worst: (0.5 km, 0.2885 km) -> 0.577 km shift
User bit rate	8 kbps
Activity	100%
Target Eb/I0	7.9 dB
ACIR	20, 25, 30, 35, 40 dB

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Source: **Alcatel, Ericsson, Lucent Technologies, Motorola, NEC, Nokia, Nortel Networks, Sien**

Title: **Analysis of the OHG proposal**

Document for: **Discussion**

Agenda Item:

Introduction

This document presents an initial analysis of the requirements that the Operators Harmonisation Group (OHG) proposal [1] would place on the 3GPP release 99 contents. It addresses the work to be performed in 3GPP in 99 to cover these requirements which would allow for the provision for connection of UTRA radio interface to ANSI41 networks, while allowing seamless handovers with a cdma2000 (Multi Carrier including 1xRTT) radio interface.

References

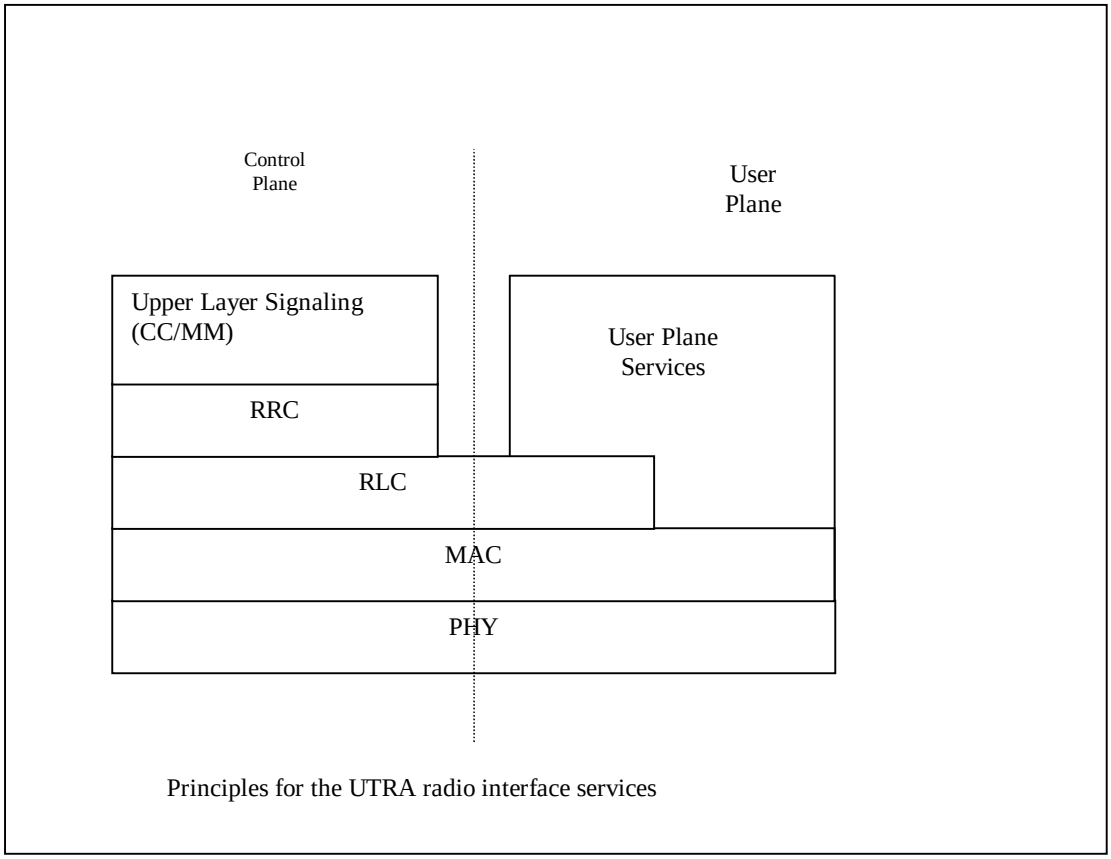
[1] RP-99358 Open Letter to Standard Organisations from OHG on Global 3G (G3G) CDMA standard.
[2] 3GPP TR 25.921 Guidelines and principles for protocol description and error Handling

Mapping of ANSI 41 onto UTRA radio interface

First we will address where the upper layers are expecting services from the UTRA stack, since it is where the mapping of ANSI41 onto UTRA will be performed:

- Upper layer signalling (MM, CC) is mapped on top of RRC, and uses its transport function for UE to network communication. This signalling is transparent to the UTRA stacks.
- The control of the services provided by the User plane of the UTRA stacks is provided via the generic SAPs on top of RRC. This is purely a model since these SAPs are local to the RNC and UE.
- The user plane services are mapped on top of the RLC layer (for Acknowledged Mode, Unacknowledged Mode, and Transparent Mode) or on top of MAC (when no RLC service is needed). Note that in model of RAN2, all services are on top of RLC, but RLC can be transparent..
- Concurrent user plane services can be flexibly multiplexed by MAC or Layer 1 multiplexing.

This leads to the following representation of the service mapping on the UTRA protocol stacks:



Principles for the UTRA radio interface services

This means that the following services will be used for cdma2000 services:

- The transport services provided by RRC to Upper layers
- The services provided directly on top of the MAC layer
- The services provided directly on top of the RLC layer

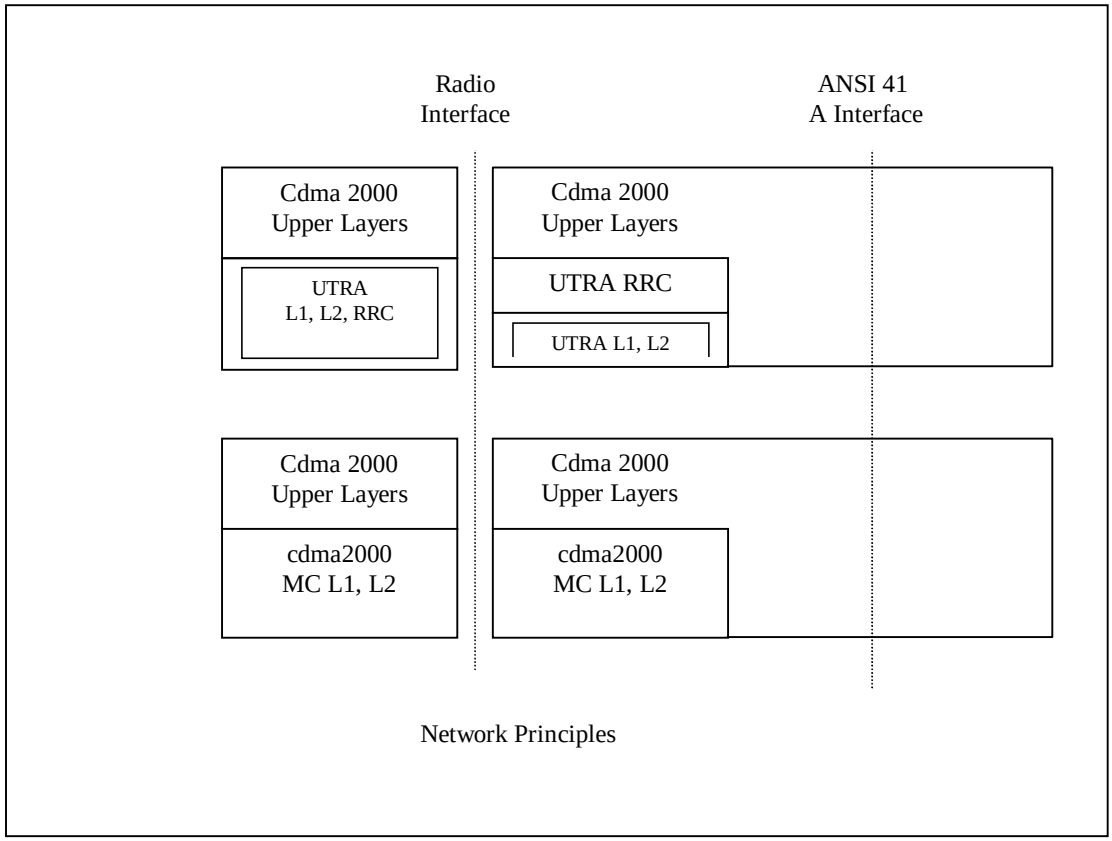
Handover aspects

Since the cdma2000 (MC including 1xRTT) to/from UMTS handover can be based on a hard handover procedure, protocol extensions of RRC should be sufficient. On the user plane level, a reset of the L1 and L2 will be necessary, similar to the case of inter-BSC handover in cdma2000. This means that Layer 2 protocols from cdma2000 and UMTS do not need to be aligned in how that provide the services, but only on which services they provide.

RRC protocol extensions will be necessary for the signalling of handover between cdma2000 and UTRA.

Architecture aspects

The following figure shows how UTRA radio protocol stacks are incorporated inside an ANSI41/cdma2000 architecture, according to the principles developed in [1].



The mapping of the cdma2000 on the radio interface is performed inside the Access Network (in fact, the node which is responsible for providing these UTRA radio interface services on the network side is the RNC). This is *within* the RAN, and therefore does not impact the Iu interface or other higher level entities in the network (like the Core Network).

On the UE side, the services used are only those of the Access Stratum (RRC and below), and are therefore also fully constrained in the RAN also.

Hooks and extensions

The OHG proposal [1] defines that hooks and extensions should be provided so that the services provided by the UTRA radio interface layers can later support the cdma2000 Upper Layer signalling and services.

Hooks and extension are only means by which a given protocol can be extended to supported new functions in future releases. The only true requirement in order to achieve backwards compatibility is to provide a good error handling mechanism is the UEs. This is already a pre-requisite in 3GPP alone, since this support is essential for a viable evolution of the system in future releases. Therefore, this is already a requirement of 3GPP release 99.

Nevertheless, in order to have a straightforward implementation of dual mode equipment, it is beneficial that these are straightforward extensions, rather then requiring some restructuring of the radio interface architecture. This will allow to later enhance the UTRA protocol stacks, rather than introducing specific changes. It is also important that these extensions are provided in a way which is backwards compatible, but as already stated extensibility is a basic property of the release 99 of 3GPP.

Based on the assumption that protocol extensions, like addition of new RRC messages, is a straightforward exercise for the UTRA protocols, work should focus on services provided to the Upper layers, both for the control plane but also the user plane. Still, what needs to be considered is not only whether ANSI41 can be supported by UTRA (for which the answer can be positive without much risks), but whether ANSI41 can be supported *efficiently*.

The following sections will look at the extensibility mechanisms which are in place in 3GPP today in order to understand what should be done in 3GPP for the release 99 in view of meeting the OHG recommendations.

Physical layer extensions

An analysis was performed within the work of the OHG on the services provided by the physical layer. This analysis did not identify services required by cdma2000 which would be missing from WCDMA L1.

The impacts on the physical layer should therefore be limited to the following two categories:

- Already identified harmonisation of physical layer, as proposed in [1]
- Later changes that would be the consequence of the need to support new transport channels to map *efficiently* some cdma2000 services.

The current list of Transport Channels supported in 3GPP is very wide, providing capabilities from low bit rate to high bit rates requirements, as well as an efficient support for bursty to continuous traffic profiles. Therefore it may be enough for the mapping of cdma2000 services.

Nevertheless, whenever necessary, new transport channels can easily be added in later releases of the standard and overlayed at the physical layer on already defined channels.

RRC, RLC and MAC layer extensions

All layers can be extended in a straightforward manner based on the preliminary principles already defined in [2]. In fact, RRC allows also to negotiate RLC and MAC protocol capabilities (or versions), so that extensions can always be added.

RRC messages can be easily added or existing messages can be extended. Also, RRC allows to transport efficiently Upper layer messages in an efficient way irrespective of their size. In fact, GSM/GPRS has a variety of DTAP signalling messages, from relatively small MM messages, up to SMS or even USSD which can be relatively big.

No restriction is expected on the extensibility of RRC, RLC and MAC after release 99. Also, extensibility is from the beginning a crucial requirement because further releases are envisioned (with some items already known are being in later release only).

Identification of global functional architecture

In order to ensure that the extensions which would be added on the existing protocol do not imply a res of the protocol architecture, the global functional architecture should be defined in 99.

Conclusion

Based on the preliminary analysis explained in this contribution, it appears that extensions to the UTRA radio protocol stacks as requested in [1] can be performed in future releases in a similar manner to what has already been planned for 3GPP evolution.

Regarding the extension capabilities of UTRA protocols, it has been shown that this is already a baseline requirement for the 3GPP release 99, and therefore does not represent extra work based on the OHG proposal.

Since the radio interface has been tailored for multimedia support, it provide a great flexibility in the services that is provides. Also, its architecture has been modelled so as to allow for gradual extensions in a straight forward way (as proven recently in the way that the CPCH concept could be incorporated in a simple manner).

As a consequence, it is expected that the impacts on 3GPP release 99 can be limited to the following:

- Harmonisation of the physical layer parameters (pilot structure and chip rate), for which concrete proposals were already made in WG1 and WG4.
- Identification of the services provided by the UTRA MAC, RLC and RRC layers which would be missing and would need to be added later.

These impacts are not expected to influence the current time plan in 3GPP for release 99.

It has also been shown that the necessary work is limited to the UTRA radio interface specifications. There should be no implications on the bearers and services provided by UTRAN. Therefore no impact is expected on the work of TSG-SA and TSG-CN.