3GPP TSG-RAN WG4 Meeting # 101-bis-e Revision of R4-2201919

Electronic Meeting, January 17-25, 2022

**Agenda item:** 6.1.3.3

**Source:** Keysight Technologies

**Title:** Pass/Fail Limits for FR1 Channel Model Validation

**Document for:** Approval

# Introduction

Original excess delay values of OTA channel models in [1] are specified in accuracy of two decimals in nano second units, i.e., in 10 pico second accuracy. Such high delay accuracy in validation measurement would require a test system with bandwidth of approximately 100 GHz. It is evident that the excess delay precision of the original channel model cannot be achieved in PDP validation. The purpose of this document is to specify power and excess delay target values for the PDP validation measurement. Moreover, the procedure of determining those values is described.

Additionally, remaining channel model validation limits will be proposed in a revision of this contribution.

# Discussion (PDP)

The procedure to determine target power and excess delay values is defined as follow.

1. Take the original discrete reference PDP that results from angularly filtering the tabulated CDL model with the specified gNB beam. Let us denote this PDP . (This is plotted with black dots in Figure 1.)
2. Quantize the original 0.01 ns resolution excess delay values to 5 ns grid by rounding to the nearest value, i.e., multiples of 5 ns. The resulting PDP is .
3. Filter the PDP to 200 MHz BW by taking Fourier transformation, weighting the frequency domain function by the Hanning window function , and by inverse transforming the product back to delay domain. Power values of the filtered PDP are normalized such that the maximum becomes 0 dB. The resulting filtered (band limited) PDP is . (This is the red curve in Figure 1.)
4. Select a few peak values of the filtered PDP to specify the discrete target PDP . (This is plotted with green triangles in Figure 1.)

The above process for filtering the PDP and choosing the power and delay samples is illustrated in Figure 1 for UMa beam 1 @2450 MHz. Beam 2 and the corresponding 3600 MHz PDPs are shown in Figures 3 - 5. PDP filtering without 5 ns delay quantization is shown for comparison in Figure 2, where filtered PDPs is illustrated with and without delay quantization. The one without step 2, i.e., with the original non-quantized delays, is the purple curve. Also, the quantized delays are shown by green circles. We can observe the impact of step 2 by comparing the red and purple curves. The red PDP has a better match with the original discrete PDP. Moreover, “tails” of the red curve are clearly smaller, and the power drops rapidly in the delay bins without original model taps. The grid of 5 ns is inherent to 200 MHz BW, hence quantization to it prevents inaccuracies on tap powers split to two adjacent delay bins. For example, the mismatch in the measurement delay sample grid for the non-quantized delays can be observed to introduce approximately 2 dB inaccuracy for the tap at 480 ns.



Figure 1. The original, the filtered, and the target PDP of UMa CDL-C model with beam 1 at 2450 MHz.



Figure 2. Original, quantized delay, and two filtered, and a measured PDP of UMa CDL-C model with beam 1 at 2450 MHz.

The proposed target powers and excess delay values for PDP validation model are shown in Table 1 for UMa and in Table 2 for the UMi model (which will be updated in a revision of this contribution).

Table 1. Target power and excess delay values for PDP validation for UMa model

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | CDL-C beam 1 (2450 MHz) | | CDL-C beam 2 (2450 MHz) | | CDL-C beam 1  (3600 MHz) | | CDL-C beam 2  (3600 MHz) | |
| Value number | Delay [ns] | Power [dB] | Delay [ns] | Power [dB] | Delay [ns] | Power [dB] | Delay [ns] | Power [dB] |
| 1 | [0] | [-32.4] | [0] | [-26] | [0] | [-32.4] | [0] | [-25.9] |
| 2 | [80] | [-18.1] | [75] | [0.0] | [80] | [-17.9] | [75] | [0.0] |
| 3 | [230] | [0.0] | [85] | [-2.6] | [230] | [0.0] | [85] | [-2.5] |
| 4 | [240] | [-2.7] | [235] | [-17.2] | [240] | [-2.8] | [235] | [-17.1] |
| 5 | [290] | [-31.8] | [290] | [-26.2] | [290] | [-32.9] | [290] | [-27.2] |
| 6 | [300] | [-39.7] | [450] | [-26] | [300] | N/A (Note 1) | [450] | [-26.2] |
| 7 | [450] | [-33.9] | [480] | [-26.1] | [450] | [-34] | [480] | [-26.9] |
| 8 | [480] | [-32.1] | [1680] | [-39.3] | [480] | [-32.9] | [1680] | N/A  (Note 1) |
| Note 1: Power value is below the -40 dB limit | | | | | | | | |

Table 2. Target power and excess delay values for PDP validation for UMi model

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | CDL-C beam 1 (2450 MHz) | | CDL-C beam 1 (3600 MHz) | |
| Value number | Delay [ns] | Power [dB] | Delay [ns] | Power [dB] |
| 1 | [0] | [-30.7] | [0] | [-30.7] |
| 2 | [20] | [-19.5 | [20] | [-19.5] |
| 3 | [65] | [0] | [65] | [0] |
| 4 | [80] | [-33] | [80] | [-33.1] |
| 5 | [130] | [-32.1] | [130] | [-32.1] |
| 6 | [215] | [-40.8] | [215] | [-41] |
| 7 | [460] | [-41.5] | [460] | [-41.6] |



Figure 3. The original, the filtered, and the target PDP of UMa CDL-C model with beam 2 at 2450 MHz.



Figure 4. The original, the filtered, and the target PDP of UMa CDL-C model with beam 1 at 3600 MHz.



Figure 5. The original, the filtered, and the target PDP of UMa CDL-C model with beam 2 at 3600 MHz.



Figure 6. The original, the filtered, and the target PDP of UMi CDL-C model with beam 1 at 2450 MHz.



Figure 7. The original, the filtered, and the target PDP of UMi CDL-C model with beam 1 at 3600 MHz.

Proposal 1: Adopt the 200 MHz filter with Hanning window for 5 ns quantized reference PDP for generating the filtered reference PDP data as described in this paper.

Proposal 2: Adopt the delay and power sample values for UMa and UMi models according to Tables 1 and 2 as reference data for PDP validation measurement.

# PASS/FAIL Limits for PDP

If the **Proposal 1** is adopted, it is possible to set much tighter pass/fail limits compared to the case if not adopted. For paths 0 to 20 dB below the peak, use power tolerance of +/- 0.85 dB and for paths 20 to 40 dB below the peak, use +/- 2 dB power tolerance.

**Proposal 3: Adopt the pass/fail limit +/- 0.85 dB for PDP paths 0 to 20 dB below the peak.**

**Proposal 4: Adopt the pass/fail limit +/- 2 dB for PDP paths 20 to 40 dB below the peak.**

# Conclusion

The following observations and proposals were made in this contribution

**Proposal 1: Adopt the 200 MHz filter with Hanning window for 5 ns quantized reference PDP for generating the filtered reference PDP data as described in this paper.**

**Proposal 2: Adopt the delay and power sample values for UMa and UMi models according to Tables 1 and 2 as reference data for PDP validation measurement.**

**Proposal 3: Adopt the pass/fail limit +/- 0.85 dB for PDP paths 0 to 20 dB below the peak.**

**Proposal 4: Adopt the pass/fail limit +/- 2 dB for PDP paths 20 to 40 dB below the peak.**

# References

1. TR 38.827, Study on radiated metrics and test methodology for the verification of multi-antenna reception performance of NR User Equipment (UE), V16.4.0 (2021-09)