Source:	**Editor for S25.101 UE Radio transmission and reception (FDD)**
Title:	**AH05 report**
Document for	**Discussion and decision**

1 Document status

The current approved version S25.101v2.1.0 was sent to the WG4 reflector on the 30/06/99. This version include all the changes to document (ver 2.0.0) submitted to the RAN#4 meeting in Miami plus the harmonization changes agreed in the RAN meeting. The RAN decision allowed the editors to make the necessary changes which have been released as ver 2.1.0. The changes made from ver 2.0.0 to ver 2.1.0 by the editor are summarized below for information.

New Clause Nos.	Editorial / Technical	Comment
Title	E	Version status updated to S25.101v2.1.0
2	E	Added reference to ITU-R Recommendations SM.329 and S25.213 (Gain factor)
3.1	E	Added row called 'Average power' – Definition need
3.3 5.1 6.6.1	T	Change 4.096 Mcps to 3.84 Mcps
6.4.4.1 6.5.1 6.6.2.2.1 6.7.1	T	Where the minimum requirement is specified in terms of a power and 4.096 MHz bandwidth, the bandwidth term has been removed and the following text is added. - "measured with a filter that has a Root-Raised Cosine (RRC) filter response with a roll off $\alpha = 0.22$ and a bandwidth equal to the chip rate. This was agreed in WG4 but had not been included in ver 2.0.0 due to limited time available to present the document to the RAN#4 meeting
6.6.2.2.1	T	ACLR value has be increased by 1 dB as per WG4 agreement pending RAN#4 approval
6.8.1	T	Chip duration specified (0.26042 uS) to take account of 3.84 chip rate.
6.8.2	E	Table 9 deleted and minimum requirement is now specified as text. Note table 6 to 9 have been re-assigned in this revision.
7 (All parts)	T	All measurement test parameters which specified a 4.096 MHz bandwidth has been replaced with 3.84 MHz
7.5.1	T	ACS value has been increased by 1 dB as per WG4 agreement pending RAN#4 approval. The following test parameters have been proposed for table 13b to account for the new value • PCCPCH_Ec/Ior = -0.46dB , • DPCH_Ec/Ior = -10dB, • Ior = -93dBm , • Ioac = -52dBm
7.6.1	T/E	Typo error for in Table 15 corrected for blocking offset for Band 2 changed to 2255< f < 12750 previously it was 2225<f<12750
8 (All parts)	T	All measurement test parameters which specified a 4.096 MHz bandwidth has been replaced with 3.84 MHz
Annex D	E	Two further open items added on definition of average power and Tx-Rx frequency separation
Annex E	T	UE capabilities – chip rate changed to 3.84 Mcps
History	E	Revision change indicated.

2   Input to S25.101v 2.1.0

The following comments have been sent either to the reflector or directly to the editor for inclusion in the next version release. These changes have been proposed from the continuing harmonization discussion in WG1 and further discussion in other AH groups in WG4. These changes are submitted to WG4 for discussion/decision.

New Clause Nos.	Editorial / Technical	Comment
6.4.2.1.1	T	0.625 ms should be changed to 0.667 ms to account for 15 slots
6.4.5	T	1.6 KHz should be changed to 1.5 KHz to account for 15 slots
6.5.3.1	T	Figure 2a and 2B , 625 us should be changed to 667 us to reflect change to 15 slots
6.7.1	T	This item was listed as an open item to resolve the compatibility between the agreed ACLR values and the current IM value in the specification. The current specification for Tx IM of –35 dBc is not in line with the agreed ALCR agreement of –33 dBc. It is proposed this value is changed to –31 dBc. This proposal is to ensure the Tx IM measurement is not masked by the contribution of the ACLR. Based on an ACLR specification of -33 dBc the implementation value for the Tx IM will need to be –35 dBc to ensure a measured value of –31 dBc for the Tx IM is achieved.
B2.2	T	Changes to choice of multi-path fading propagation conditions as per AH01 report . < Note the delays in the propagation condition need to be modified to reflect the change in chip period >
Annex D		The following additions to the list of open items are proposed 1. Closed loop power control; SIR tolerance and dynamic range 2. Peak code domain error is outstanding 3. Chapter 8 – Performance requirements