3GPP TSG-RAN WG1 #19 ***Tdoc R1-01-0375***
USA, Las Vegas, 27 Feb – 02 Mar 2001

CR-Form-v3

CHANGE REQUEST

✍ **25.225** **CR** **24** ✍ rev **1** ✍ Current version: **3.5.0** ✍

*For **HELP** on using this form, see bottom of this page or look at the pop-up text over the ✍ symbols.*

Proposed change affects: ✍ (U)SIM ☐ ME/UE **X** Radio Access Network **X** Core Network ☐

Title: ✍	Inclusion of 1.28Mcps TDD in TS 25.225	
Source: ✍	Siemens, CWTS, CATT	
Work item code: ✍	LCRTDD	***Date:*** ✍ 28.02.2001
Category: ✍	**B**	***Release:*** ✍ REL-4

Use one of the following categories:
F *(essential correction)*
A *(corresponds to a correction in an earlier release)*
B *(Addition of feature),*
C *(Functional modification of feature)*
D *(Editorial modification)*
Detailed explanations of the above categories can be found in 3GPP TR 21.900.

Use one of the following releases:

2	*(GSM Phase 2)*
R96	*(Release 1996)*
R97	*(Release 1997)*
R98	*(Release 1998)*
R99	*(Release 1999)*
REL-4	*(Release 4)*
REL-5	*(Release 5)*

Reason for change: ✍	Inclusion of 1.28 Mcps TDD
Summary of change: ✍	?? The basis for this document was CR024, R1-01-0185 ?? in revision 1, the approved contributions from WG1#19 have been included
Consequences if not approved: ✍	

Clauses affected: ✍	**5.2.8 (section name revised),** **New section:** 5.1.14 Timing Advance (T_{ADV}) for 1.28 Mcps TDD **New section:** 5.2.10 Received SYNC-UL Timing Deviation for 1.28 Mcps TDD		
Other specs affected: ✍	**X** Other core specifications ☐ Test specifications ☐ O&M Specifications	✍	25.221, 25.222, 25.223, 25.224
Other comments: ✍			

How to create CRs using this form:
Comprehensive information and tips about how to create CRs can be found at: http://www.3gpp.org/3G_Specs/CRs.htm. Below is a brief summary:

1) Fill out the above form. The symbols above marked ✍ contain pop-up help information about the field that they are closest to.
2) Obtain the latest version for the release of the specification to which the change is proposed. Use the MS Word "revision marks" feature (also known as "track changes") when making the changes. All 3GPP specifications can be downloaded from the 3GPP server under ftp://www.3gpp.org/specs/ For the latest version, look for the directory name with the latest date e.g. 2000-09 contains the specifications resulting from the September 2000 TSG meetings.
3) With "track changes" disabled, paste the entire CR form (use CTRL-A to select it) into the specification just in front of the clause containing the first piece of changed text. Delete those parts of the specification which are not relevant to the change request.

5.1.14 Timing Advance (T_{ADV}) for 1.28 Mcps TDD

Definition	The 'timing advance (T_{ADV})' is the time difference $T_{ADV} = T_{RX} - T_{TX}$ Where T_{RX}: calculated beginning time of a certain uplink time slot with the UE timing according to the reception of a certain downlink time slot (for the timing it is assumed that the time slots within a sub-frame are scheduled like given in the frame structure described in 25.221 chapter 6.1) T_{TX}: time of the beginning of the same uplink time slot by the UE (for the timing it is assumed that the time slots within a sub-frame are scheduled like given in the frame structure described in 25.221 chapter 6.1)

Note: This measurement can be used for uplink synchronisation or location services.

5.2.8 RX Timing Deviation (for the 3.84 Mcps option)

Definition	'RX Timing Deviation' is the time difference $T_{RXdev} = T_{TS} - T_{RXpath}$ in chips, with T_{RXpath}: time of the reception in the Node B of the first detected uplink path (in time) to be used in the detection process. The reference point for T_{RXpath} shall be the Rx antenna connector. T_{TS}: time of the beginning of the respective slot according to the Node B internal timing

NOTE: This measurement can be used for timing advance calculation or location services.

5.2.10 Received SYNC-UL Timing Deviation for 1.28 Mcps TDD

Definition	'Received SYNC-UL Timing Deviation' is the time difference $UpPCH_{POS} = UpPTS_{Rxpath} - UpPTS_{TS}$ Where $UpPTS_{Rxpath}$: time of the reception in the Node B of the SYNC-UL to be used in the uplink synchronization process $UpPTS_{TS}$: time instance two symbols prior to the end of the DwPCH according to the Node B internal timing UE can calculate Round Trip Time (RTT) towards the UTRAN after the reception of the FPACH containing $UpPCH_{POS}$ transmitted from the UTRAN. Round Trip Time RTT is defined by $RTT = UpPCH_{AVD} + UpPCH_{POS} - 8*16\ T_C$ Where $UpPCH_{ADV}$: the amount of time by which the transmission of UpPCH is advanced in time relative to the end of the guard period according to the UE Rx timing.

Annex A (informative): Monitoring GSM from TDD: Calculation Results

A.1 Low data rate traffic using 1 uplink and 1 downlink slot (for the 3.84 Mcps option)

A.2 Low data rate traffic using 1 uplink and 1 downlink slot (for the 1.28 Mcps option)

NOTE: The section evaluates the time to acquire the FCCH if all idle slots are devoted to the tracking of a FCCH burst, meaning that no power measurements is done concurrently. The derived figures are better than those for GSM. The section does not derive though any conclusion. A conclusion may be that the use of the idle slots is a valid option. An altemative conclusion may be that this is the only mode to be used, removing hence the use of the slotted frames for low data traffic or the need for a dual receiver, if we were to considering the monitoring of GSM cells only, rather than GSM, TDD and FDD.

If a single synthesiser UE uses only one uplink and one downlink slot, e.g. for speech communication, the UE is not in transmit or receive state during 5 slots in each frame. According to the timeslot numbers allocated to the traffic, this period can be split into two continuous idle intervals A and B as shown in the figure below.

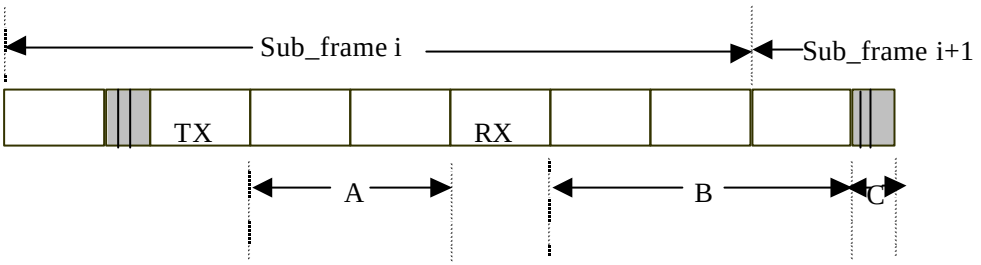

Figure A.2: Possible idle periods in a subframe with two occupied timeslots

A is defined as the number of idle slots between the Tx and Rx slots and B the number of idle slots between the Rx and Tx slots. It is clear that A+B=5 time slots and C is equal to the DwPTS+GP+UpPTS.

In the scope of low cost terminals, a [0.5] ms period is supposed to be required to perform a frequency jump from 1.28Mcps TDD to GSM and vice versa. This lets possibly two free periods of A*Timeslots-1 ms and B*Timeslots+C-1 ms during which the mobile station can monitor GSM, Timeslots being the slot period.

Following table evaluates the average synchronisation time and maximum synchronisation time, where the announced synchronisation time corresponds to the time needed to find the FCCH. The FCCH is supposed to be perfectly detected which means that it is entirely present in the monitoring window. The FCCH being found the SCH location is unambiguously known from that point. All the 5 idle slots and the DwPTS+GP+UpPTS are assumed to be devoted to FCCH tracking and the UL traffic is supposed to occupy the time slot 1.

Table A.2: example- of average and maximum synchronisation time with two busy timeslots per frame and with 0.5 ms switching time

Downlink time slot number	Number of free Timeslots in A	Number of free Timeslots in B	Average synchronisation time (ms)	Maximum synchronisation time (ms)
0	5	0	83	231
2	0	5	75	186
3	1	4	98	232
4	2	3	185	558
5	3	2	288	656
6	4	1	110	371

(*) All simulations have been performed with a random initial delay between GSM frames and 1.28Mcps TDD sub-frames.

Each configuration of Timeslots allocation described above allows a monitoring period sufficient to acquire synchronisation.

NOTE: Considering about the frame structure of 1.28Mcps TDD, there are total 7 timeslot in each sub-frame that can be used as data traffic. If more than 1 uplink and/or 1 downlink TDD timeslot are used for data traffic, that means it will occupy at least 3 time slot, equal to 0.675*3=2.205ms. And more time slots for traffic data means more switching point are needed to switch between the GSM and the 1.28Mcps TDD. As it was mentioned above, each switching will take 0.5ms. As a result, the idle time left for monitoring the GSM will be very little. So monitoring GSM from 1.28Mcps TDD under this situation will be considered in the future. It will need more carefully calculation and simulation.

A.2.1 Higher data rate traffic using more than 1 uplink and/or 1 downlink TDD timeslot (for 1.28Mcps TDD)

The minimum idle time to detect a complete FCCH burst for all possible alignments between the GSM and the 1.28Mcps TDD frame structure (called 'guaranteed FCCH detection'), assuming that monitoring happens every sub-frame, can be calculated as follows (t_{FCCH} = one GSM slot):

$$t_{\min\ ,\ guaranteed} = 2 \cdot t_{synth} + t_{FCCH} + \frac{5\,\text{ms}}{13} = 2 \cdot t_{synth} + \frac{25\,\text{ms}}{26}$$

- (e.g for t_{synth} =0ms: 2 1.28Mcps TDD **consecutive** idle timeslots needed, for t_{synth} =0.3ms: 3 slots (or 2 slots and the DwPTS+GP+UpPTS), for t_{synth} =0.5ms: 3 slots, for t_{synth} =0.8ms: 4 slots). Under this conditions the FCCH detection time can never exceed the time of 660ms.
- (For a more general consideration t_{synth} may be considered as a sum of all delays before starting monitoring is possible).
- For detecting SCH instead of FCCH (for a parallel search) the same equation applies.
- In the equation before the dual synthesiser UE is included if the synthesiser switching time is 0ms.

Table A.2.1 : FCCH detection time for a single synthesizer UE monitoring GSM from 1.28Mcps TDD every sub-frame

Occupied Slots	Cases	**AVERAGE** FCCH detection time in ms	**MAXIMUM** FCCH detection time in ms
2	21	136.625	660.785
3	35	188.451	660.785
4	35	231.115	660.785
5	21	-	-
6	7	-	-
7	1	-	-

The result in the above table is based on the following assumption:

?? A single synthesizer is used.

?? A [0.5] ms period is supposed to be required to perform a frequency jump from 1.28Mcps TDD to GSM and vice versa.

?? For a given number of occupied slots in the TDD mode all possible cases of distributions of these occupied TDD slots are considered (see 'cases'). For every case arbitrary alignments of the TDD and the GSM frame structure are taken into account for calculating the average FCCH detection time (only these cases are used which guarantee FCCH detection for all alignments; only the non-parallel FCCH search is reflected by the detection times in the above table).

The term 'occupied slots' means that the UE is not able to monitor in these TDD slots.

For a synthesiser switching time of one or one half TDD timeslot the number of needed consecutive idle TDD timeslots is summarized in the table below:

Table A.2.2 : Link between the synthesiser performance and the number of free consecutive Timeslots for guaranteed FCCH detection, needed for GSM monitoring

One-way switching time for the synthesiser	Number of free consecutive 1.28Mcps TDD timeslots needed in the sub-frame for a guaranteed FCCH detection
1 Timeslot (=864 chips)	4
0.5 Timeslot (=432 chips)	3
0 (dual synthesiser)	2