Agenda item:	**AdHoc #24 HSDPA**
Source:	**Motorola**
Title:	**Physical Layer Structure for HSDPA – Text Proposal for Section 6.1**
Document for:	**Approval**

Introduction: In this contribution, description of S-A-W protocol is added to Section 5.2.

5.2 Hybrid ARQ (H-ARQ)

H-ARQ is an implicit link adaptation technique. Whereas, in AMC explicit C/I measurements or similar measurements are used to set the modulation and coding format, in H-ARQ, link layer acknowledgements are used for re-transmission decisions. There are many schemes for implementing H-ARQ - Chase combining, Rate compatible Punctured Turbo codes and Incremental Redundancy. Incremental redundancy or H-ARQ-type-II is another implementation of the H-ARQ technique wherein instead of sending simple repeats of the entire coded packet, additional redundant information is incrementally transmitted if the decoding fails on the first attempt.

H-ARQ-type-III also belongs to the class of incremental redundancy ARQ schemes. However, with H-ARQ-type-III, each retransmission is self-decodable which is not the case with H-ARQ-type II. Chase combining (also called H-ARQ-type-III with one redundancy version) involves the retransmission by the transmitter of the same coded data packet. The decoder at the receiver combines these multiple copies of the transmitted packet weighted by the received SNR. Diversity (time) gain is thus obtained. In the H-ARQ-type-III with multiple redundancy version different puncture bits are used in each retransmission.

AMC by itself does provide some flexibility to choose an appropriate MCS for the channel conditions based on measurements either based on UE measurement reports or network determined. However, an accurate measurement is required and there is an effect of delay. Also, an ARQ mechanism is still required. H-ARQ autonomously adapts to the instantaneous channel conditions and is insensitive to the measurement error and delay. Combining AMC with H-ARQ leads to the best of both worlds - AMC provides the coarse data rate selection, while H-ARQ provides for fine data rate adjustment based on channel conditions.

The choice of H-ARQ mechanism however is important. Window based Selective Repeat (SR) is a common type of ARQ protocol employed by many systems including RLC R99. SR is generally insensitive to delay and has the favorable property of repeating only those blocks that have been received in error. To accomplish this feat, the SR ARQ transmitter must employ a sequence number to identify each block it sends. SR may fully utilize the available channel capacity by ensuring that the maximum block sequence number (MBSN) exceeds the number of blocks transmitted in one round trip feedback delay. The greater the feedback delay the larger the maximum sequence number must be. However, when Hybrid ARQ is partnered with SR, several difficulties are seen.

?? *UE memory requirements are high*. The mobile must store soft samples for each transmission of a block. MSBN blocks may be in transit at any time. A large MBSN requires significant storage in the UE adding to the unit's cost.

?? *Hybrid ARQ requires the receiver to reliably determine the sequence number of each transmission.* Unlike conventional ARQ, every block is used even if there is an error in the data. In addition, the sequence information must be very reliable to overcome whatever channel conditions have induced errors in the data. Typically a separate, strong code must be used to encode the sequence information, effectively multiplying the bandwidth required for signaling

Stop-and-wait is one of the simplest forms of ARQ requiring very little overhead. In stop-and-wait, the transmitter operates on the current block until the block has been received successfully. Protocol correctness is ensured with a simple one-bit sequence number that identifies the current or the next block. As a result, the control overhead is minimal. Acknowledgement overhead is also minimal, as the indication of a successful/unsuccessful decoding (using ACK, NACK, etc) may be signaled concisely with a single bit. Furthermore, because only a single block is in transit at a time, memory requirements at the UE are also minimized. Therefore, HARQ using a stop-and-wait mechanism offers significant improvements by reducing the overall bandwidth required for signaling and the UE memory. However, one major drawback exists: acknowledgements are not instantaneous and therefore after every transmission, the transmitter must wait to receive the acknowledgement prior to transmitting the next block. This is a well-known problem with stop-and-wait ARQ. In the interim, the channel remains idle and system capacity goes wasted. In a slotted system, the feedback delay will waste at least half the system capacity while the transmitter is waiting for acknowledgments. As a result, at least every other timeslot must go idle even on an error free channel. *N* channel stop-and-wait Hybrid ARQ offers a solution by parallelizing the stop-and-wait protocol and in effect running a separate instantiation of the Hybrid ARQ protocol when the channel is idle. As a result no system capacity goes wasted since one instance of the algorithm communicates a data block on the forward link at the same time that the other communicates an acknowledgment on the reverse link.