TSG-RAN Working Group 1 meeting #17
November 21-24, Stockholm, Sweden

TSGR1-00-1464

Agenda Item: 7

Source: Nokia

Title: Text proposal for HARQ complexity evaluation in HSDPA TR

Document for: Approval

1 Introduction

This document proposes HARQ complexity evaluation content for the RAN WG1 HSDPA technical report TR25.848. The contribution concentrates on N-channel stop-and-wait H-ARQ scheme. However, section 7.2.2 is structured such that it is clear that evaluations of other H-ARQ schemes may be added later.

2 Text proposal to TR 25.848

7 Evaluation of Technologies

7.1 Adaptive Modulation and Coding (AMC)

7.1.1 Performance Evaluation <throughput, delay>

7.1.2 Complexity Evaluation <UE and RNS impacts>

7.2 Hybrid ARQ (H-ARQ)

7.2.1 Performance Evaluation <throughput, delay>

7.2.2 Complexity Evaluation <UE and RNS impacts>

7.2.2.1 N-channel stop-and-wait H-ARQ

7.2.2.1.1 Introduction

The complexity of H-ARQ mechanisms when employed for link adaptation in HSDPA transmission depends on the H-ARQ scheme selected as well as on where the retransmission functionality is located in the UTRAN. Dual-channel stop-and-wait (SAW) protocol has been proposed as the retransmission functionality for HDSPA. A complexity evaluation on SAW H-ARQ is presented in this section. In this complexity evaluation it is further assumed that H-ARQ retransmission protocol operates in Node B.

7.2.2.1.2 Buffering complexity

The principle of hybrid ARQ is to buffer HSDPA TTIs that were not received correctly and consequently combine the buffered data with retransmissions. The actual method of doing soft combining depends on the H-ARQ combining scheme selected. In Chase combining scheme the receiver always combines the full retransmission of the failed HSDPA TTI, i.e. the amount of data in the receiver buffer remains the same. In the incremental redundancy schemes the receiver buffers coded symbols, which introduce new information to the HSDPA TTI transmitted first, i.e. the amount of data to be buffered increases with consecutive retransmissions. However, probably in practice the buffer in the receiver needs to be dimensioned considering the maximum size of the HSDPA TTI after all the incremental redundancy has been introduced. Regardless of the H-ARQ combining scheme soft combining is done on L1 before the decoding stage of FEC. Prior to decoding these symbols are soft-valued, i.e. each symbol is represented by two or more bits.

Regardless of the location of retransmission functionality in the RNS the number of symbols to be buffered in L1 receiver can be estimated generally as follows:

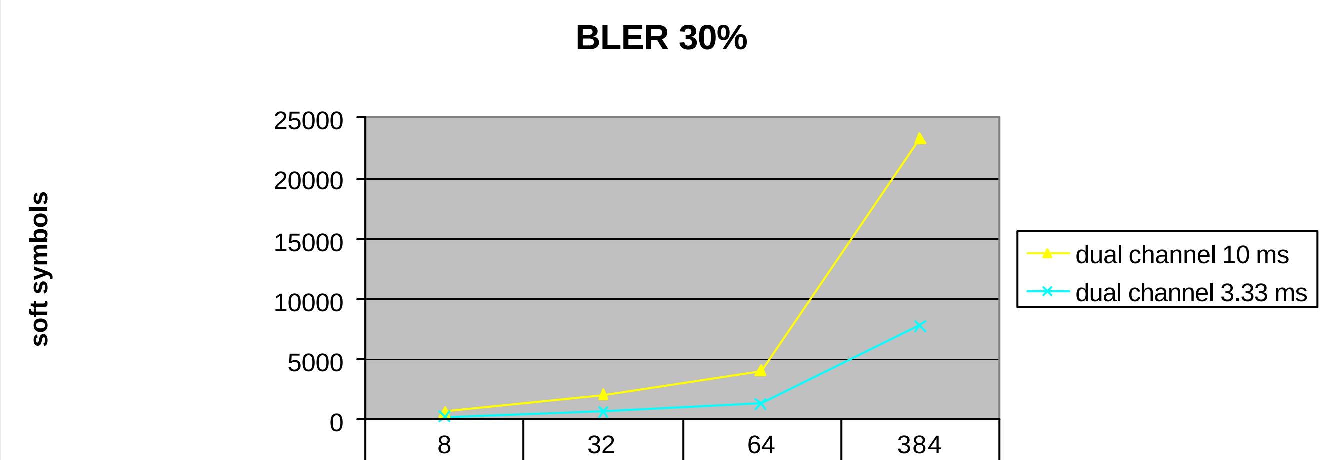
$$buffer \;?\; ?coded\ bits_{PDU} \;?\; failed\ PDUs\, in\, TTI \;?\; (latency_{retransmit} \;?\; latency_{NACK})?$$

where it is assumed for the sake of clarity that an integer number of PDUs fit into one HSDPA TTI. The latencies are also considered as multiples of a HSDPA TTI. For dual channel stop-and-wait H-ARQ the buffer size estimation is considerably simplified since no new PDUs are transmitted on a subchannel before the previous packet is acknowledged. The receiver has to buffer one HSDPA TTI from both subchannels. The next transmission is either a new packet or a retransmission of an erroneous packet. In either case, the maximum buffering need is two HSDPA TTIs. The actual size of the buffer needed for each HSDPA TTI depends on the H-ARQ combining scheme as described above. The receiver buffering complexity estimate can be easily extended to *n*-channel stop-and-wait protocol, where at maximum *n* HSDPA TTIs would be buffered at any given time. Thus, for *n*-channel stop-and-wait ARQ the L1 buffering can be expressed as:

$$buffer \;?\; ?coded\ bits_{TTI} \;?\; n?$$

However, it must be noted that the size of HSDPA TTI may change when the number of subchannels changes, i.e. TTI length for n-channel SAW HARQ can be shorter than one for dual channel SAW HARQ. Average receiver buffer sizes for dual channel HARQ for some block error rates are depicted in Figures 1-3.

Naturally, the number of subchannels in stop-and-wait ARQ is reflected in the amount of acknowledgment signaling needed to be sent to the transmitter. The complexity impact on RNS is mainly concentrated on Node B where the H-ARQ retransmission resides according to the current proposal. However, packet buffering is not as much an issue in Node B hardware.



kbps	8	32	64	384
dual channel 10 ms	672	2112	4032	23232
dual channel 3.33 ms	224	704	1344	7744

Figure 1. Average receiver L1 buffer size for BLER = 30%

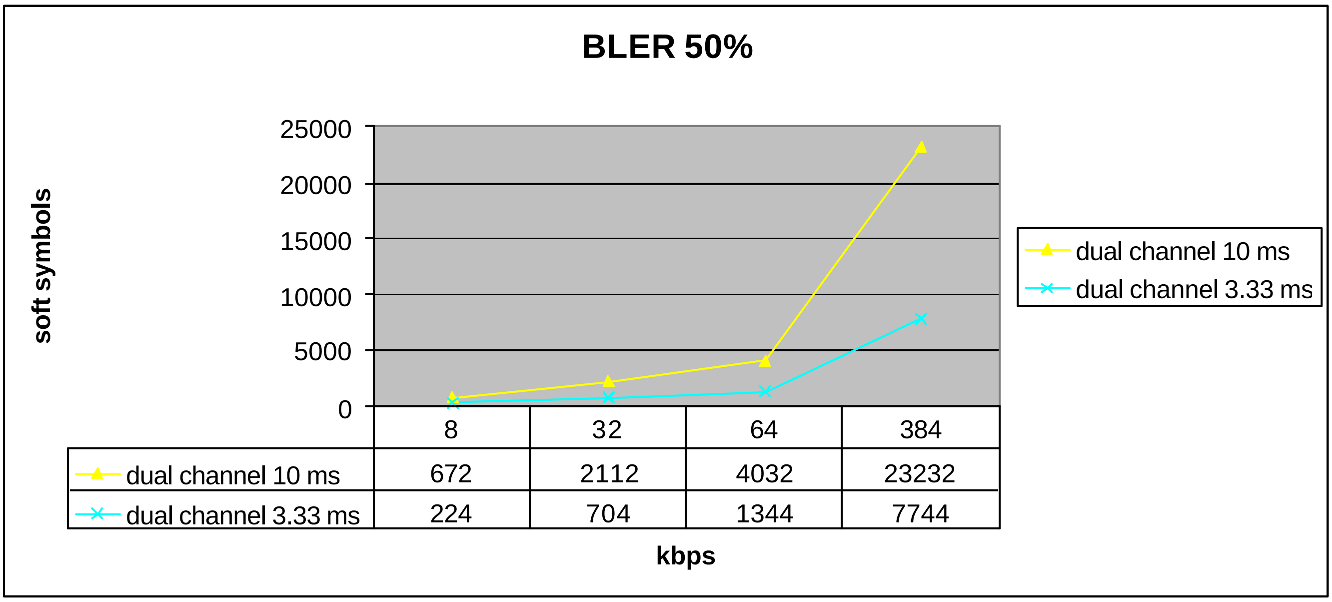


Figure 2. Average receiver L1 buffer size for BLER = 50%

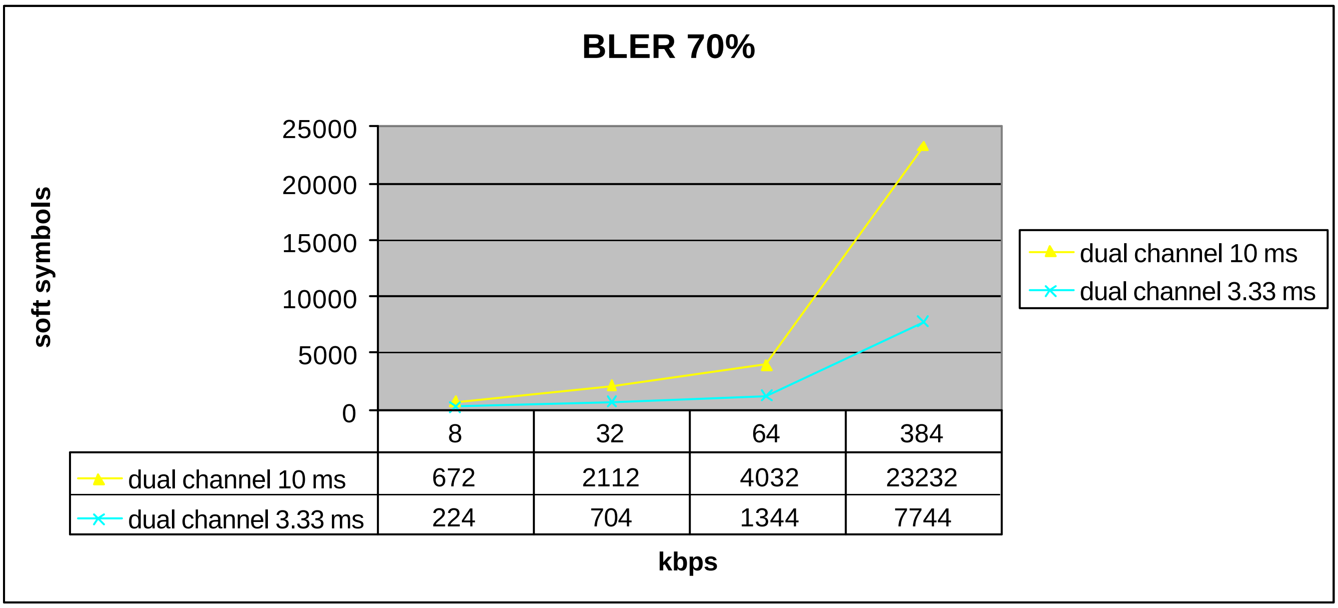


Figure 3. Average receiver L1 buffer size for BLER = 70%

7.2.2.1.3 Encoding/decoding and rate matching complexity

In order to facilitate incremental redundancy it is likely that the FEC encoder rate has to be lowered, i.e. instead of a 1/3 rate encoder, a 1/5 or even lower rate encoder would be employed. For example, as proposed this far, by puncturing different symbols out of the output code word, different redundancy information is generated for soft combining. A mother code of lower rate does increase the complexity of both encoding and decoding stage. However, it is not necessary to add new constituent encoders to a turbo coder in order to lower the coding rate. More advanced methods that output more than one symbol per bit per branch could be utilized. Furthermore, investigations are needed to check whether the existing rate matching algorithm of Rel –99 can be used in conjunction with incremental redundancy or whether modification of either the rate matching or the encoder are necessary"

7.2.2.1.4 UE and RNS processing time considerations

7.3 Fast Cell Selection (FCS)

7.3.1 Performance Evaluation <throughput, delay>

7.3.2 Complexity Evaluation <UE and RNS impacts>

7.4 Multiple Input Multiple Output Antenna Processing

7.4.1 Performance Evaluation <throughput, delay>

7.4.2 Complexity Evaluation <UE and RNS impacts>

8 Backwards compatibility aspects

9 Conclusions and recommendations