3GPP TSG RAN WG1 ***TSGR1#15(00)1098***
Berlin, Germany, 22nd – 25th August, 2000

Agenda item:

Source: **Philips**

Title: **DPCH initialisation procedure (revised)**

Document for: **Decision**

Introduction

The attached Release '99 CRs for TS25.211 and TS25.214 are the result of discussions and comments made since RAN1 #14 with the aim of clarifying the timing aspects of the procedure for initialisation of new DPCHs. In CR25211-071, it is proposed to delete section 7.7 "Timing relations for initialisation of channels" in TS25.211, so as to remove information which is only informative for layer 1 and is duplicated in the higher layer specifications. CR25214-123 inserts the remaining layer 1 information from section 7.7 into the synchronisation procedure in section 4.3 of TS25.214.

Summary of proposed corrections

The information in 25.211 section 7.7 regarding the time of the start of the DL DPCCH is the responsibility of higher layers in the UTRAN. The chip-offset of the frame boundaries is already defined in section 7.1.

The maximum total signalling response delay for the establishment of a new DPCH is defined in TS25.133 section 7.3, and a cross-reference to this section is therefore inserted in the synchronisation procedure in 25.214.

The purely informative parameters N_{offset_1} and N_{offset_2} are therefore removed from the layer 1 specifications.

All remaining information is consolidated into the synchronisation procedure, and cross-references to section 7.7 in 25.211 are updated to refer to appropriate sections in 25.214.

3GPP TSG RAN WG1 Meeting #15
Berlin, Germany, 22nd – 25th August, 2000

Document R1-00-1098
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

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25.211	CR	071	Current Version:	3.3.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to: RAN #9 *list expected approval meeting # here ↑*	for approval	X	strategic		*(for SMG use only)*
	for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from:* ftp://ftp.3gpp.org/Information/CR-Form-v2.doc

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Philips **Date:** 2000-08-20

Subject: DPCH initialisation procedure

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	X	**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature			Release 97	
C	Functional modification of feature			Release 98	
D	Editorial modification			Release 99	X
				Release 00	

Reason for change: Initialisation procedure for DPCHs needs to be consistent between specifications. Hence section 7.7 is deleted and cross-references are updated as appropriate.

Clauses affected: 5.2.1, 5.3.2, 7.7

Other specs affected:

Other 3G core specifications	X	→ List of CRs:	CR25.214-123r1
Other GSM core specifications		→ List of CRs:	
MS test specifications		→ List of CRs:	
BSS test specifications		→ List of CRs:	
O&M specifications		→ List of CRs:	

Other comments:

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5.2 Uplink physical channels

5.2.1 Dedicated uplink physical channels

There are two types of uplink dedicated physical channels, the uplink Dedicated Physical Data Channel (uplink DPDCH) and the uplink Dedicated Physical Control Channel (uplink DPCCH).

The DPDCH and the DPCCH are I/Q code multiplexed within each radio frame (see [4]).

The uplink DPDCH is used to carry the DCH transport channel. There may be zero, one, or several uplink DPDCHs on each radio link.

The uplink DPCCH is used to carry control information generated at Layer 1. The Layer 1 control information consists of known pilot bits to support channel estimation for coherent detection, transmit power-control (TPC) commands, feedback information (FBI), and an optional transport-format combination indicator (TFCI). The transport-format combination indicator informs the receiver about the instantaneous transport format combination of the transport channels mapped to the simultaneously transmitted uplink DPDCH radio frame. There is one and only one uplink DPCCH on each radio link.

Figure 1 shows the frame structure of the uplink dedicated physical channels. Each radio frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period.

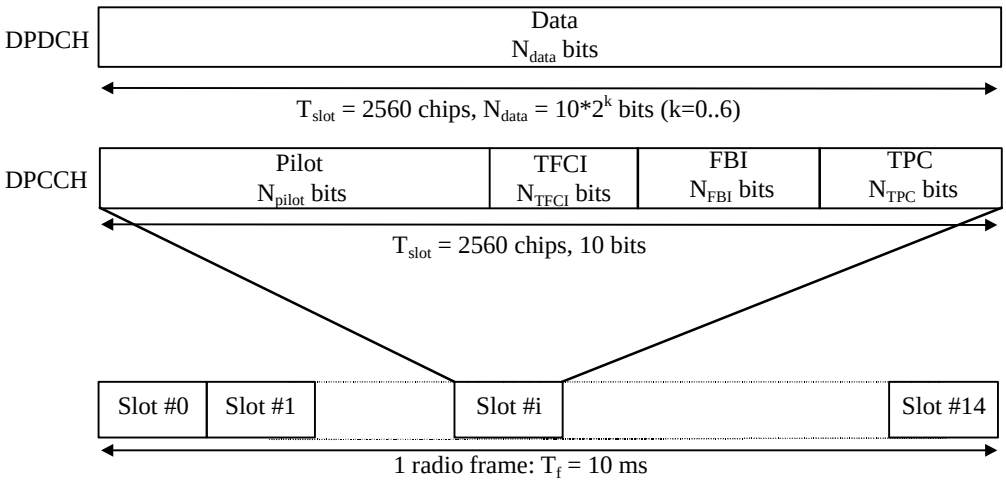

Figure 1: Frame structure for uplink DPDCH/DPCCH

The parameter k in figure 1 determines the number of bits per uplink DPDCH slot. It is related to the spreading factor SF of the DPDCH as SF = $256/2^k$. The DPDCH spreading factor may range from 256 down to 4. The spreading factor of the uplink DPCCH is always equal to 256, i.e. there are 10 bits per uplink DPCCH slot.

The exact number of bits of the uplink DPDCH and the different uplink DPCCH fields (N_{pilot}, N_{TFCI}, N_{FBI}, and N_{TPC}) is given by table 1 and table 2. What slot format to use is configured by higher layers and can also be reconfigured by higher layers.

The channel bit and symbol rates given in table 1 and table 2 are the rates immediately before spreading. The pilot patterns are given in table 3 and table 4, the TPC bit pattern is given in table 5.

The FBI bits are used to support techniques requiring feedback from the UE to the UTRAN Access Point, including closed loop mode transmit diversity and site selection diversity transmission (SSDT). The structure of the FBI field is shown in figure 2 and described below.

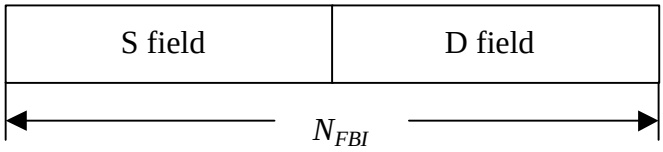

Figure 2: Details of FBI field

The S field is used for SSDT signalling, while the D field is used for closed loop mode transmit diversity signalling. The S field consists of 0, 1 or 2 bits. The D field consists of 0 or 1 bit. The total FBI field size N_{FBI} is given by table 2. Simultaneous use of SSDT power control and closed loop mode transmit diversity requires that the S field consists of 1 bit. The use of the FBI fields is described in detail in [5].

Table 1: DPDCH fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}
0	15	15	256	150	10	10
1	30	30	128	300	20	20
2	60	60	64	600	40	40
3	120	120	32	1200	80	80
4	240	240	16	2400	160	160
5	480	480	8	4800	320	320
6	960	960	4	9600	640	640

There are two types of uplink dedicated physical channels; those that include TFCI (e.g. for several simultaneous services) and those that do not include TFCI (e.g. for fixed-rate services). These types are reflected by the duplicated rows of table 2. It is the UTRAN that determines if a TFCI should be transmitted and it is mandatory for all UEs to support the use of TFCI in the uplink. The mapping of TFCI bits onto slots is described in [3].

In compressed mode, DPCCH slot formats with TFCI fields are changed. There are two possible compressed slot formats for each normal slot format. They are labelled A and B and the selection between them is dependent on the number of slots that are transmitted in each frame in compressed mode.

Table 2: DPCCH fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{pilot}	N_{TPC}	N_{TFCI}	N_{FBI}	Transmitted slots per radio frame
0	15	15	256	150	10	6	2	2	0	15
0A	15	15	256	150	10	5	2	3	0	10-14
0B	15	15	256	150	10	4	2	4	0	8-9
1	15	15	256	150	10	8	2	0	0	8-15
2	15	15	256	150	10	5	2	2	1	15
2A	15	15	256	150	10	4	2	3	1	10-14
2B	15	15	256	150	10	3	2	4	1	8-9
3	15	15	256	150	10	7	2	0	1	8-15
4	15	15	256	150	10	6	2	0	2	8-15
5	15	15	256	150	10	5	1	2	2	15
5A	15	15	256	150	10	4	1	3	2	10-14
5B	15	15	256	150	10	3	1	4	2	8-9

The pilot bit patterns are described in table 3 and table 4. The shadowed column part of pilot bit pattern is defined as FSW and FSWs can be used to confirm frame synchronization. (The value of the pilot bit pattern other than FSWs shall be "1".)

Table 3: Pilot bit patterns for uplink DPCCH with N_{pilot} = 3, 4, 5 and 6

	N_{pilot} = 3			N_{pilot} = 4				N_{pilot} = 5					N_{pilot} = 6					
Bit #	0	1	2	0	1	2	3	0	1	2	3	4	0	1	2	3	4	5
Slot #0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0
1	0	0	1	1	0	0	1	0	0	1	1	0	1	0	0	1	1	0
2	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1
3	0	0	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0
4	1	0	1	1	1	0	1	1	0	1	0	1	1	1	0	1	0	1
5	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0
6	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0	0
7	1	0	1	1	1	0	1	1	0	1	0	0	1	1	0	1	0	0
8	0	1	1	1	0	1	1	0	1	1	1	0	1	0	1	1	1	0
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1
11	1	0	1	1	1	0	1	1	0	1	1	1	1	1	0	1	1	1
12	1	0	1	1	1	0	1	1	0	1	0	0	1	1	0	1	0	0
13	0	0	1	1	0	0	1	0	0	1	1	1	1	0	0	1	1	1
14	0	0	1	1	0	0	1	0	0	1	1	1	1	0	0	1	1	1

Table 4: Pilot bit patterns for uplink DPCCH with N_{pilot} = 7 and 8

	N_{pilot} = 7							N_{pilot} = 8							
Bit #	0	1	2	3	4	5	6	0	1	2	3	4	5	6	7
Slot #0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
1	1	0	0	1	1	0	1	1	0	1	0	1	1	1	0
2	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1
3	1	0	0	1	0	0	1	1	0	1	0	1	0	1	0
4	1	1	0	1	0	1	1	1	1	1	0	1	0	1	1
5	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
6	1	1	1	1	0	0	1	1	1	1	1	1	0	1	0
7	1	1	0	1	0	0	1	1	1	1	0	1	0	1	0
8	1	0	1	1	1	0	1	1	0	1	1	1	1	1	0
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1
11	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
12	1	1	0	1	0	0	1	1	1	1	0	1	0	1	0
13	1	0	0	1	1	1	1	1	0	1	0	1	1	1	1
14	1	0	0	1	1	1	1	1	0	1	0	1	1	1	1

The relationship between the TPC bit pattern and transmitter power control command is presented in table 5.

Table 5: TPC Bit Pattern

TPC Bit Pattern		Transmitter power control command
N_{TPC} = 1	N_{TPC} = 2	
1	11	1
0	00	0

Multi-code operation is possible for the uplink dedicated physical channels. When multi-code transmission is used, several parallel DPDCH are transmitted using different channelization codes, see [4]. However, there is only one DPCCH per radio link.

A power control preamble may be used for initialisation of a DCH. Both the UL and DL DPCCHs shall be transmitted during the power control preamble. The length of the power control preamble is a UE-specific higher layer parameter, N_{pcp} (see [5], section 5.1.2.4), signalled by the network. The UL DPCCH shall take the same slot format in the power control preamble as afterwards, as given in table 2. When, $N_{pcp} > 0$ the pilot patterns from slot #(15- N_{pcp}) to slot #14 of table 3 and table 4 shall be used. The timing of the power control preamble is ~~shown in Figure 33~~described in [5], subclause 4.3.2.2~~7.7~~. The TFCI field is filled with "1" bits.

5.3.2 Dedicated downlink physical channels

There is only one type of downlink dedicated physical channel, the Downlink Dedicated Physical Channel (downlink DPCH).

Within one downlink DPCH, dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH), is transmitted in time-multiplex with control information generated at Layer 1 (known pilot bits, TPC commands, and an optional TFCI). The downlink DPCH can thus be seen as a time multiplex of a downlink DPDCH and a downlink DPCCH, compare subclause 5.2.1.

Figure 9 shows the frame structure of the downlink DPCH. Each frame of length 10 ms is split into 15 slots, each of length T_{slot} = 2560 chips, corresponding to one power-control period.

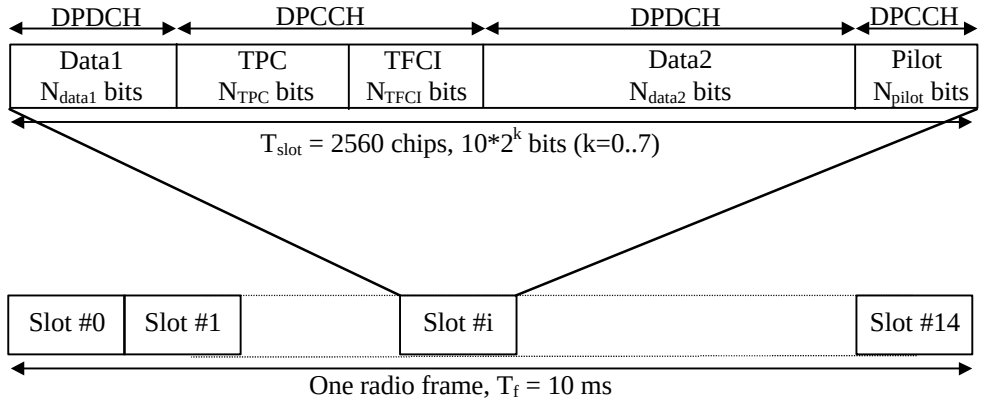

Figure 9: Frame structure for downlink DPCH

The parameter k in figure 9 determines the total number of bits per downlink DPCH slot. It is related to the spreading factor SF of the physical channel as $SF = 512/2^k$. The spreading factor may thus range from 512 down to 4.

The exact number of bits of the different downlink DPCH fields (N_{pilot}, N_{TPC}, N_{TFCI}, N_{data1} and N_{data2}) is given in table 11. What slot format to use is configured by higher layers and can also be reconfigured by higher layers.

There are basically two types of downlink Dedicated Physical Channels; those that include TFCI (e.g. for several simultaneous services) and those that do not include TFCI (e.g. for fixed-rate services). These types are reflected by the duplicated rows of table 11. It is the UTRAN that determines if a TFCI should be transmitted and it is mandatory for all UEs to support the use of TFCI in the downlink. The mapping of TFCI bits onto slots is described in [3].

In compressed mode, a different slot format is used compared to normal mode. There are two possible compressed slot formats that are labelled A and B. Format B is used for compressed mode by spreading factor reduction and format A is used for all other transmission time reduction methods. The channel bit and symbol rates given in table 11 are the rates immediately before spreading.

Table 11: DPDCH and DPCCH fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Slot	DPDCH Bits/Slot		DPCCH Bits/Slot			Transmitted slots per radio frame
					N_{Data1}	N_{Data2}	N_{TPC}	N_{TFCI}	N_{Pilot}	N_{Tr}
0	15	7.5	512	10	0	4	2	0	4	15
0A	15	7.5	512	10	0	4	2	0	4	8-14
0B	30	15	256	20	0	8	4	0	8	8-14
1	15	7.5	512	10	0	2	2	2	4	15
1B	30	15	256	20	0	4	4	4	8	8-14
2	30	15	256	20	2	14	2	0	2	15
2A	30	15	256	20	2	14	2	0	2	8-14
2B	60	30	128	40	4	28	4	0	4	8-14
3	30	15	256	20	2	12	2	2	2	15
3A	30	15	256	20	2	10	2	4	2	8-14
3B	60	30	128	40	4	24	4	4	4	8-14
4	30	15	256	20	2	12	2	0	4	15
4A	30	15	256	20	2	12	2	0	4	8-14
4B	60	30	128	40	4	24	4	0	8	8-14
5	30	15	256	20	2	10	2	2	4	15
5A	30	15	256	20	2	8	2	4	4	8-14
5B	60	30	128	40	4	20	4	4	8	8-14
6	30	15	256	20	2	8	2	0	8	15
6A	30	15	256	20	2	8	2	0	8	8-14
6B	60	30	128	40	4	16	4	0	16	8-14
7	30	15	256	20	2	6	2	2	8	15
7A	30	15	256	20	2	4	2	4	8	8-14
7B	60	30	128	40	4	12	4	4	16	8-14
8	60	30	128	40	6	28	2	0	4	15
8A	60	30	128	40	6	28	2	0	4	8-14
8B	120	60	64	80	12	56	4	0	8	8-14
9	60	30	128	40	6	26	2	2	4	15
9A	60	30	128	40	6	24	2	4	4	8-14
9B	120	60	64	80	12	52	4	4	8	8-14
10	60	30	128	40	6	24	2	0	8	15
10A	60	30	128	40	6	24	2	0	8	8-14
10B	120	60	64	80	12	48	4	0	16	8-14
11	60	30	128	40	6	22	2	2	8	15
11A	60	30	128	40	6	20	2	4	8	8-14
11B	120	60	64	80	12	44	4	4	16	8-14
12	120	60	64	80	12	48	4	8*	8	15
12A	120	60	64	80	12	40	4	16*	8	8-14
12B	240	120	32	160	24	96	8	16*	16	8-14
13	240	120	32	160	28	112	4	8*	8	15
13A	240	120	32	160	28	104	4	16*	8	8-14
13B	480	240	16	320	56	224	8	16*	16	8-14
14	480	240	16	320	56	232	8	8*	16	15
14A	480	240	16	320	56	224	8	16*	16	8-14
14B	960	480	8	640	112	464	16	16*	32	8-14
15	960	480	8	640	120	488	8	8*	16	15
15A	960	480	8	640	120	480	8	16*	16	8-14
15B	1920	960	4	1280	240	976	16	16*	32	8-14
16	1920	960	4	1280	248	1000	8	8*	16	15
16A	1920	960	4	1280	248	992	8	16*	16	8-14

* If TFCI bits are not used, then DTX shall be used in TFCI field.

NOTE1: Compressed mode is only supported through spreading factor reduction for SF=512 with TFCI.

NOTE2: Compressed mode by spreading factor reduction is not supported for SF=4.

The pilot bit patterns are described in table 12. The shadowed column part of pilot bit pattern is defined as FSW and FSWs can be used to confirm frame synchronization. (The value of the pilot bit pattern other than FSWs shall be "11".) In table 12, the transmission order is from left to right.

In downlink compressed mode through spreading factor reduction, the number of bits in the TPC and Pilot fields are doubled. Symbol repetition is used to fill up the fields. Denote the bits in one of these fields in normal mode by x_1, x_2, x_3, …, x_X. In compressed mode the following bit sequence is sent in corresponding field: x_1, x_2, x_1, x_2, x_3, x_4, x_3, x_4,…, x_X,.

Table 12: Pilot bit patterns for downlink DPCCH with N_{pilot} = 2, 4, 8 and 16

	N_{pilot} = 2	N_{pilot} = 4 (*1)		N_{pilot} = 8 (*2)				N_{pilot} = 16 (*3)							
Symbol #	0	0	1	0	1	2	3	0	1	2	3	4	5	6	7
Slot #0	11	11	11	11	11	11	10	11	11	11	10	11	11	11	10
1	00	11	00	11	00	11	10	11	00	11	10	11	11	11	00
2	01	11	01	11	01	11	01	11	01	11	01	11	10	11	00
3	00	11	00	11	00	11	00	11	00	11	00	11	01	11	10
4	10	11	10	11	10	11	01	11	10	11	01	11	11	11	11
5	11	11	11	11	11	11	10	11	11	11	10	11	01	11	01
6	11	11	11	11	11	11	00	11	11	11	00	11	10	11	11
7	10	11	10	11	10	11	00	11	10	11	00	11	10	11	00
8	01	11	01	11	01	11	10	11	01	11	10	11	00	11	11
9	11	11	11	11	11	11	11	11	11	11	11	11	00	11	11
10	01	11	01	11	01	11	01	11	01	11	01	11	11	11	10
11	10	11	10	11	10	11	11	11	10	11	11	11	00	11	10
12	10	11	10	11	10	11	00	11	10	11	00	11	01	11	01
13	00	11	00	11	00	11	11	11	00	11	11	11	00	11	00
14	00	11	00	11	00	11	11	11	00	11	11	11	10	11	01

NOTE *1: This pattern is used except slot formats 2B and 3B.

NOTE *2: This pattern is used except slot formats 0B, 1B, 4B, 5B, 8B, and 9B.

NOTE *3: This pattern is used except slot formats 6B, 7B, 10B, 11B, 12B, and 13B.

NOTE: For slot format *n*B where n = 0, …, 15, the pilot bit pattern corresponding to $N_{pilot}/2$ is to be used and symbol repetition shall be applied.

The relationship between the TPC symbol and the transmitter power control command is presented in table 13.

Table 13: TPC Bit Pattern

TPC Bit Pattern			Transmitter power control command
N_{TPC} = 2	N_{TPC} = 4	N_{TPC} = 8	
11	1111	11111111	1
00	0000	00000000	0

Multicode transmission may be employed in the downlink, i.e. the CCTrCH (see [3]) is mapped onto several parallel downlink DPCHs using the same spreading factor. In this case, the Layer 1 control information is transmitted only on the first downlink DPCH. DTX bits are transmitted during the corresponding time period for the additional downlink DPCHs, see figure 10.

In case there are several CCTrCHs mapped to different DPCHs transmitted to the same UE different spreading factors can be used on DPCHs to which different CCTrCHs are mapped. Also in this case, Layer 1 control information is only transmitted on the first DPCH while DTX bits are transmitted during the corresponding time period for the additional DPCHs.

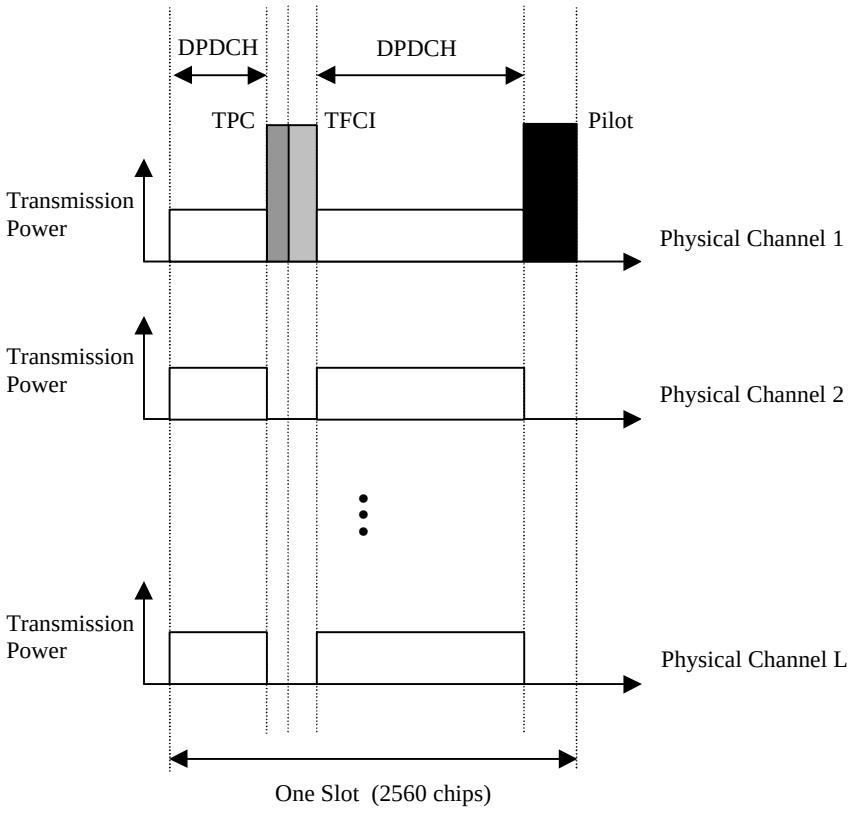

Figure 10: Downlink slot format in case of multi-code transmission

A power control preamble may be used for initialisation of a DCH. The DL DPCH shall take the same slot format in the power control preamble as afterwards, as given in Table 11, with the restriction that DTX shall be used in the DL DPDCH fields in the power control preamble. The length of the power control preamble is a UE-specific higher-layer parameter, N_{pcp} (see [5], section 5.1.2.4~~7.7~~), signalled by the network. When $N_{pcp} > 0$, the pilot patterns from slot #(15 – N_{pcp}) to slot #14 of table 12 shall be used. The TFCI field is filled with "1" bits.

5.3.2.1 STTD for DPCH

The pilot bit pattern for the DPCH channel transmitted on antenna 2 is given in table 14.

- For N_{pilot} = 8, 16 the shadowed part indicates pilot bits that are obtained by STTD encoding the corresponding (shadowed) bits in Table 12. The non-shadowed pilot bit pattern is orthogonal to the corresponding (non-shadowed) pilot bit pattern in table 12.

- For N_{pilot} = 4, the diversity antenna pilot bit pattern is obtained by STTD encoding both the shadowed and non-shadowed pilot bits in table 12.

- For N_{pilot} = 2, the diversity antenna pilot pattern is obtained by STTD encoding the two pilot bits in table 12 with the last two bits (data or DTX) of the second data field (data2) of the slot. Thus for N_{pilot} = 2 case, the last two bits of the second data field (data 2) after STTD encoding, follow the diversity antenna pilot bits in Table 14.

STTD encoding for the DPDCH, TPC, and TFCI fields is done as described in subclause 5.3.1.1.1. For the SF=512 $_{DPCH}$, the first two bits in each slot, i.e. TPC bits, are not STTD encoded and the same bits are transmitted with equal power from the two antennas. The remaining four bits are STTD encoded.

For compressed mode through spreading factor reduction and for $N_{pilot} > 4$, symbol repetition shall be applied to the pilot bit patterns of table 14, in the same manner as described in 5.3.2. For slot formats 2B and 3B, i.e. compressed mode through spreading factor reduction and N_{pilot} = 4, the pilot bits on antenna 1 are STTD encoded, and thus the pilot bit pattern is as shown in the most right set of table 14.

7 Timing relationship between physical channels

7.1 General

The P-CCPCH, on which the cell SFN is transmitted, is used as timing reference for all the physical channels, directly for downlink and indirectly for uplink.

Figure 28 below describes the frame timing of the downlink physical channels. For the AICH the access slot timing is included. Transmission timing for uplink physical channels is given by the received timing of downlink physical channels, as described in the following subclauses.

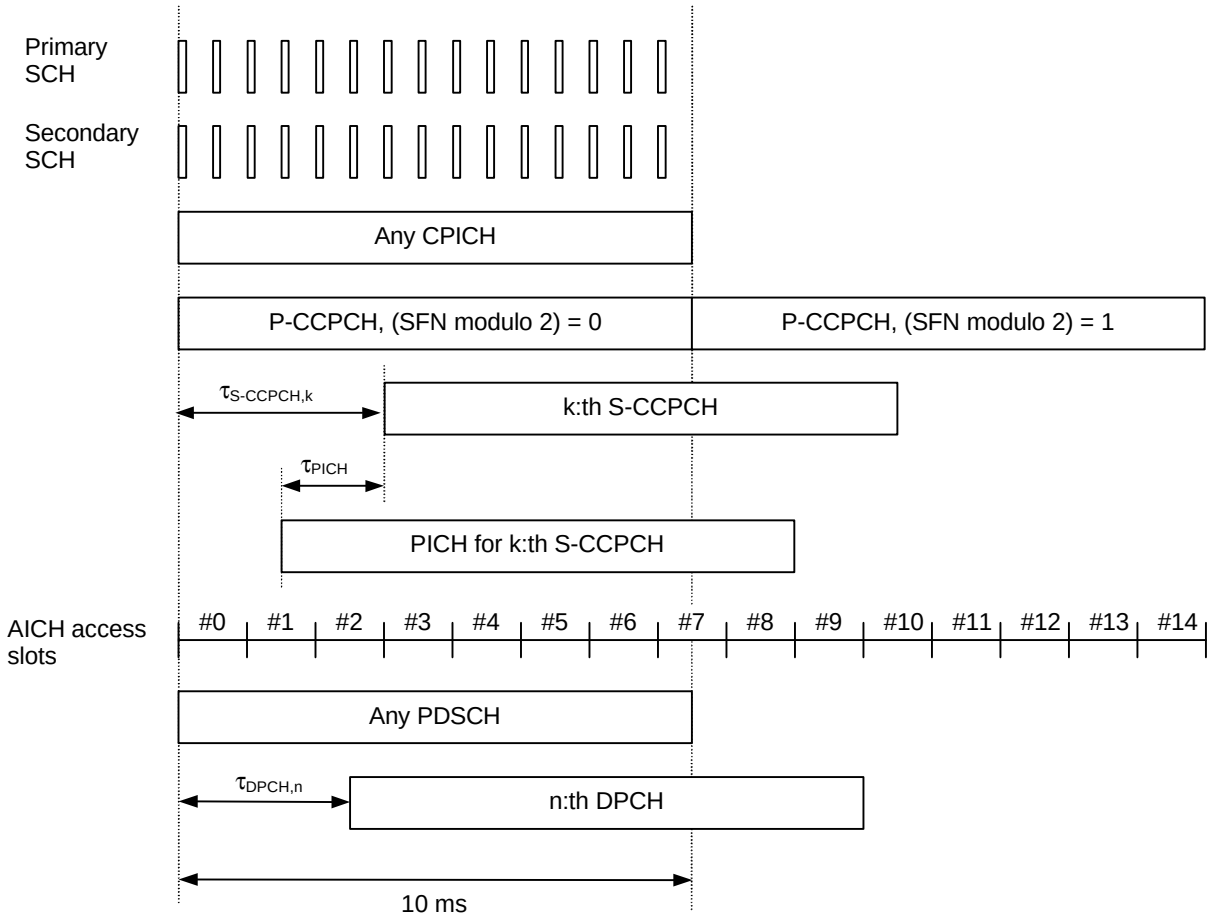

Figure 28: Frame timing and access slot timing of downlink physical channels

The following applies:

- SCH (primary and secondary), CPICH (primary and secondary), P-CCPCH, and PDSCH have identical frame timings.
- The S-CCPCH timing may be different for different S-CCPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{S\text{-}CCPCH,k} = T_k \times 256$ chip, $T_k \in \{0, 1, \ldots, 149\}$.
- The PICH timing is $\tau_{PICH} = 7680$ chips prior to its corresponding S-CCPCH frame timing, i.e. the timing of the S-CCPCH carrying the PCH transport channel with the corresponding paging information, see also subclause 7.2.
- AICH access slots #0 starts the same time as P-CCPCH frames with (SFN modulo 2) = 0. The AICH/PRACH and AICH/PCPCH timing is described in subclauses 7.3 and 7.4 respectively.

- The relative timing of associated PDSCH and DPCH is described in subclause 7.5.
- The DPCH timing may be different for different DPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{DPCH,n} = T_n \times 256$ chip, $T_n \in \{0, 1, \ldots, 149\}$. The DPCH (DPCCH/DPDCH) timing relation with uplink DPCCH/DPDCHs is described in subclause 7.6.

7.2 PICH/S-CCPCH timing relation

Figure 29 illustrates the timing between a PICH frame and its associated S-CCPCH frame, i.e. the S-CCPCH frame that carries the paging information related to the paging indicators in the PICH frame. A paging indicator set in a PICH frame means that the paging message is transmitted on the PCH in the S-CCPCH frame starting τ_{PICH} chips after the transmitted PICH frame. τ_{PICH} is defined in subclause 7.1.

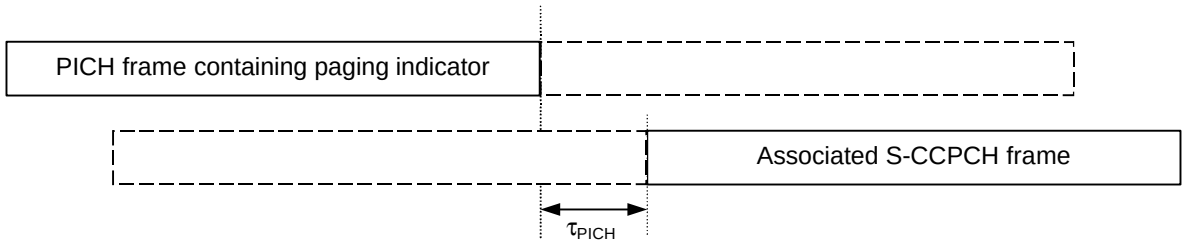

Figure 29: Timing relation between PICH frame and associated S-CCPCH frame

7.3 PRACH/AICH timing relation

The downlink AICH is divided into downlink access slots, each access slot is of length 5120 chips. The downlink access slots are time aligned with the P-CCPCH as described in subclause 7.1.

The uplink PRACH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number *n* is transmitted from the UE $\tau_{p\text{-}a}$ chips prior to the reception of downlink access slot number *n*, *n* = 0, 1, …, 14.

Transmission of downlink acquisition indicators may only start at the beginning of a downlink access slot. Similarly, transmission of uplink RACH preambles and RACH message parts may only start at the beginning of an uplink access slot.

The PRACH/AICH timing relation is shown in figure 30.

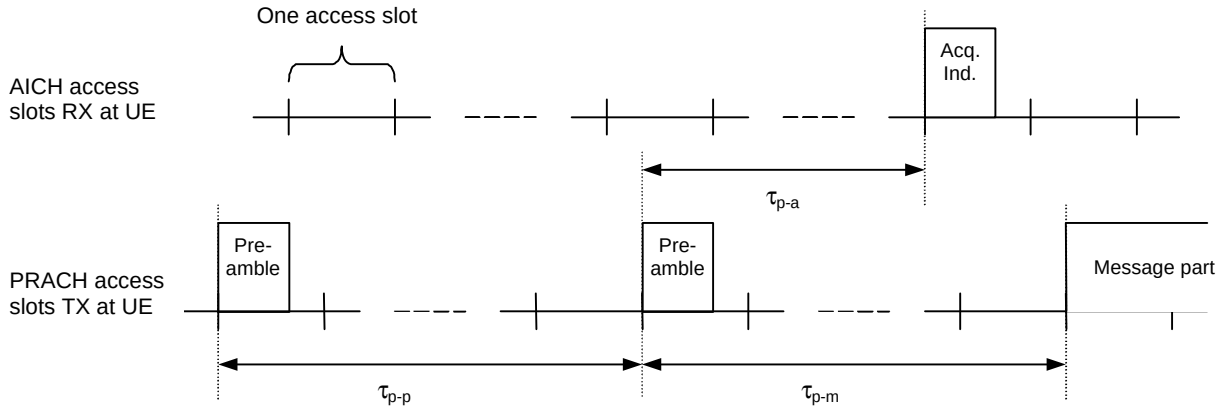

Figure 30: Timing relation between PRACH and AICH as seen at the UE

The preamble-to-preamble distance $\tau_{p\text{-}p}$ shall be larger than or equal to the minimum preamble-to-preamble distance $\tau_{p\text{-}p,min}$, i.e. $\tau_{p\text{-}p} \geq \tau_{p\text{-}p,min}$.

In addition to $\tau_{p\text{-}p,min}$, the preamble-to-AI distance $\tau_{p\text{-}a}$ and preamble-to-message distance $\tau_{p\text{-}m}$ are defined as follows:

- when AICH_Transmission_Timing is set to 0, then

  $\tau_{p\text{-}p,min}$ = 15360 chips (3 access slots)

  $\tau_{p\text{-}a}$ = 7680 chips

  $\tau_{p\text{-}m}$ = 15360 chips (3 access slots)

- when AICH_Transmission_Timing is set to 1, then

  $\tau_{p\text{-}p,min}$ = 20480 chips (4 access slots)

  $\tau_{p\text{-}a}$ = 12800 chips

  $\tau_{p\text{-}m}$ = 20480 chips (4 access slots)

The parameter AICH_Transmission_Timing is signalled by higher layers.

7.4 PCPCH/AICH timing relation

The uplink PCPCH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number n is transmitted from the UE $\tau_{p\text{-}a1}$ chips prior to the reception of downlink access slot number n, n =0, 1, …,14.

The timing relationship between preambles, AICH, and the message is the same as PRACH/AICH. Note that the collision resolution preambles follow the access preambles in PCPCH/AICH. However, the timing relationships between CD-Preamble and CD-ICH is identical to RACH Preamble and AICH. The timing relationship between CD-ICH and the Power Control Preamble in CPCH is identical to AICH to message in RACH. The T_{cpch} timing parameter is identical to the PRACH/AICH transmission timing parameter. When T_{cpch} is set to zero or one, the following PCPCH/AICH timing values apply.

Note that a1 corresponds to AP-AICH and a2 corresponds to CD-ICH.

$\tau_{p\text{-}p}$ = Time to next available access slot, between Access Preambles.

Minimum time = 15360 chips + 5120 chips X Tcpch

Maximum time = 5120 chips X 12 = 61440 chips

Actual time is time to next slot (which meets minimum time criterion) in allocated access slot subchannel group.

$\tau_{p\text{-}a1}$ = Time between Access Preamble and AP-AICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

$\tau_{a1\text{-}cdp}$ = Time between receipt of AP-AICH and transmission of the CD Preamble $\tau_{a1\text{-}cdp}$ has a minimum value of $\tau_{a1\text{-}cdp,\ min}$ =7680 chips.

$\tau_{p\text{-}cdp}$ = Time between the last AP and CD Preamble. $\tau_{p\text{-}cdp}$ has a minimum value of $\tau_{p\text{-}cdp\text{-}min}$ which is either 3 or 4 access slots, depending on T_{cpch}

$\tau_{cdp\text{-}a2}$ = Time between the CD Preamble and the CD-ICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

$\tau_{cdp\text{-}pcp}$ = Time between CD Preamble and the start of the Power Control Preamble is either 3 or 4 access slots, depending on $T_{cpch.}$

The message transmission shall start 0 or 8 slots after the start of the power control preamble depending on the length of the power control preamble.

Figure 31 illustrates the PCPCH/AICH timing relationship whenT_{cpch} is set to 0 and all access slot subchannels are available for PCPCH.

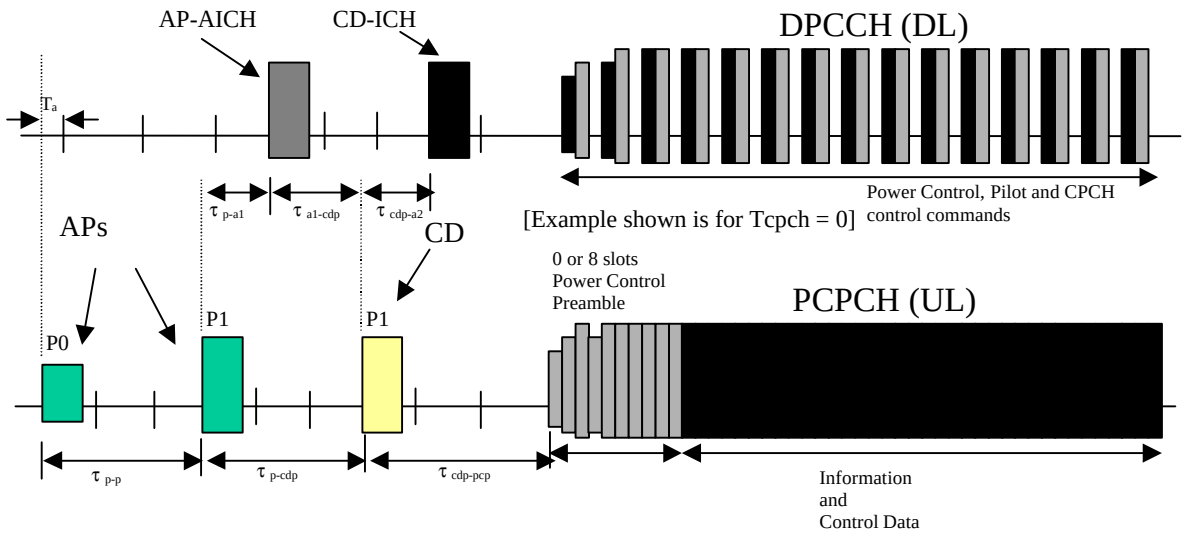

Figure 31: Timing of PCPCH and AICH transmission as seen by the UE, with T_{cpch}= 0

7.5 DPCH/PDSCH timing

The relative timing between a DPCH frame and the associated PDSCH frame is shown in figure 32.

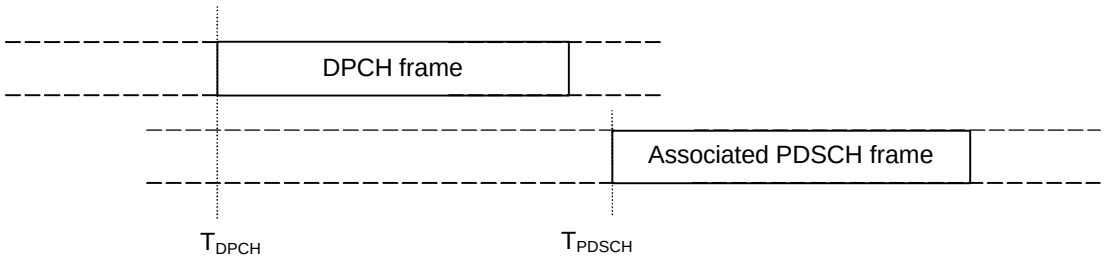

Figure 32: Timing relation between DPCH frame and associated PDSCH frame

The start of a DPCH frame is denoted T_{DPCH} and the start of the associated PDSCH frame is denoted T_{PDSCH}. Any DPCH frame is associated to one PDSCH frame through the relation 46080 chips ≤ T_{PDSCH} - T_{DPCH} < 84480 chips, i.e. the associated PDSCH frame starts anywhere between three slot after the end of the DPCH frame up to 18 slots behind the end of the DPCH frame.

7.6 DPCCH/DPDCH timing relations

7.6.1 Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

7.6.2 Downlink

In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

7.6.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of T_0 can be found in [5].

7.7 Timing relations for initialisation of channels

Figure 33 shows the timing relationships between the physical channels involved in the initialisation of a DCH.

The maximum time permitted for the UE to decode the relevant FACH frame before the first frame of the DPCCH is received shall be T_{B-min} = 38400 chips (i.e.15 slots).

The downlink DPCCH shall commence at a time T_B after the end of the relevant FACH frame, where $T_B \geq T_{B-min}$ according to the following equation:

$$T_B = (T_n - T_k) \times 256 - N_{pcp} \times 2560 + N_{offset\_1} \times 38400 \text{ chips}$$, where:

N_{pcp} is a higher layer parameter set by the network, and represents the length (in slots) of the power control preamble (see [5], subclause 5.1.2.4).

N_{offset_1} is a parameter set by higher layers and derived from the activation time if one is specified. In order that $T_B \geq T_{B-min}$, N_{offset_1} shall be an integer number of frames such that:

$$N_{offset\_1} \geq \begin{cases} 1 \text{ when } T_n - T_k \geq \dfrac{T_{B-\min}}{256} + 10N_{pcp} - 150 \\ 2 \text{ when } \dfrac{T_{B-\min}}{256} + 10N_{pcp} - 300 \leq T_n - T_k < \dfrac{T_{B-\min}}{256} + 10N_{pcp} - 150 \\ 3 \text{ when } T_n - T_k < \dfrac{T_{B-\min}}{256} + 10N_{pcp} - 300 \end{cases}$$

T_n and T_k are parameters defining the timing of the frame boundaries on the DL DPCCH and S-CCPCH respectively (see subclause 7.1). These parameters are provided by higher layers.

The uplink DPCCH shall commence at a time T_C after the end of the relevant FACH frame, where

$$T_C = T_B + T_0 + N_{offset\_2} \times 38400 \text{ chips}$$, where T_0 is as in subclause 7.6.3. If an activation time for the uplink DPCCH is specified, then N_{offset_2} shall be set to zero. Otherwise the stating time of the uplink DPCCH shall be determined by higher layers according to the procedure in TS 25.214 sub clause 4.3.2, subject to the constraint that N_{offset_2} shall be an integer number of frames greater than or equal to zero.

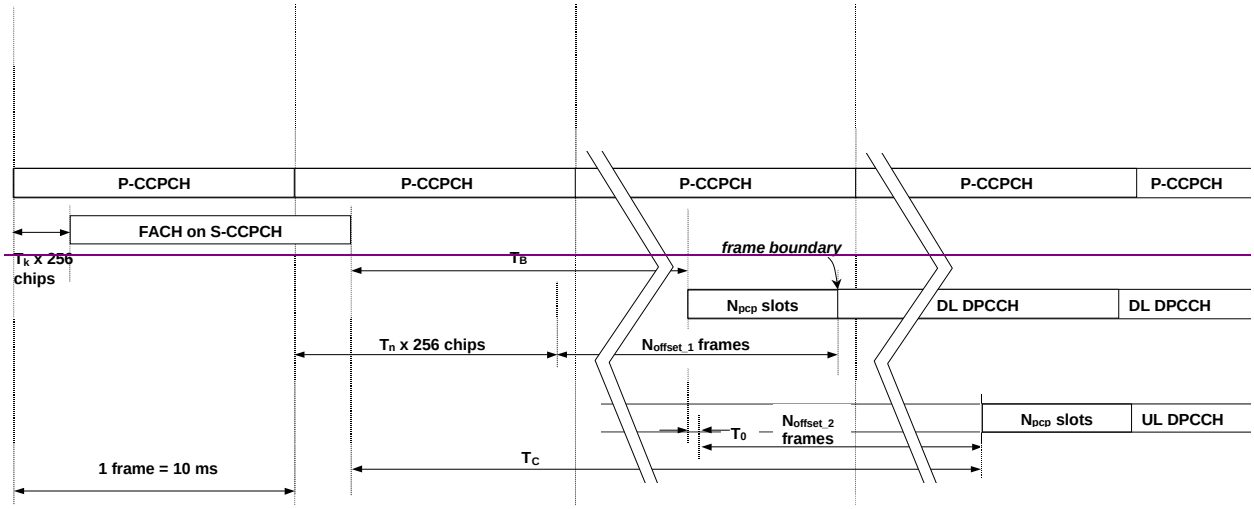

Figure 33: Timing for initialisation of DCH.

The data channels shall not commence before the end of the power control preamble.

3GPP TSG RAN WG1 Meeting #15
Berlin, Germany, 22nd – 25th August, 2000

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e.g. for 3GPP use the format TP-99xxx
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CHANGE REQUEST

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25.214	CR	123r1	Current Version:	3.3.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	RAN #9	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from:* ftp://ftp.3gpp.org/Information/CR-Form-v2.doc

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Philips **Date:** 2000-08-20

Subject: DPCH initialisation procedure

Work item:

Category: *(only one category Shall be marked With an X)*

F	Correction	X	**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature			Release 97	
C	Functional modification of feature			Release 98	
D	Editorial modification			Release 99	X
				Release 00	

Reason for change: Initialisation procedure for DPCHs needs to be consistent between specifications.

Clauses affected: 2, 4.3.2.2

Other specs Affected:

Other 3G core specifications	[ ]	→ List of CRs:	CR 25.211-071
Other GSM core specifications	[ ]	→ List of CRs:	
MS test specifications	[ ]	→ List of CRs:	
BSS test specifications	[ ]	→ List of CRs:	
O&M specifications	[ ]	→ List of CRs:	

Other comments:

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1 Scope

The present document specifies and establishes the characteristics of the physicals layer procedures in the FDD mode of UTRA.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.

[1] TS 25.211: "Physical channels and mapping of transport channels onto physical channels (FDD)".

[2] TS 25.212: "Multiplexing and channel coding (FDD)".

[3] TS 25.213: "Spreading and modulation (FDD)".

[4] TS 25.215: "Physical layer – Measurements (FDD)".

[5] TS 25.331: "RRC Protocol Specification".

[6] TS 25.433: "UTRAN Iub Interface NBAP Signalling".

[7] TS 25.101: "UE Radio transmission and Reception (FDD)".

[8] TS 25.133: "Requirements for Support of Radio Resource Management (FDD)".

3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

ASC	Access Service Class
AP	Access Preamble
BCH	Broadcast Channel
CCC	CPCH Control Command
CCPCH	Common Control Physical Channel
CD	Collision Detection
CPCH	Common Packet Channel
DCH	Dedicated Channel
DPCCH	Dedicated Physical Control Channel
DPCH	Dedicated Physical Channel
DTX	Discontinuous Transmission
DPDCH	Dedicated Physical Data Channel
FACH	Forward Access Channel
MUI	Mobile User Identifier
PCH	Paging Channel
PCPCH	Physical Common Packet Channel
PI	Paging Indication
PRACH	Physical Random Access Channel
RACH	Random Access Channel
SCH	Synchronisation Channel
SIR	Signal-to-Interference Ratio

4.3.2 Radio link establishment

4.3.2.1 General

The establishment of a radio link can be divided into two cases:

- when there is no existing radio link, i.e. when at least one downlink dedicated physical channel and one uplink dedicated physical channel are to be set up;
- or when one or several radio links already exist, i.e. when at least one downlink dedicated physical channel is to be set up and an uplink dedicated physical channel already exists.

The two cases are described in subclauses 4.3.2.2 and 4.3.2.3 respectively.

In Node B, each radio link set can be in three different states: initial state, out-of-sync state and in-sync state. Transitions between the different states is shown in figure 1 below. The state of the Node B at the start of radio link establishment is described in the following subclauses. Transitions between initial state and in-sync state are described in subclauses 4.3.2.2 and 4.3.2.3 and transitions between the in-sync and out-of-sync states are described in subclause 4.3.3.2.

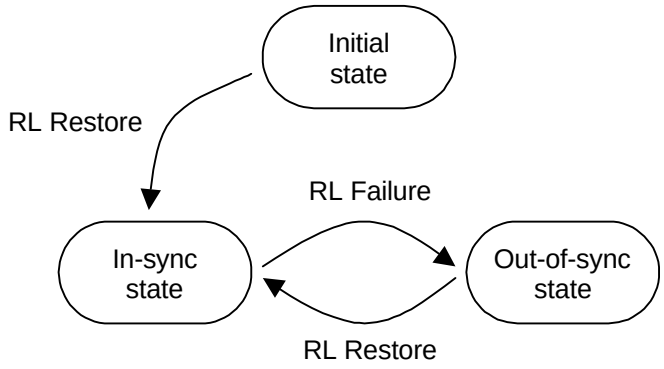

Figure 1: Node B radio link set states and transitions

4.3.2.2 No existing radio link

When one or several radio links are to be established and there is no existing radio link for the UE already, a dedicated physical channel is to be set up in uplink and at least one dedicated physical channel is to be set up in downlink. This corresponds to the case when a dedicated physical channel is initially set up on a frequency.

The radio link establishment is as follows:

a) Node B considers the radio link sets which are to be set up to be in the initial state. UTRAN starts the transmission of downlink DPCCH/DPDCHs.

b) The UE establishes downlink chip and frame synchronisation of DPCCH/DPDCHs, using the P-CCPCH timing and timing offset information notified from UTRAN. Frame synchronisation can be confirmed using the frame synchronisation word. Downlink synchronisation status is reported to higher layers every radio frame according to subclause 4.3.1.2.

c) If no activation time for uplink DPCCH/DPDCH has been signalled to the UE, uplink DPCCH/DPDCH transmission is started when higher layers consider the downlink physical channel established. If an activation time has been given, uplink DPCCH/DPDCH transmission is started at the activation time or later, as soon as higher layers consider the downlink physical channel established. Physical channel establishment and activation time are defined in [5]. The total signalling response delay for the establishment of a new DPCH shall not exceed the requirements given in [8] sub-clause 7.3. If a power control preamble of non-zero length is used for initialisation of the DCH, uplink DPDCH transmission shall not start before the end of the power control preamble. The length of the power control preamble is N_{pcp} slots beginning at the start of uplink DPCCH transmission, where N_{pcp} is a higher layer parameter set by the network (see section 5.1.2.4). ~~The timing of the start of the uplink channels is as defined in subclause 7.7 in [1].~~The starting time for transmission of DPDCHs shall also satisfy the constraints on adding transport channels to a CCTrCH, as defined in [2] sub-clause 4.2.14.

d) UTRAN establishes uplink chip and frame synchronisation. Frame synchronisation can be confirmed using the frame synchronisation word. Radio link sets remain in the initial state until N_INSYNC_IND successive in-sync indications are received from layer 1, when Node B shall trigger the RL Restore procedure indicating which radio link set has obtained synchronisation. When RL Restore has been triggered the radio link set shall be considered to be in the in-sync state. The parameter value of N_INSYNC_IND is configurable, see [6]. The RL Restore procedure may be triggered several times, indicating when synchronisation is obtained for different radio link sets.

4.3.2.3 One or several existing radio links

When one or several radio links are to be established and one or several radio links already exist, there is an existing DPCCH/DPDCH in the uplink, and at least one corresponding dedicated physical channel shall be set up in the downlink. This corresponds to the case when new radio links are added to the active set and downlink transmission starts for those radio links.

The radio link establishment is as follows:

a) Node B considers new radio link sets to be set up to be in initial state. If a radio link is to be added to an existing radio link set this radio link set shall be considered to be in the state the radio link set was prior to the addition of the radio link, i.e. if the radio link set was in the in-sync state before the addition of the radio link it shall remain in that state.

b) UTRAN starts the transmission of the downlink DPCCH/DPDCH at a frame timing such that the frame timing received at the UE will be within $T_0 \pm 148$ chips prior to the frame timing of the uplink DPCCH/DPDCH at the UE. Simultaneously, UTRAN establishes uplink chip and frame synchronisation of the new radio link. Frame synchronisation can be confirmed using the frame synchronization word. Radio link sets considered to be in the initial state shall remain in the initial state until N_INSYNC_IND successive in-sync indications are received from layer 1, when Node B shall trigger the RL Restore procedure indicating which radio link set has obtained synchronisation. When RL Restore is triggered the radio link set shall be considered to be in the in-sync state. The parameter value of N_INSYNC_IND is configurable, see [6]. The RL Restore procedure may be triggered several times, indicating when synchronisation is obtained for different radio link sets.

c) The UE establishes chip and frame synchronisation of the new radio link. Frame synchronisation can be confirmed using the frame synchronization word. Downlink synchronisation status shall be reported to higher layers every radio frame according to subclause 4.3.1.2.

4.3.3 Radio link monitoring

4.3.3.1 Downlink radio link failure

The downlink radio links shall be monitored by the UE, to trigger radio link failure procedures. The downlink radio link failure criteria is specified in [5], and is based on the synchronisation status primitives CPHY-Sync-IND and CPHY-Out-of-Sync-IND, indicating in-sync and out-of-sync respectively.

4.3.3.2 Uplink radio link failure/restore

The uplink radio link sets are monitored by the Node B, to trigger radio link failure/restore procedures. Once the radio link sets have been established, they will be in the in-sync or out-of-sync states as shown in figure 1 in subclause 4.3.2.1. Transitions between those two states are described below.

The uplink radio link failure/restore criteria is based on the synchronisation status primitives CPHY-Sync-IND and CPHY-Out-of-Sync-IND, indicating in-sync and out-of-sync respectively. Note that only one synchronisation status indication shall be given per radio link set.

When the radio link set is in the in-sync state, Node B shall start timer T_RLFAILURE after receiving N_OUTSYNC_IND consecutive out-of-sync indications. Node B shall stop and reset timer T_RLFAILURE upon receiving successive N_INSYNC_IND in-sync indications. If T_RLFAILURE expires, Node B shall trigger the RL Failure procedure and indicate which radio link set is out-of-sync. When the RL Failure procedure is triggered, the state of the radio link set change to the out-of-sync state.

When the radio link set is in the out-of-sync state, after receiving N_INSYNC_IND successive in-sync indications Node B shall trigger the RL Restore procedure and indicate which radio link set has re-established synchronisation. When the RL Restore procedure is triggered, the state of the radio link set change to the in-sync state.

The specific parameter settings (values of T_RLFAILURE, N_OUTSYNC_IND, and N_INSYNC_IND) are configurable, see [6].

4.3.4 Transmission timing adjustments

During a connection the UE may adjust its DPDCH/DPCCH transmission time instant.

If the receive timing for any downlink DPCCH/DPDCH in the current active set has drifted, so the time between reception of the downlink DPCCH/DPDCH in question and transmission of uplink DPCCH/DPDCH lies outside the valid range, L1 shall inform higher layers of this, so that the network can be informed of this and downlink timing can be adjusted by the network.

NOTE: The maximum rate of uplink TX time adjustment, and the valid range for the time between downlink DPCCH/DPDCH reception and uplink DPCCH/DPDCH transmission in the UE is to be specified by RAN WG4.

5 Power control

5.1 Uplink power control

5.1.1 PRACH

5.1.1.1 General

The power control during the physical random access procedure is described in clause 6. The setting of power of the message control and data parts is described in the next subclause.

5.1.1.2 Setting of PRACH control and data part power difference

The message part of the uplink PRACH channel shall employ gain factors to control the control/data part relative power similar to the uplink dedicated physical channels. Hence, subclause 5.1.2.5 applies also for the RACH message part, with the differences that:

- b_c is the gain factor for the control part (similar to DPCCH);
- b_d is the gain factor for the data part (similar to DPDCH);
- no inner loop power control is performed.

5.1.2 DPCCH/DPDCH

5.1.2.1 General

The initial uplink DPCCH transmit power is set by higher layers. Subsequently the uplink transmit power control procedure simultaneously controls the power of a DPCCH and its corresponding DPDCHs (if present). The relative transmit power offset between DPCCH and DPDCHs is determined by the network and is computed according to subclause 5.1.2.5 using the gain factors signalled to the UE using higher layer signalling.

The operation of the inner power control loop, described in sub clause 5.1.2.2, adjusts the power of the DPCCH and DPDCHs by the same amount, provided there are no changes in gain factors. Additional adjustments to the power of the DPCCH associated with the use of compressed mode are described in sub clause 5.1.2.3.