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TITLE:

Link Evaluation Methods for High Speed Downlink Packet Access (HSDPA)

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SOURCE:

ABSTRACT:

This document provides simulation assumptions related to link-level evaluation of high-speed packet downlink packet access (HSDPA) for 3GPP.

1 Introduction

In TSG-R1 meeting #14 both link and system level simulation assumptions for High Speed Downlink Packet Access (HSDPA) studies were presented [1,2,3] Two contribution presenting link and system level simulation assumptions applicable to different simulation platforms were agreed to be produced based on [1,2,3]. This contribution presents assumptions for link level simulations

1.1 Study Objective and Scope

The objective of this document is to propose a set of definitions, assumptions, and a general framework for performing initial link level simulations for High Speed Downlink Packet Access (HSDPA). The objective of these link level simulations is to provide the needed input data to initial system level simulations and to evaluate the link performance of different Adaptive Modulation and Coding schemes and fast Hybrid ARQ methods.

1.2 Simulation Description Overview

A symbol level downlink simulator may be used to simulate the performance of higher order modulation schemes and Hybrid ARQ. The general forward link simulation model is shown in Figure 1. The terminology used throughout the document is as follows: I_{or} is the total transmitted power density by a BTS, $\hat{I}_{or}$ is the post-channel transmitted power density, $I_{oc} + N_o$ is the other cell interference plus noise power density and I_o is the total received power density at the MS antenna. Note, that the ratio $\hat{I}_{or} / \left(I_{oc} + N_o \right)$ is fixed in this simulation model. Since the base station has a fixed amount of power (set by the BTS power amplifier size), it is the average transmitted (often called allocated) power by the BTS to the MS that determines the user capacity of the forward link. This fraction of allocated power is called average traffic channel E_c/I_{or} and is inversely proportional to the forward link capacity.

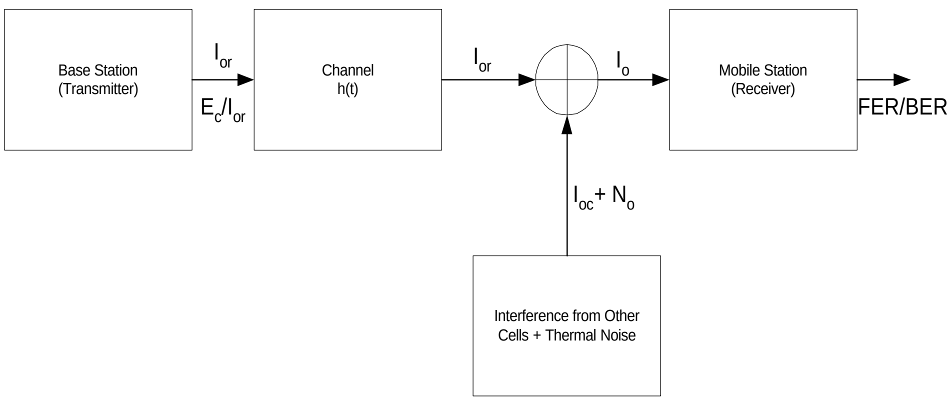

Figure 1. Simulation Block Diagram.

2 Standard Constellations for M-ary Modulation

In case of 8-PSK modulation, every three binary symbols from the channel interleaver output shall be mapped to a 8-PSK modulation symbol according to Figure 2.

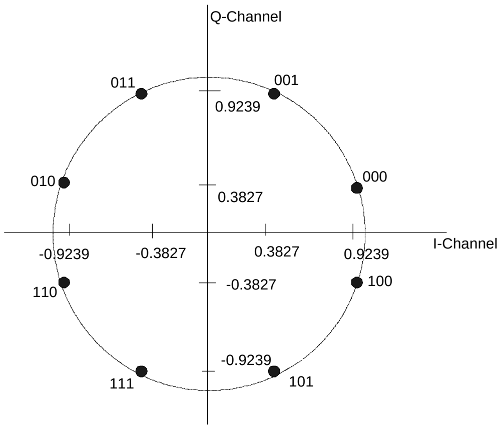

Figure 2. Signal Constellation for 8-PSK Modulation.

In case of 16-QAM modulation, every four binary symbols of the block interleaver output shall be mapped to a 16-QAM modulation symbol according to Figure 3.

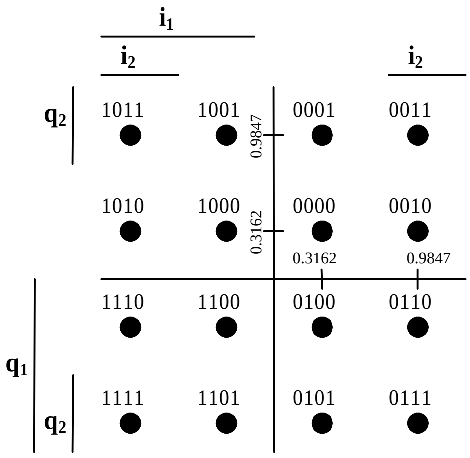

Figure 3. Signal Constellation for 16-QAM Modulation.

In case of 64-QAM modulation, every six binary symbols of the block interleaver output shall be mapped to a 64-QAM modulation symbol according to Figure 4.

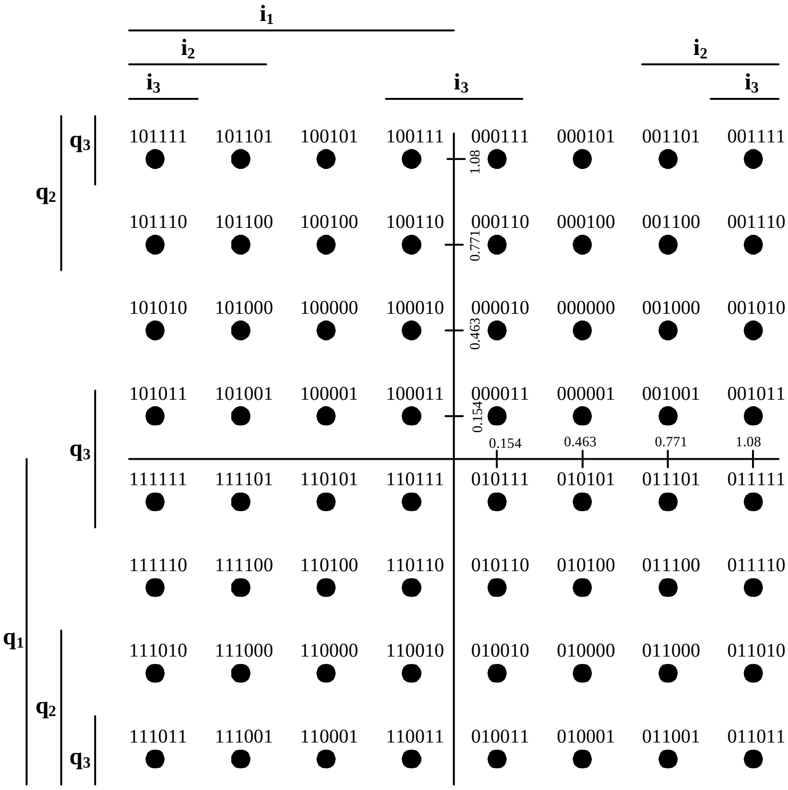

Figure 4. Signal Constellation for 64-QAM Modulation.

3 Turbo decoding

The *M*-ary QAM demodulator generates soft decisions as inputs to the Turbo decoder. As a baseline method, the soft inputs to the decoder may be generated by an approximation to the log-likelihood ratio function. First define,

$$\Lambda^{(i)}(z) = K_f\left[\underset{j\in S_i}{Min}\{d_j^2\} - \underset{j\in \overline{Si}}{Min}\{d_j^2\}\right],\ i = 0,1,2,\cdots,\log_2 M - 1 \quad (1)$$

where M is the modulation alphabet size, i.e. 8, 16, 32 or 64 and

$$z = A_d A_p a\ \hat{a}\ e^{-j(q-\hat{q})} x + n, \quad (2)$$

x is the transmitted QAM symbol, A_d is the traffic channel gain, A_p is the pilot channel gain, $a\ e^{jq}$ is the complex fading channel gain, and $A_p \hat{a}\ e^{j\hat{q}}$ is the fading channel estimate obtained from the pilot channel,

$$S_i = \{\forall j : i^{th} \text{ component of } y_j \text{ is "0"}\}, \quad (3)$$

$$\overline{S_i} = \{\forall j : i^{th} \text{ component of } y_j \text{ is "1"}\} \qquad (4)$$

and K_f is a scale factor proportional to the received signal-to-noise ratio. The parameter d_j is the Euclidean distance of the received symbol z from the points on the QAM constellation in S or its complement. The Pilot/Data gain is assumed known at the receiver. In this case the distance metric is computed as follows

$$d_j^2 = \left| A_p z - Q_j bg^2 \right|^2 \quad Q_j \in S_i \ \textbf{or} \ \overline{S}_i \qquad (5)$$

where $b = A_d$ and $g = A_p \hat{a}$ is an estimate formed from the pilot channel after processing through the channel estimation filter.

4 Performance Metrics and Simulation Parameters:

The following link performance criteria are used:

1. FER vs. E_c / I_{or} (for a fixed $\hat{I}_{or} / (I_{oc} + N_o)$) or

FER vs. $\hat{I}_{or} / (I_{oc} + N_o)$ (for a fixed E_c / I_{or})

2. Throughput vs. E_c/I_{oc}

where throughput measured in term of bits per second : $T = R\left(\frac{1 - FER_r}{\overline{N}}\right)$ in bits per second

where T is the throughput, R is the transmitted information bit rate and FER_r is the residual Frame Error Rate beyond the maximum number of transmissions and $\overline{N}$ is the average number of transmission attempts.

5 Simulation Parameters:

Table 1 provides a list of link-level simulation parameters.

Table 1. Simulation Parameters

Parameter	Value	Comments
Carrier Frequency	2GHz	
Propagation conditions	AWGN, Flat, Pedestrian A (3 Kmph)	Additional channel cases?
Vehicle Speed for Flat Fading	3 kmph/30 kmph/120 kmph	
CPICH relative power	10% (-10dB)	
Closed loop Power Control	OFF	Power control may be used for signalling channels associated with HSDPA transmission
HSDPA frame Length[1]	10ms, 3.33 ms, 0.67 ms	

[1] According to system simulation assumption document [4], 3.33 msec frame will be prioritized for simulation purpose.

Ior/Ioc	Variable	
Channel Estimation	Ideal/Non-Ideal(using CPICH)	
Fast fading model	Jakes spectrum	Generated e.g. by Jakes or filtering approach
Channel coding	Turbo code (PCCC), rate 1/4, 1/2, 3/4, etc.	
Tail bits	6	
Max no. of iterations for Turbo Coder	8	
Metric for Turbo Coder	Max[2]	
Input to Turbo Decoder	Soft	
Turbo Interleaver	Random	
Number of Rake fingers	Equal to number of taps in the channel model	
Hybrid ARQ	Chase combining	For initial evaluation of fast HARQ. Other schemes may also be studied.
Max number of frame transmissions for H-ARQ		Specify the value used
Information Bit Rates (Kbps)	As defined	
Number of Multicodes Simulated	As defined	
TFCI model	Random symbols, ignored in the receiver but it is assumed that the receiver gets error free reception of TFCI information	
STTD	On/Off	
Other L1 Parameters	As Specified in Release-99 Specification	

Table 2, 3, and 4 shows examples of numerology for HSDPA frames of length 0.67 ms (1 slot), 3.33 ms (5 slots), and 10 ms (15 slots) respectively for different MCS and different number of HSDPA codes.

[2] Optimum performance can be achieved with max* metric. However, this metric is sensitive to SNR scaling.

Table 2. Information bit rate for frame duration of 0.67 msec

Chip Rate = 3.84 Mcps				SF = 32			Frame Size = 0.67 ms	
	20 codes			1 code				
MCS	Info Rate (Mbps)	Info bits/frame (bits)	(octets)	Info Rate (Mbps)	Info bits/frame (bits)	(octets)	Code rate	Modulation
7	10.8000	7200	900	0.54	360	45	3/4	64
6	7.2000	4800	600	0.36	240	30	3/4	16
5	4.8000	3200	400	0.24	160	20	1/2	16
4	5.4000	3600	450	0.27	180	22.5	3/4	8
3	3.6000	2400	300	0.18	120	15	3/4	4
2	2.4000	1600	200	0.12	80	10	1/2	4
1	1.2000	800	100	0.06	40	5	1/4	4

Table 3 . Information bit rate for frame duration of 3.33 msec

Chip Rate = 3.84 Mcps				SF = 32			Frame Size = 3.33 ms	
	20 codes			1 code				
MCS	Info Rate (Mbps)	Info bits/frame (bits)	(octets)	Info Rate (Mbps)	Info bits/frame (bits)	(octets)	Code rate	Modulation
7	10.8000	36000	*4500*	0.54	1800	*225*	3/4	64
6	7.2000	24000	*3000*	0.36	1200	*150*	3/4	16
5	4.8000	16000	2000	0.24	800	100	1/2	16
4	5.4000	18000	2250	0.27	900	112.5	3/4	8
3	3.6000	12000	1500	0.18	600	75	3/4	4
2	2.4000	8000	*1000*	0.12	400	*50*	1/2	4
1	1.2000	4000	500	0.06	200	25	1/4	4

Table 4. Information bit rate for frame duration of 10 msec

Chip Rate = 3.84 Mcps				SF = 32			Frame Size = 10.00 ms	
	20 codes			1 code				
MCS	Info Rate (Mbps)	Info bits/frame (bits)	(octets)	Info Rate (Mbps)	Info bits/frame (bits)	(octets)	Code rate	Modulation
7	10.8000	1E+05	13500	0.54	5400	675	3/4	64
6	7.2000	72000	9000	0.36	3600	450	3/4	16
5	4.8000	48000	6000	0.24	2400	300	1/2	16
4	5.4000	54000	6750	0.27	2700	337.5	3/4	8
3	3.6000	36000	4500	0.18	1800	225	3/4	4
2	2.4000	24000	3000	0.12	1200	150	1/2	4

REFERENCES

[1] Motorola. Link Evaluation Methods for High Speed Downlink Packet Access (HSDPA). TSG-R1 document, TSGR#14(00)0910, 4-7th, July, 2000, Oulu, Finland, 6 pp.

[2] Motorola. Evaluation Methods for High Speed Downlink Packet Access (HSDPA). TSG-R1 document, TSGR#14(00)0909, 4-7th, July, 2000, Oulu, Finland, 15 pp.

[3] Nokia. High Speed Downlink Packet Access simulation assumptions. TSG-R1 document, TSGR#14(00)0881, 4-7th, July, 2000, Oulu, Finland, 9 pp.

[4] Nokia, Ericsson, Motorola, Common HSDPA system simulation assumptions, TSGR#15(00)XXXX, August, 2000, Berlin, Germany.