TSG-RAN Working Group 1 meeting #14
Oulu, Finland
July 4th – 7th, 2000

TSGR1#14(00)0925

Agenda item:

Source: Samsung

Title: DPCH timing offset in CPCH

Document for: Discussion and approval

Background

When the DPCH is set up to UE, the timing offset may be allocated to each channel. The timing offset of the each channel is the multiple of the 256 chips. It improves the performance in view of the downlink radiation power. Since the powers of the TPC, TFCI, and Pilot are higher than that of the DPDCH, it is reasonable to spread the locations of those fields. One more advantage is improving load balance in the UTRAN. Since the uplink data is distributed over the time period, the decoding load is spread in a frame. Now, for consistency, in the CPCH, since there is a DPCH, the timing offset is needed for downlink DPCCH in CPCH.

Proposed Correction

Since the DPCH has the timing offset, we propose the DPCH timing offset in CPCH for the consistency. Furthermore, since the CPCH timing unit is Access Slot, the spreading locations of the timing offset are based on the Access Slot. So, after receiving the CD or CD/CA from the UTRAN, the message part may be started at the given timing offset for the CPCH channel.

- Now, the change of the 25.211 is about the $\tau_{cdp\text{-}pcp}$, which is the time between CD Preamble and the start of the Power Control Preamble. The Previous one has the value of 3 or 4 access slots. The proposed one has the value as follows. It has the value of 3 or 4 access slots plus $\tau_{CPCH,n}$ chips, where it has the value between from 0 chips to 4608 chips.

  $\tau_{cdp\text{-}pcp} = (T_{cpch} + 3)$ X 5120 + $\tau_{CPCH,n}$ chips, where $\tau_{CPCH,n} = T_{CPCH,n} \times 512$ chip, $T_{CPCH,n} \in \{0, 1, \ldots, 9\}$.

- We propose 512 chips multiples for $\tau_{CPCH,n}$ because the SF of the downlink is 512.

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3GPP TSG RAN WG1 Meeting #14
Oulu, Finland, 4th – 7th July 2000

Document R1-00-925
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.211	CR	069	Current Version:	3.3.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	RAN#9	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Samsung **Date:** 07/07/2000

Subject: DPCH timing offset in CPCH

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	X	**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature			Release 97	
C	Functional modification of feature			Release 98	
D	Editorial modification			Release 99	X
				Release 00	

Reason for change: For the consistency, since there is the timing offset in DPCH, the timing offset is needed for CPCH message part DPCH.

Clauses affected: 7.4

Other specs affected:

Other 3G core specifications	[ ]	→ List of CRs:
Other GSM core specifications	[ ]	→ List of CRs:
MS test specifications	[ ]	→ List of CRs:
BSS test specifications	[ ]	→ List of CRs:
O&M specifications	[ ]	→ List of CRs:

Other comments:

help.doc

<--------- double-click here for help and instructions on how to create a CR.

$\tau_{p\text{-}a}$ = 12800 chips

$\tau_{p\text{-}m}$ = 20480 chips (4 access slots)

The parameter AICH_Transmission_Timing is signalled by higher layers.

7.4 PCPCH/AICH timing relation

The uplink PCPCH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number n is transmitted from the UE $\tau_{p\text{-}a1}$ chips prior to the reception of downlink access slot number n, n =0, 1, …,14.

The timing relationship between preambles, AICH, and the message is the same as PRACH/AICH. Note that the collision resolution preambles follow the access preambles in PCPCH/AICH. However, the timing relationships between CD-Preamble and CD-ICH is identical to RACH Preamble and AICH. The timing relationship between CD-ICH and the Power Control Preamble in CPCH is identical to AICH to message in RACH. The T_{cpch} timing parameter is identical to the PRACH/AICH transmission timing parameter. When T_{cpch} is set to zero or one, the following PCPCH/AICH timing values apply.

Note that a1 corresponds to AP-AICH and a2 corresponds to CD-ICH.

$\tau_{p\text{-}p}$ = Time to next available access slot, between Access Preambles.

Minimum time = 15360 chips + 5120 chips X Tcpch

Maximum time = 5120 chips X 12 = 61440 chips

Actual time is time to next slot (which meets minimum time criterion) in allocated access slot subchannel group.

$\tau_{p\text{-}a1}$ = Time between Access Preamble and AP-AICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

$\tau_{a1\text{-}cdp}$ = Time between receipt of AP-AICH and transmission of the CD Preamble $\tau_{a1\text{-}cdp}$ has a minimum value of $\tau_{a1\text{-}cdp,\ min}$ =7680 chips.

$\tau_{p\text{-}cdp}$ = Time between the last AP and CD Preamble. $\tau_{p\text{-}cdp}$ has a minimum value of $\tau_{p\text{-}cdp\text{-}min}$ which is either 3 or 4 access slots, depending on T_{cpch}

$\tau_{cdp\text{-}a2}$ = Time between the CD Preamble and the CD-ICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

~~$\tau_{cdp\text{-}pcp}$ = Time between CD Preamble and the start of the Power Control Preamble is either 3 or 4 access slots, depending on T_{cpch}.~~

$\tau_{cdp\text{-}pcp}$ = Time between CD Preamble and the start of the Power Control Preamble:

$(T_{cpch} + 3)$ X 5120 + $\tau_{CPCH,n}$ chips, where $\tau_{CPCH,n} = T_{CPCH,n} \times 512$ chip, $T_{CPCH,n} \in \{0, 1, \ldots, 9\}$.

The message transmission shall start 0 or 8 slots after the start of the power control preamble depending on the length of the power control preamble.

Figure 31 illustrates the PCPCH/AICH timing relationship whenT_{cpch} is set to 0 and all access slot subchannels are available for PCPCH.

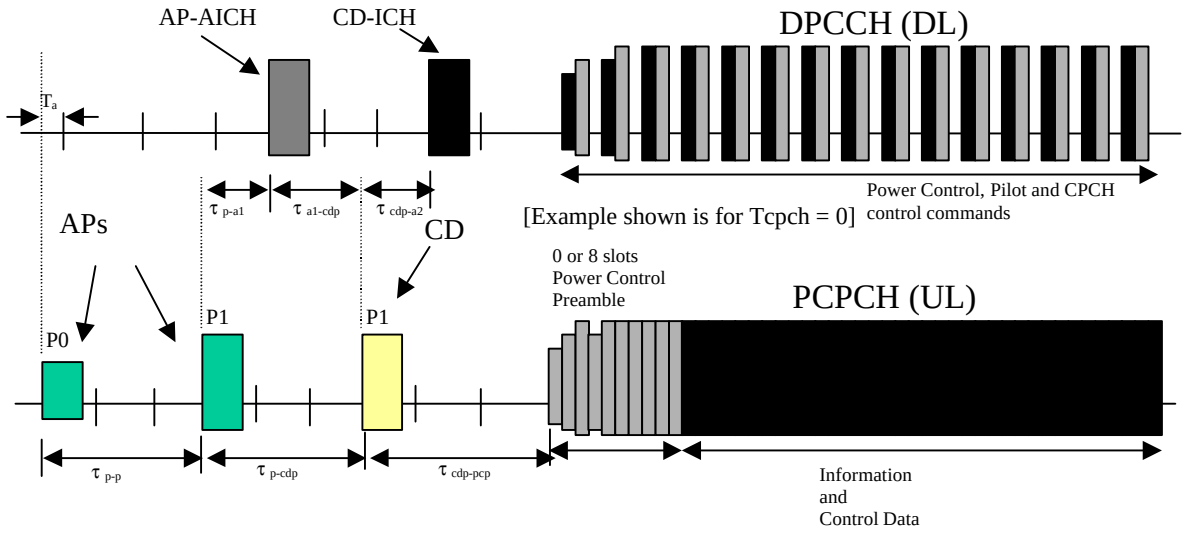

Figure 31: Timing of PCPCH and AICH transmission as seen by the UE, with T_{cpch}= 0

7.5 DPCH/PDSCH timing

The relative timing between a DPCH frame and the associated PDSCH frame is shown in figure 32.

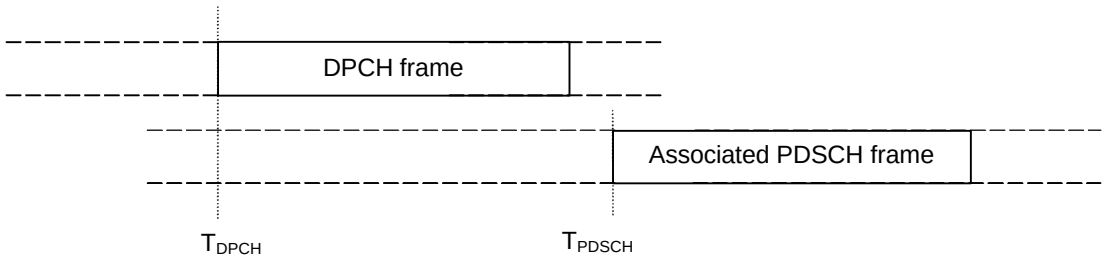

Figure 32: Timing relation between DPCH frame and associated PDSCH frame

The start of a DPCH frame is denoted T_{DPCH} and the start of the associated PDSCH frame is denoted T_{PDSCH}. Any DPCH frame is associated to one PDSCH frame through the relation 46080 chips ≤ T_{PDSCH} - T_{DPCH} < 84480 chips, i.e. the associated PDSCH frame starts anywhere between three slot after the end of the DPCH frame up to 18 slots behind the end of the DPCH frame.

7.6 DPCCH/DPDCH timing relations

7.6.1 Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

7.6.2 Downlink

In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

7.6.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of T_0 can be found in [5].