TSG-RAN Working Group 1 , AdHoc 21 **TSGR1(00)0827**

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Agenda Item: AH21
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To: TSG RAN WG1
Title: Examples of service mapping for low chip rate TDD option
Document for: Discussion and Approval

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1 Introduction

Due to the different burst structure, number of bits per physical channel in 1.28Mcps TDD is different from 3.84Mcps TDD. This contribution provides some examples for mapping of services to physical channels in 1.28Mcps TDD.

Conclusion

This document describes some examples of service mapping for low chip rate TDD option, it is proposed to include these examples of service mapping for low chip rate TDD option in Annex B of TR 25.928

---------- changes to TR25.928 begin ----------

Annex B Examples of service mapping

B.1 BCH

Table B.1 Parameters for BCH

Transport block size	246 bits+1bit (*)
CRC	16 bits
Coding	CC, coding rate = 1/3 This has to be included in table 1 in 25.222 4.2.3.
TTI	20 ms
Midamble	144 chips
Codes and time slots	SF = 16 2 codes x 1 time slot
TFCI	0 bit
L1 control signals	0 bit

Note: The example is applied to BCH without multiplexing PCH and FACH.
*: 1 extra bit in transport block is used for BCH indication.

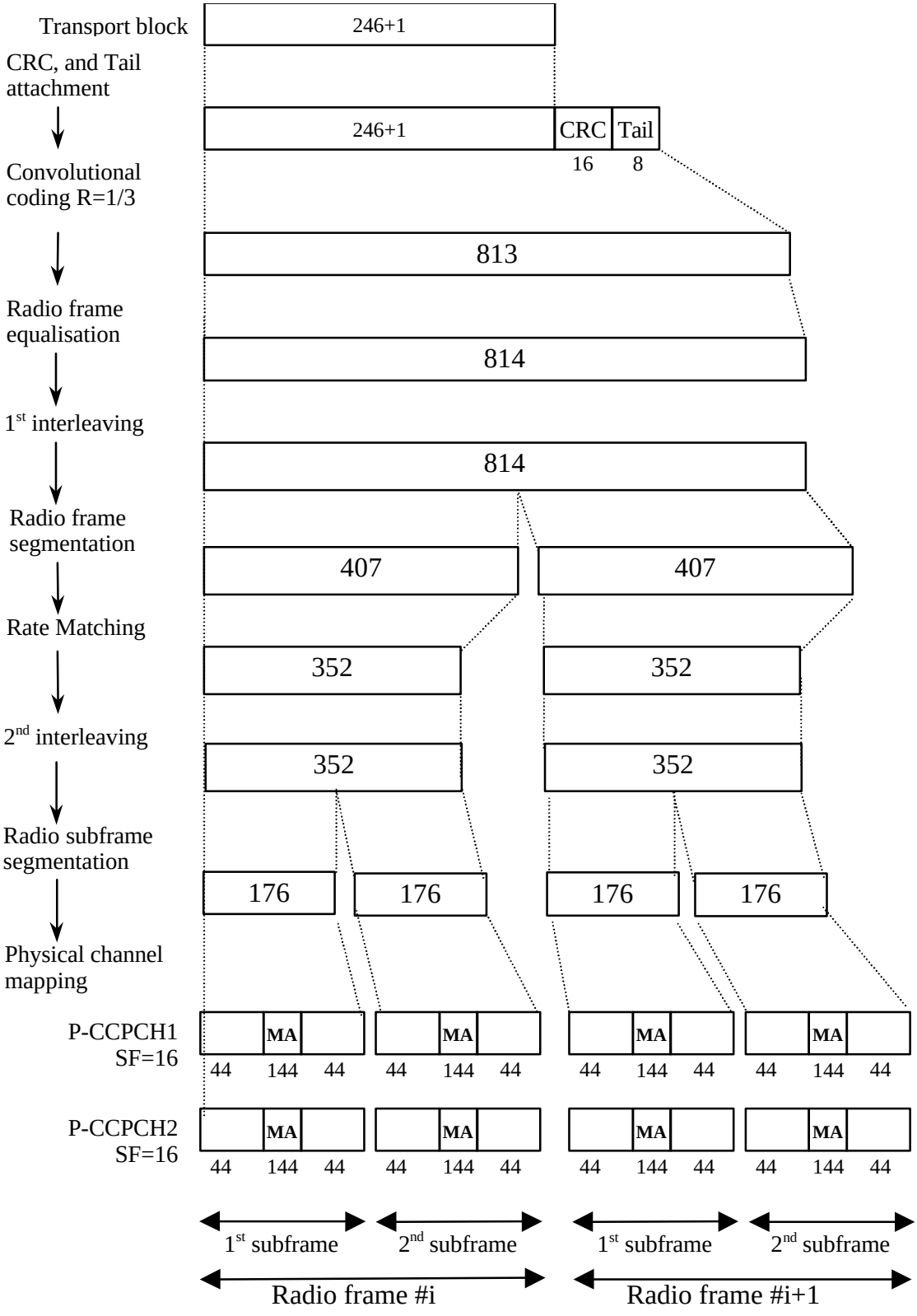


Figure B.1 Service mapping for BCH

B.2 2.4kbps data for downlink

Table B.2 Parameter examples for 2.4kbps data

Transport block set size	48 bits
CRC	16 bits
Coding	CC, coding rate = 1/2
TTI	20 ms

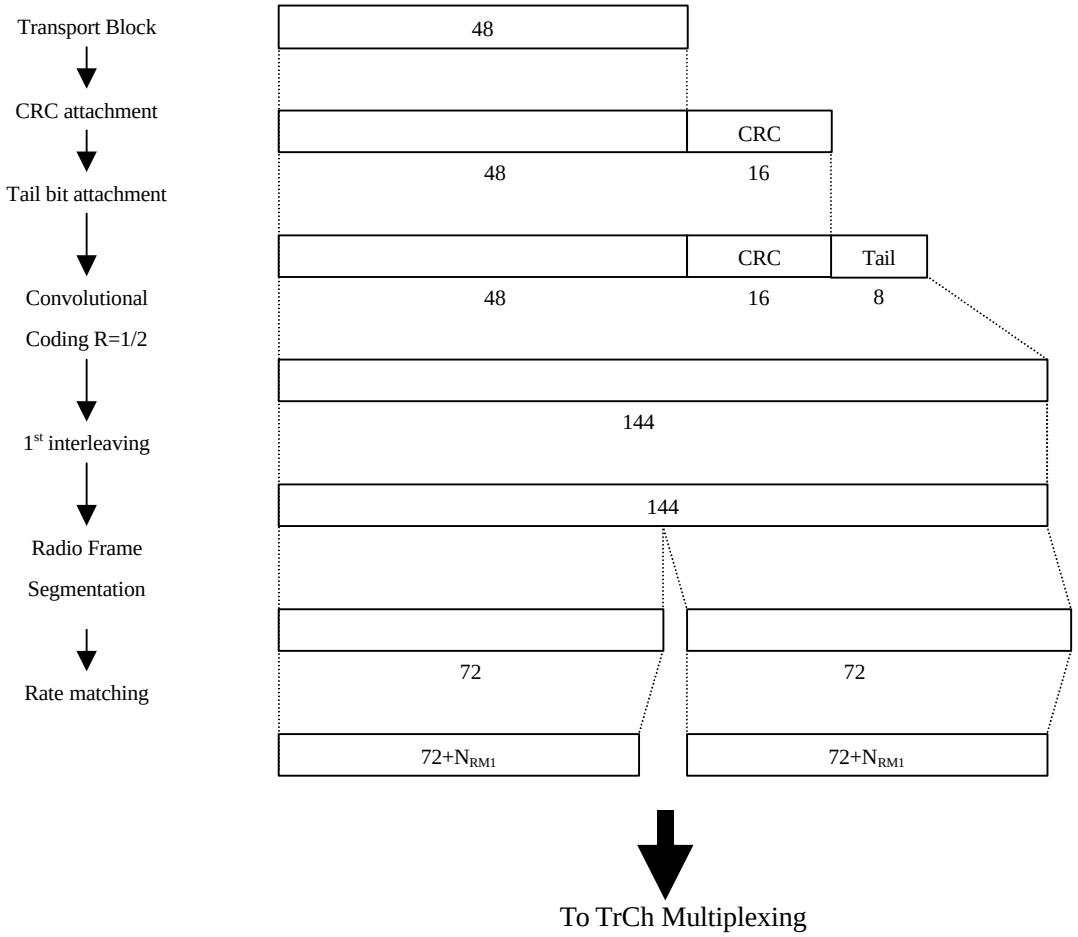


Figure B.2 Channel coding for 2.4kbps data

B.3 12.2kbps data for downlink

Note: this example can be applied to AMR speech

Table B.3 Parameter examples for 12.2kbps data

Number of TrChs	3
Transport block size	81bits(TrCh#1) 103bits(TrCh#2) 60bits(TrCh#3)
CRC	12(Only for TrCh#1)
Coding	CC, coding rate = 1/2, class B, C CC, coding rate = 1/3, class A
TTI	20 ms
Midamble	144 chips
Codes and time slots	SF = 16 2 codes x 1 time slots
TFCI	16bits (8 bits in each subframe)
L1control signals	4bits

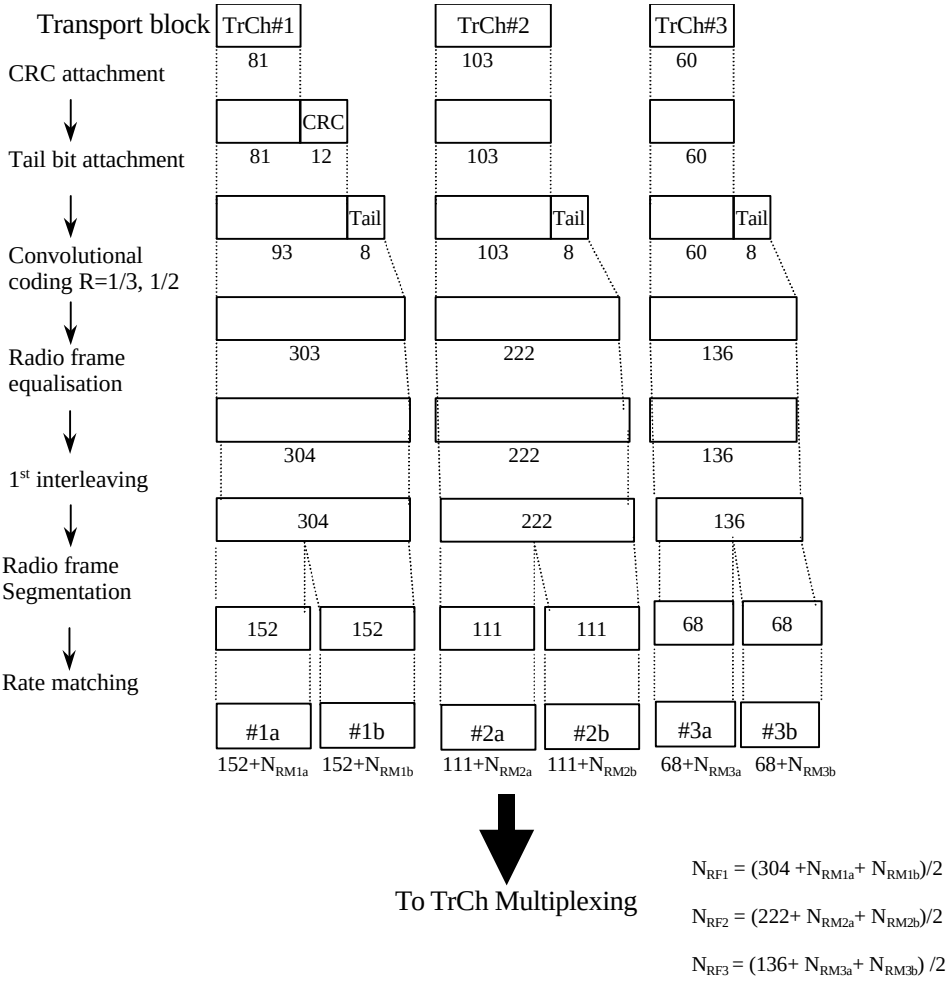
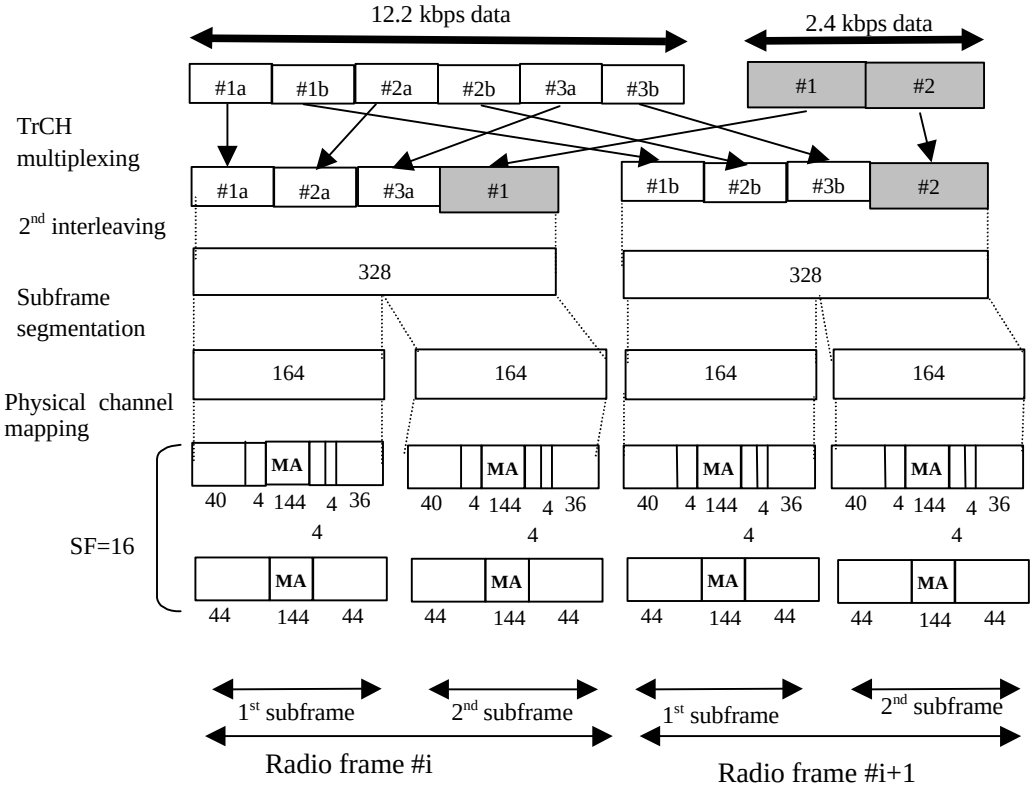


Figure B.3 Channel coding for 12.2kbps AMR

B.3-1 Example for multiplexing of 12.2 kbps data and 2.4 kbps data



B.4 384kbps packet data for downlink

Table B.4 Parameter examples for 384kbps packet data

The number of TrChs	1
Transport block set size	3840*B bits(B=0,1,2)
Segmentation C	1 (B = 0, 1) or 2 (B = 2)
CRC	16 bits
Coding	Turbo coding, coding rate = 1/3
TTI	20 ms
Midamble	144chips
Codes and time slots	SF = 16 16 codes x 4 time slots
TFCI	16bits
L1 signals	4 bits

Note1: 13codes*4 time slots+12codes*1 time slot is under considered.
Note2: Convolutional code with code rate 1/3 is optional for 384kbps packet data if UE capability supports it. B=2 for the figure B.4.

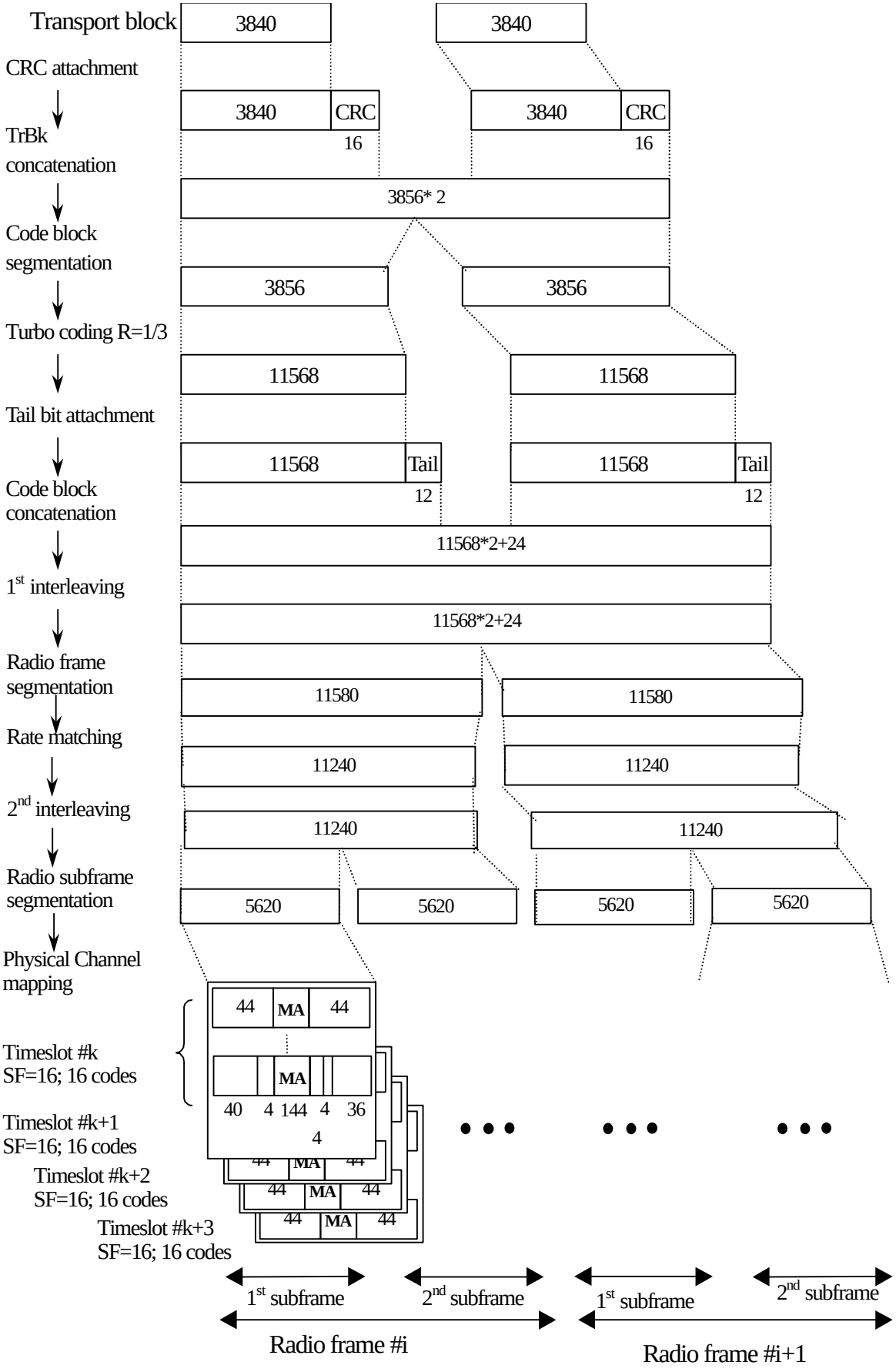


Figure B.4 Service mapping for 384kbps packet data

B.5 2Mbps packet data for downlink

In low chip rate TDD optional, 2Mbps service is only used in some special environment. E.g. Indoor environment

Table B.5 Parameter examples for 2Mbps packet data

Transport block size	20480*B bits(B=0,1)
CRC	24 bits
Coding	no
TTI	10 ms
Midamble	144 chips
Codes and time slots	SF = 1 1 codes x 5 time slots
TFCI	24bits
L1control signals	6bits

Note1: 8PSK has to be used to provide 2Mbps packet data service. B=1 for the figure B.5.
Note2: other mapping schemes, e.g. using more resource unit and using some channel coding, or increasing the number of the code block segmentation to reduce BLER are considered.

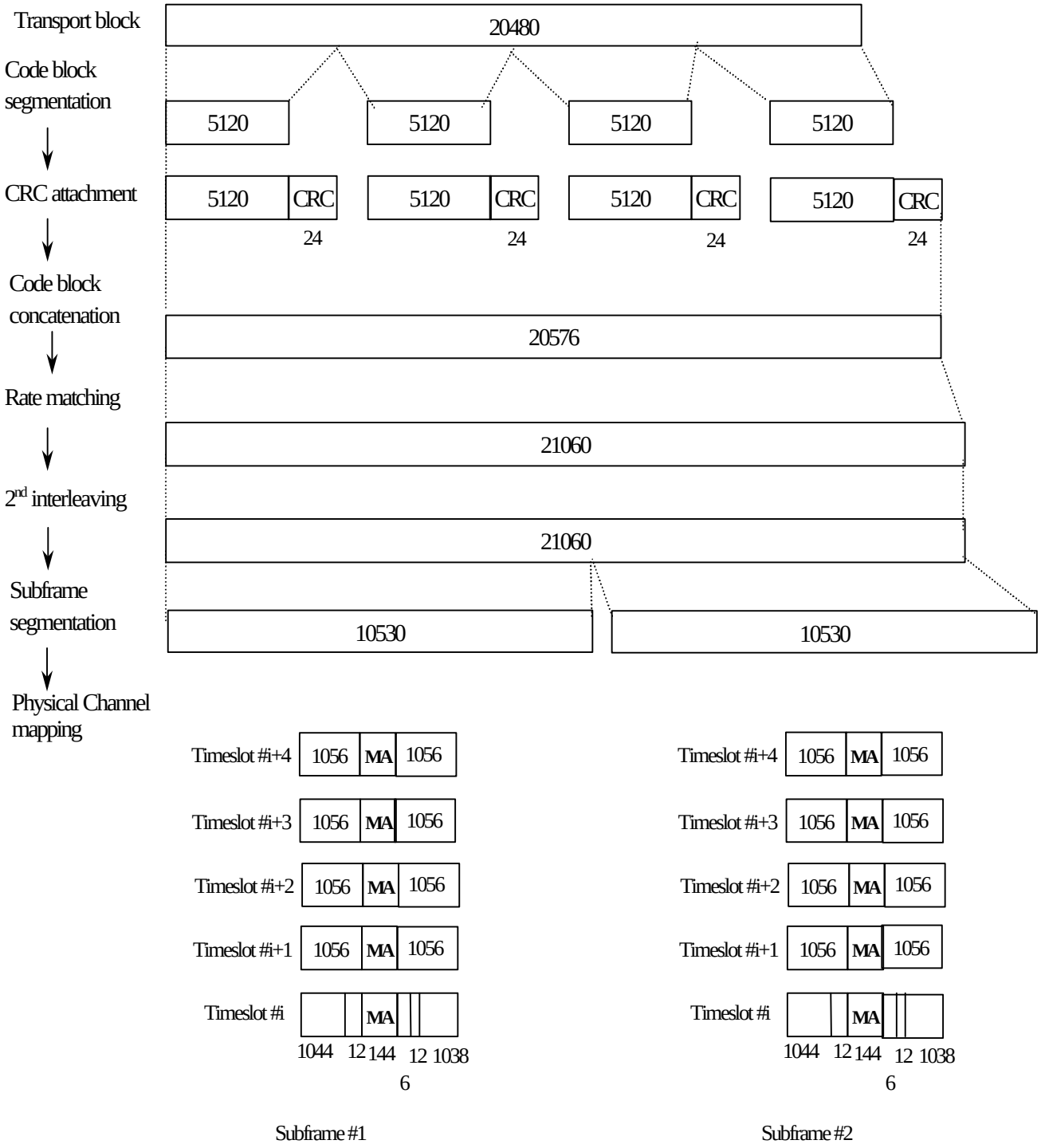


Figure B.5 Service mapping for 2Mbps packet data

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