TSG-RAN Working Group 1 meeting #12
Seoul, Korea, 10.-13. April 2000

TSGR1#12(00)0583

Agenda Item:

Source: Siemens

Title: TPC transmission for TDD

Document for: Approval

The current definition of the transmission of TPC bits is not consistent between differetn WGs:

- In WG1 specs the transmission of TPC bits is described as optional and negotiated at call setup
- In WG2 there is no such procedure as TPC negotiation or a TPC option. The TPC is mandatory.

It is proposed to remove the TPC bit option in WG1 specs and have a TPC bit mandatory in the PUSCH and UL DPCH. The reasons are as follows:

- TPC transmission has only very little impact on the system capacity
- The removal of the optional TPC bits simplifies the system. The number of burst types is significantly reduced
- Even at high speeds, the TPC bits give some indications for the power settings in the node B.

Furthermore, a typing error has been corrected in uplink burst type no. 99.

3GPP TSG RAN WG1 Meeting #12
Seoul, Korea, 10. –13. April 2000

Document R1-00-0583
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.221	CR	020r1	Current Version:	3.2.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	RAN#7	for approval	X	strategic		*(for SMG use only)*
List expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Siemens **Date:** 2000-04-04

Subject: TPC transmission for TDD

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	X	**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature			Release 97	
C	Functional modification of feature			Release 98	
D	Editorial modification			Release 99	X
				Release 00	

Reason for change: WG1 description has to be aligned with higher layer descriptions, TPC transmission should be mandatory for PUSCH and uplink DPCH

Clauses affected: 5.2.2.1, 5.2.2.2, 5.2.2.3

Other specs affected:

Other 3G core specifications		→ List of CRs:
Other GSM core specifications		→ List of CRs:
MS test specifications		→ List of CRs:
BSS test specifications		→ List of CRs:
O&M specifications		→ List of CRs:

Other comments:

help.doc

<--------- double-click here for help and instructions on how to create a CR.

5.2 Dedicated Physical Channel (DPCH)

5.2.2.1 Transmission of TFCI

Both burst types 1 and 2 provide the possibility for transmission of TFCI both in up- and downlink.

The transmission of TFCI is negotiated at call setup and can be re-negotiated during the call. For each CCTrCH it is indicated by higher layer signalling, which TFCI format is applied. Additionally for each allocated timeslot it is signalled individually whether that timeslot carries the TFCI or not.If a time slot contains the TFCI, then it is always transmitted using the first allocated channelisation code in the timeslot, according to the order in the higher layer allocation message.

The transmission of TFCI is done in the data parts of the respective physical channel, this means TFCI and data bits are subject to the same spreading procedure as depicted in [8]. Hence the midamble structure and length is not changed. The TFCI information is to be transmitted directly adjacent to the midamble, possibly after the TPC. Figure 6 shows the position of the TFCI in a traffic burst in downlink~~, if no TPC is transmitted~~. Figure 7 shows the position of the TFCI in a traffic burst in uplink~~, if TPC is transmitted~~.

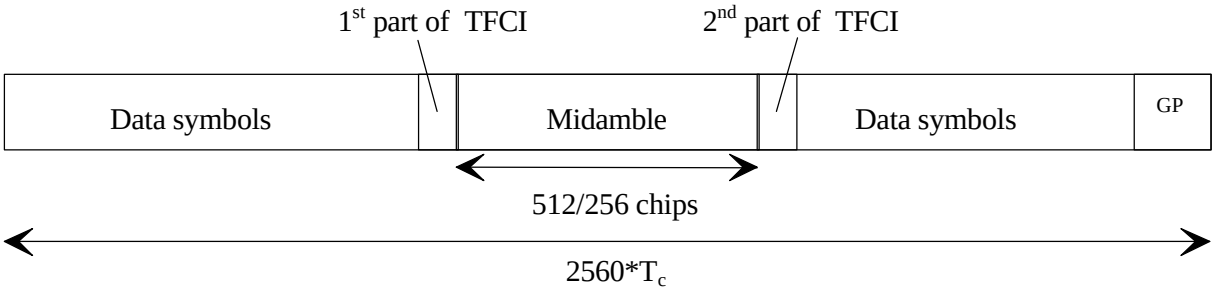

Figure 6: Position of TFCI information in the traffic burst in case of downlink~~no TPC~~

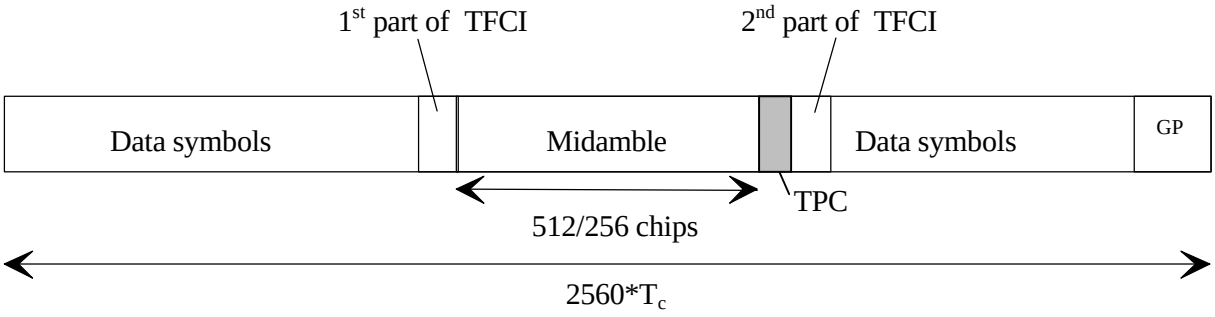

Figure 7: Position of TFCI information in the traffic burst in case of uplink ~~TPC~~

Two examples of TFCI transmission in the case of multiple DPCHs used for a connection are given in the Figure 8 and Figure 9 below. Combinations of the two schemes shown are also applicable. It should be noted that the SF can vary for the DPCHs not carrying TFCI information.

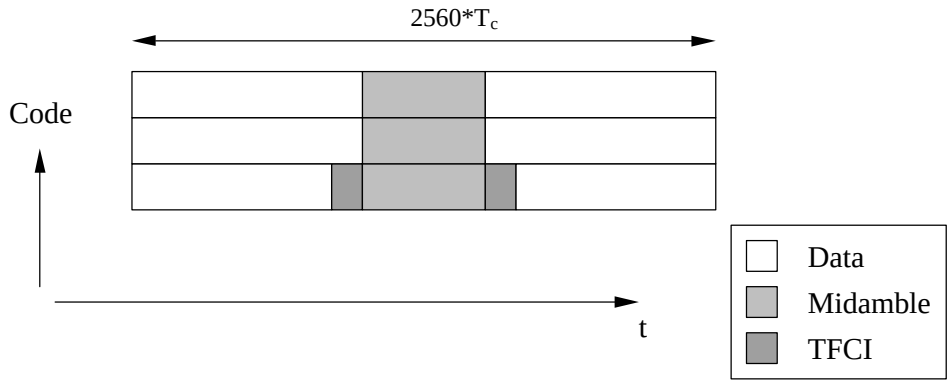

Figure 8: Example of TFCI transmission with physical channels multiplexed in code domain

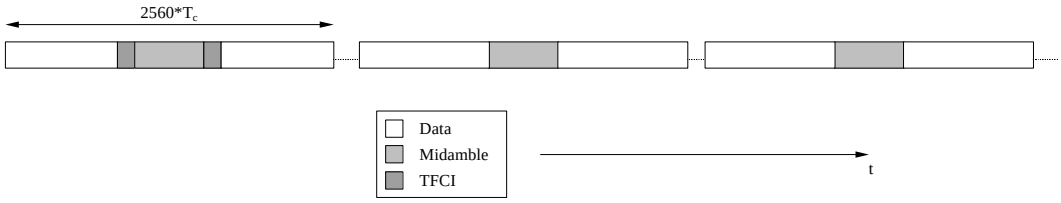

Figure 9: Example of TFCI transmission with physical channels multiplexed in time domain

5.2.2.2 Transmission of TPC

Both burst types 1 and 2 for dedicated channels provide the possibility for transmission of TPC in uplink.

~~The transmission of TPC is negotiated at call setup and can be re-negotiated during the call. If applied,~~The transmission of TPC is done in the data parts of the traffic burst. Hence the midamble structure and length is not changed. The TPC information is to be transmitted directly after the midamble. Figure 10 shows the position of the TPC in a traffic burst.

For every user the TPC information shall~~is to~~ be transmitted at least once per transmitted frame. If TFCI is applied for a CCTrCH, TPC shall be transmitted with the same channelization codes and in the same timeslots as TFCI. ~~If the TPC is applied, then i~~~~I~~If no TFCI is applied for a CCTrCH, TPC shall be~~is always~~ transmitted using the first allocated channelisation code and the first allocated timeslot, according to the order in the higher layer allocation message. The TPC is spread with the same spreading factor (SF) and spreading code as the data parts of the respective physical channel.

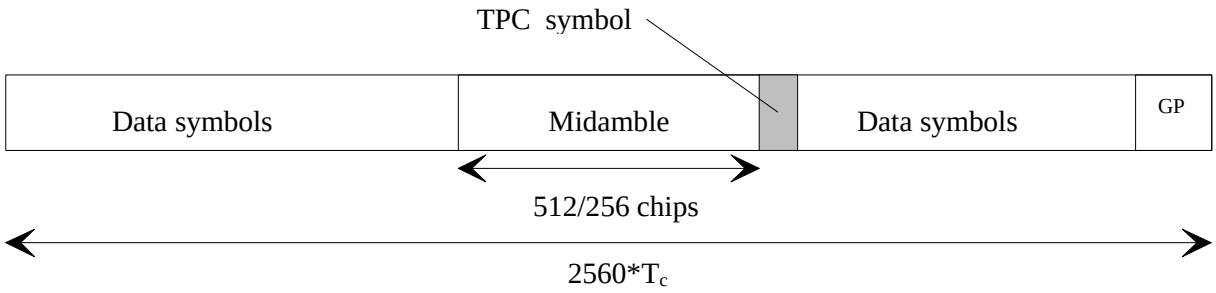

Figure 10: Position of TPC information in the traffic burst

5.2.2.3 Timeslot formats

5.2.2.3.1 Downlink timeslot formats

The downlink timeslot format depends on the spreading factor, midamble length and on the number of the TFCI bits, as depicted in the table 4a.

Table 4a: Time slot formats for the Downlink

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field}$ (bits)
0	16	512	0	244	244	122
1	16	512	4	244	240	120
2	16	512	8	244	236	118
3	16	512	16	244	228	114
4	16	512	32	244	212	106
5	16	256	0	276	276	138
6	16	256	4	276	272	136
7	16	256	8	276	268	134
8	16	256	16	276	260	130
9	16	256	32	276	244	122
10	1	512	0	3904	3904	1952
11	1	512	4	3904	3900	1950
12	1	512	8	3904	3896	1948
13	1	512	16	3904	3888	1944
14	1	512	32	3904	3872	1936
15	1	256	0	4416	4416	2208
16	1	256	4	4416	4412	2206
17	1	256	8	4416	4408	2204
18	1	256	16	4416	4400	2200
19	1	256	32	4416	4384	2192

5.2.2.3.2 Uplink timeslot formats

The uplink timeslot format depends on the spreading factor, midamble length~~, the TPC presence~~ and on the number of the TFCI bits. Due to TPC ~~In the case that TPC is used~~, different amount of bits are mapped to the two data fields. The timeslot formats are depicted in the table 4b.

Table 4b: Timeslot formats for the Uplink

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
0	16	512	0	0	244	244	122	122
~~1~~	~~16~~	~~512~~	~~4~~	~~0~~	~~244~~	~~240~~	~~120~~	~~120~~
~~2~~	~~16~~	~~512~~	~~8~~	~~0~~	~~244~~	~~236~~	~~118~~	~~118~~
~~3~~	~~16~~	~~512~~	~~16~~	~~0~~	~~244~~	~~228~~	~~114~~	~~114~~
~~4~~	~~16~~	~~512~~	~~32~~	~~0~~	~~244~~	~~212~~	~~106~~	~~106~~
5	16	512	0	2	244	242	122	120
6	16	512	4	2	244	238	120	118
7	16	512	8	2	244	234	118	116
8	16	512	16	2	244	226	114	112
9	16	512	32	2	244	210	106	104
10	16	256	0	0	276	276	138	138
~~11~~	~~16~~	~~256~~	~~4~~	~~0~~	~~276~~	~~272~~	~~136~~	~~136~~
~~12~~	~~16~~	~~256~~	~~8~~	~~0~~	~~276~~	~~268~~	~~134~~	~~134~~
~~13~~	~~16~~	~~256~~	~~16~~	~~0~~	~~276~~	~~260~~	~~130~~	~~130~~
~~14~~	~~16~~	~~256~~	~~32~~	~~0~~	~~276~~	~~244~~	~~122~~	~~122~~
15	16	256	0	2	276	274	138	136
16	16	256	4	2	276	270	136	134
17	16	256	8	2	276	266	134	132
18	16	256	16	2	276	258	130	128
19	16	256	32	2	276	242	122	120
20	8	512	0	0	488	488	244	244
~~21~~	~~8~~	~~512~~	~~4~~	~~0~~	~~488~~	~~484~~	~~242~~	~~242~~
~~22~~	~~8~~	~~512~~	~~8~~	~~0~~	~~488~~	~~480~~	~~240~~	~~240~~
~~23~~	~~8~~	~~512~~	~~16~~	~~0~~	~~488~~	~~472~~	~~236~~	~~236~~
~~24~~	~~8~~	~~512~~	~~32~~	~~0~~	~~488~~	~~456~~	~~228~~	~~228~~
25	8	512	0	2	488	486	244	242
26	8	512	4	2	488	482	242	240
27	8	512	8	2	488	478	240	238
28	8	512	16	2	488	470	236	234
29	8	512	32	2	488	454	228	226
30	8	256	0	0	552	552	276	276
~~31~~	~~8~~	~~256~~	~~4~~	~~0~~	~~552~~	~~548~~	~~274~~	~~274~~
~~32~~	~~8~~	~~256~~	~~8~~	~~0~~	~~552~~	~~544~~	~~272~~	~~272~~
~~33~~	~~8~~	~~256~~	~~16~~	~~0~~	~~552~~	~~536~~	~~268~~	~~268~~
~~34~~	~~8~~	~~256~~	~~32~~	~~0~~	~~552~~	~~520~~	~~260~~	~~260~~
35	8	256	0	2	552	550	276	274
36	8	256	4	2	552	546	274	272
37	8	256	8	2	552	542	272	270
38	8	256	16	2	552	534	268	266
39	8	256	32	2	552	518	260	258
40	4	512	0	0	976	976	488	488
~~41~~	~~4~~	~~512~~	~~4~~	~~0~~	~~976~~	~~972~~	~~486~~	~~486~~
~~42~~	~~4~~	~~512~~	~~8~~	~~0~~	~~976~~	~~968~~	~~484~~	~~484~~
~~43~~	~~4~~	~~512~~	~~16~~	~~0~~	~~976~~	~~960~~	~~480~~	~~480~~
~~44~~	~~4~~	~~512~~	~~32~~	~~0~~	~~976~~	~~944~~	~~472~~	~~472~~
45	4	512	0	2	976	974	488	486
46	4	512	4	2	976	970	486	484
47	4	512	8	2	976	966	484	482

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
48	4	512	16	2	976	958	480	478
49	4	512	32	2	976	942	472	470
50	4	256	0	0	1104	1104	552	552
~~51~~	~~4~~	~~256~~	~~4~~	~~0~~	~~1104~~	~~1100~~	~~550~~	~~550~~
~~52~~	~~4~~	~~256~~	~~8~~	~~0~~	~~1104~~	~~1096~~	~~548~~	~~548~~
~~53~~	~~4~~	~~256~~	~~16~~	~~0~~	~~1104~~	~~1088~~	~~544~~	~~544~~
~~54~~	~~4~~	~~256~~	~~32~~	~~0~~	~~1104~~	~~1072~~	~~536~~	~~536~~
55	4	256	0	2	1104	1102	552	550
56	4	256	4	2	1104	1098	550	548
57	4	256	8	2	1104	1094	548	546
58	4	256	16	2	1104	1086	544	542
59	4	256	32	2	1104	1070	536	534
60	2	512	0	0	1952	1952	976	976
~~61~~	~~2~~	~~512~~	~~4~~	~~0~~	~~1952~~	~~1948~~	~~974~~	~~974~~
~~62~~	~~2~~	~~512~~	~~8~~	~~0~~	~~1952~~	~~1944~~	~~972~~	~~972~~
~~63~~	~~2~~	~~512~~	~~16~~	~~0~~	~~1952~~	~~1936~~	~~968~~	~~968~~
~~64~~	~~2~~	~~512~~	~~32~~	~~0~~	~~1952~~	~~1920~~	~~960~~	~~960~~
65	2	512	0	2	1952	1950	976	974
66	2	512	4	2	1952	1946	974	972
67	2	512	8	2	1952	1942	972	970
68	2	512	16	2	1952	1934	968	966
69	2	512	32	2	1952	1918	960	958
70	2	256	0	0	2208	2208	1104	1104
~~71~~	~~2~~	~~256~~	~~4~~	~~0~~	~~2208~~	~~2204~~	~~1102~~	~~1102~~
~~72~~	~~2~~	~~256~~	~~8~~	~~0~~	~~2208~~	~~2200~~	~~1100~~	~~1100~~
~~73~~	~~2~~	~~256~~	~~16~~	~~0~~	~~2208~~	~~2192~~	~~1096~~	~~1096~~
~~74~~	~~2~~	~~256~~	~~32~~	~~0~~	~~2208~~	~~2176~~	~~1088~~	~~1088~~
75	2	256	0	2	2208	2206	1104	1102
76	2	256	4	2	2208	2202	1102	1100
77	2	256	8	2	2208	2198	1100	1098
78	2	256	16	2	2208	2190	1096	1094
79	2	256	32	2	2208	2174	1088	1086
80	1	512	0	0	3904	3904	1952	1952
~~81~~	~~1~~	~~512~~	~~4~~	~~0~~	~~3904~~	~~3900~~	~~1950~~	~~1950~~
~~82~~	~~1~~	~~512~~	~~8~~	~~0~~	~~3904~~	~~3896~~	~~1948~~	~~1948~~
~~83~~	~~1~~	~~512~~	~~16~~	~~0~~	~~3904~~	~~3888~~	~~1944~~	~~1944~~
~~84~~	~~1~~	~~512~~	~~32~~	~~0~~	~~3904~~	~~3872~~	~~1936~~	~~1936~~
85	1	512	0	2	3904	3902	1952	1950
86	1	512	4	2	3904	3898	1950	1948
87	1	512	8	2	3904	3894	1948	1946
88	1	512	16	2	3904	3886	1944	1942
89	1	512	32	2	3904	3870	1936	1934
90	1	256	0	0	4416	4416	2208	2208
~~91~~	~~1~~	~~256~~	~~4~~	~~0~~	~~4416~~	~~4412~~	~~2206~~	~~2206~~
~~92~~	~~1~~	~~256~~	~~8~~	~~0~~	~~4416~~	~~4408~~	~~2204~~	~~2204~~
~~93~~	~~1~~	~~256~~	~~16~~	~~0~~	~~4416~~	~~4400~~	~~2200~~	~~2200~~
~~94~~	~~1~~	~~256~~	~~32~~	~~0~~	~~4416~~	~~4384~~	~~2192~~	~~2192~~
95	1	256	0	2	4416	4414	2208	2206
96	1	256	4	2	4416	4410	2206	2204
97	1	256	8	2	4416	4406	2204	2202

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} (bits)	N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
98	1	256	16	2	4416	4398	2200	2198
99	1	256	32	2	4416	4382	2192	2190