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Title: Node B Synchronization over the Air:
A purely analytical verification of Tdoc R1-00-0074 simulation results.
Document for: Discussion

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1 Introduction

This contribution provides a purely analytical view of the simulation results of reference [3]Node B synchronisation for TDD, Siemens, TSGR1#10(00)0074, Beijing, China, January 18-21 2000.

While simulation is essential for concept verification, we believe that the use of purely analytical reasoning (rather than simply using simulation results) is useful to help us understand the cause and effect relationships that affect the node B synchronization process.

It will be seen that the key simulation results are directly explained by basic physical principles and closed form mathematical expressions.

2 Performance analysis

This section explains the performance of the synchronization process and illustrates that we can predict the simulation results shown in reference [3]. For convenience, we have reproduced the table of assumed parameters and the figure from that reference .

2.1 Summary of Assumptions and results of Reference 3

Parameter	Value
Initial Timing Error	Uniform Random Distribution over ± 50 ms
Initial Clock Rate Error	Uniform Random Distribution over ± 0.050 ppm
Measurement Resolution	¼ chip
Clock Variance	10^{-17}sec^2/sec
Timing Measurement Window	768000 chips about correct position
Clock Update Coefficient	20% of Measurement

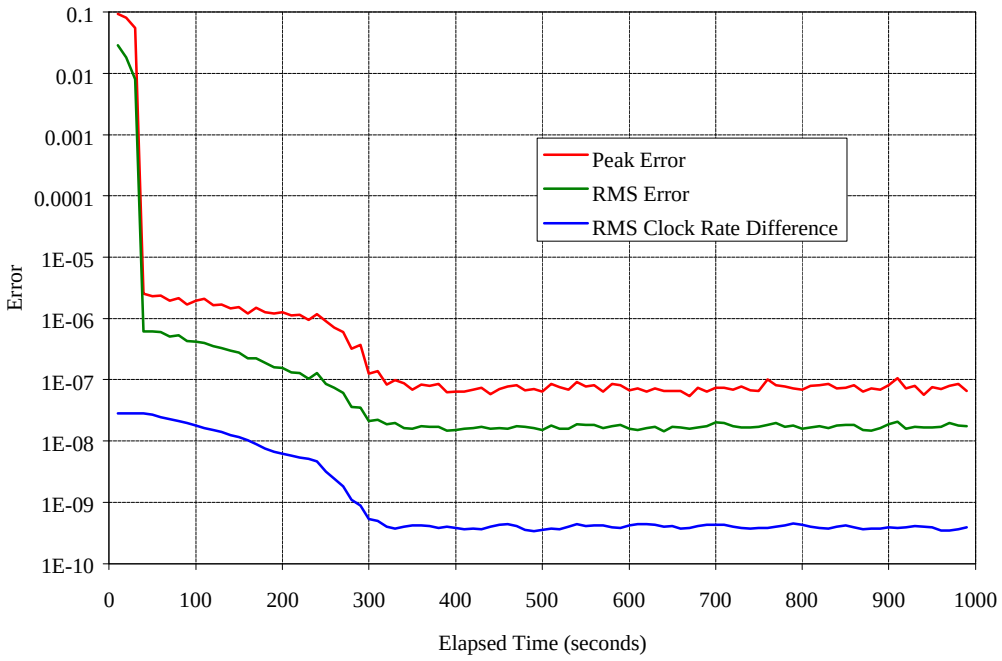

Figure 1 Sync Settling Performance

From the figure, we obtain the following data points:

Initial time error
- RMS .03 = 30 millisec
- Worst Case 0.1 = 100 millisec

After (about)40seconds
- RMS = 6.4 10-7 =0.64 microsec
- Worst Case = 2.5 microsec

After 300 seconds (steady state)
- RMS = 1.7 10-8 = .017 microsec
- Worst Case =10-7 = 0.1 microsec

2.2 Explanation

The Initial time error was shown to be:
- RMS .028 = 28 millisec
- Worst Case 0.1 = 100 millisec

Since the model assumed an intial timing error of +/- 50 millisec for each Node B with respect to the correct time, then the worst case mismatch is 2 * 50 = 100 millisec.

For a uniform distribution the mean of the difference is 0 and the standard deviation is 50/sqrt(2) = 28.8

After (about)40seconds
- RMS = 6.4 10-7 =0.64 microsec
- Worst Case = 2.5 microsec

The system is now in a state where the time difference is corrected after each measurement, but the drift rate has not yet been estimated. Therefore, the time difference error is on the order of 1 chip due to measurement accuracy immediately after a measurement, but the two time references drift apart in the interval before the next measurment.

Using initial clock rate error equal to a Uniform Random Distribution over ± 0.050 ppm, we can predict the drift variance to be sqrt (2)*(.05 10-6)* sqrt(20) = 0.32 microsec.

The contribution due to measurement accuracy needs careful evaluation. However, it is plausible to assume that it would contribute equally to the errors and the result would be the simulation result of 0.64 microsec

After 300 seconds (steady state)

- RMS = 1.7 10-8 = .017 microsec
- Worst Case =10-7 = 0.1 microsec

In this region, assume that the timing measurements have been averaged and the drift rates have been estimated. To a first approximation, assume that the time measurements are perfect. The dominant error in time diffference is due to the random (and unpredictable) short term drift, modeled by Reference [3] as $10^{-17}sec^2/sec$. Note that Siemens has stated in offline discussions that this clock model needs review.

After 20 seconds this value is $20sec \times 10^{-17}sec^2/sec = 2 \times 10^{-16}sec^2$.
Since two clocks are drifting, the variance of the difference between them is twice as large, but averaging over the full interval, we would divide by 2.

Taking the square root, sigma = .014 microsec.
The worst case would be on the order of 2 x 3 sigma = 6 sigma = approximately 1 microsecond.

This is very close to the simulation results, which would also include a small component for the impact of measurement errors. It appears that the measurement error is on the order of 1/4 chip accuracy.

3 Conclusion

We have reviewed the simulation results of reference [3] and have found them to be very much consistent with results obtained through the use of several simplifying assumptions and a "pencil and paper" analysis. We hope that the insights accompanying this exercise will be usefull as we progress in the Node B Synchronization Work Item.

4 References

[1] Synchronization of TDD Cells, TSGR3#6(99)905, Sophia Antipolis, France,August 23-27, 1999, InterDigital Comm. Corp.

[2] NBAP & RNSAP Procedure for TDD Synchronization (some additions/modifications to R3-99905)TSGR3#6(99) 882, Italtel / Siemens, August 23rd 1999,Sophia Antipolis, France

[3]Node B synchronisation for TDD, Siemens, TSGR1#10(00)0074, Beijing, China, January 18-21 2000

[4] Synchronisation of Node B's in TDD via Selected PRACH Time Slots, Siemens, TSG RAN WG1 (99)G42, New York, USA, October 12 - 15, 1999