3GPP TSG RAN WG1#11 **_TSGR1#11-00-0232_**

San Diego, USA, Feb. 29th – March 3rd, 2000

**Agenda Item : 8**

**Source : LG Information & Communications, Ltd.**

**Title : Properties of FSWs**

**Document for : FYI and discussion**

## Abstract

In this document, the properties of Frame Synchronization Words (FSWs) in pilot bit pattern is discussed. The FSWs in based on the maximal length sequence and shows the ideal property for synchronization detection. This contribution also shows the usefulness of FSWs in compressed mode.

## 1. Property of frame synchronization words

Frame synchronization words (FSWs) are shadowed part of the column pilot bit patterns of uplink DPCH, downlink DPCH, and SCCPCH [1]. This FSWs are also used for RACH message part, CPCH power control preamble part, and CPCH message part [2].

Table 1. New frame synchronization words

| Frame Synchronization Words |
| --- |
| $C_{FSW,1}$ = (1 0 0 0 1 1 1 1 0 1 0 1 1 0 0) |
| $C_{FSW,2}$ = (1 0 1 0 0 1 1 0 1 1 1 0 0 0 0) |
| $C_{FSW,3}$ = (1 1 0 0 0 1 0 0 1 1 0 1 0 1 1) |
| $C_{FSW,4}$ = (0 0 1 0 1 0 0 0 0 1 1 1 0 1 1) |
| $C_{FSW,5}$ = (1 1 1 0 1 0 1 1 0 0 1 0 0 0 1) |
| $C_{FSW,6}$ = (1 1 0 1 1 1 0 0 0 0 1 0 1 0 0) |
| $C_{FSW,7}$ = (1 0 0 1 1 0 1 0 1 1 1 1 0 0 0) |
| $C_{FSW,8}$ = (0 0 0 0 1 1 1 0 1 1 0 0 1 0 1) |

The proposed 8 frame synchronization words have the following two-valued auto-correlation function:

$$R_i(t) = \begin{cases} 15, & t = 0 \\ -1, & t \neq 0 \end{cases}, \quad i = 1,2,\cdots,8 \qquad (1)$$

where $R_i(t)$ is the auto-correlation function of frame synchronization word $C_{FSW,i}$.

Now classify the words of table 1 as follows:

E = {$C_{FSW,1}$, $C_{FSW,2}$}
F = {$C_{FSW,3}$, $C_{FSW,4}$}
G = {$C_{FSW,5}$, $C_{FSW,6}$}
H = {$C_{FSW,7}$, $C_{FSW,8}$}

We call two words within the same class preferred pair. The cross-correlation spectrum for the preferred pair {$C_{FSW,1}$, $C_{FSW,2}$}, {$C_{FSW,3}$, $C_{FSW,4}$}, {$C_{FSW,5}$, $C_{FSW,6}$}, or {$C_{FSW,7}$, $C_{FSW,8}$} is

$$R_{i,j}(t) = \begin{cases} -15, & t = 7 \\ 1, & t \neq 7 \end{cases} \qquad (2)$$

$$R_{j,i}(t+1)=\begin{cases}-15, & t=7\\ 1, & t\neq 7\end{cases} \quad (3)$$

where $R_{i,j}(t)$ is cross-correlation function between two codes of preferred pair of E, F, G, H, and $i, j = 1,2,\cdots,8$. Thus combining such auto-correlation and cross-correlation functions, we obtain the following:

$$\sum_{i=1}^{a} R_i(t)=\begin{cases}a\cdot 15, & t=0\\ -a, & t\neq 0\end{cases}, \quad a=1,2,3,\ldots,8 \quad (4)$$

$$\sum_{i=1}^{a/2}(R_{2i-1,2i}(t)+R_{2i,2i-1}(t+1))=\begin{cases}-a\cdot 15, & t=7\\ a, & t\neq 7\end{cases}, \quad a=2,4,6,8 \quad (5)$$

From (4) and (5), we obtain figure 1 when $a = 2$.

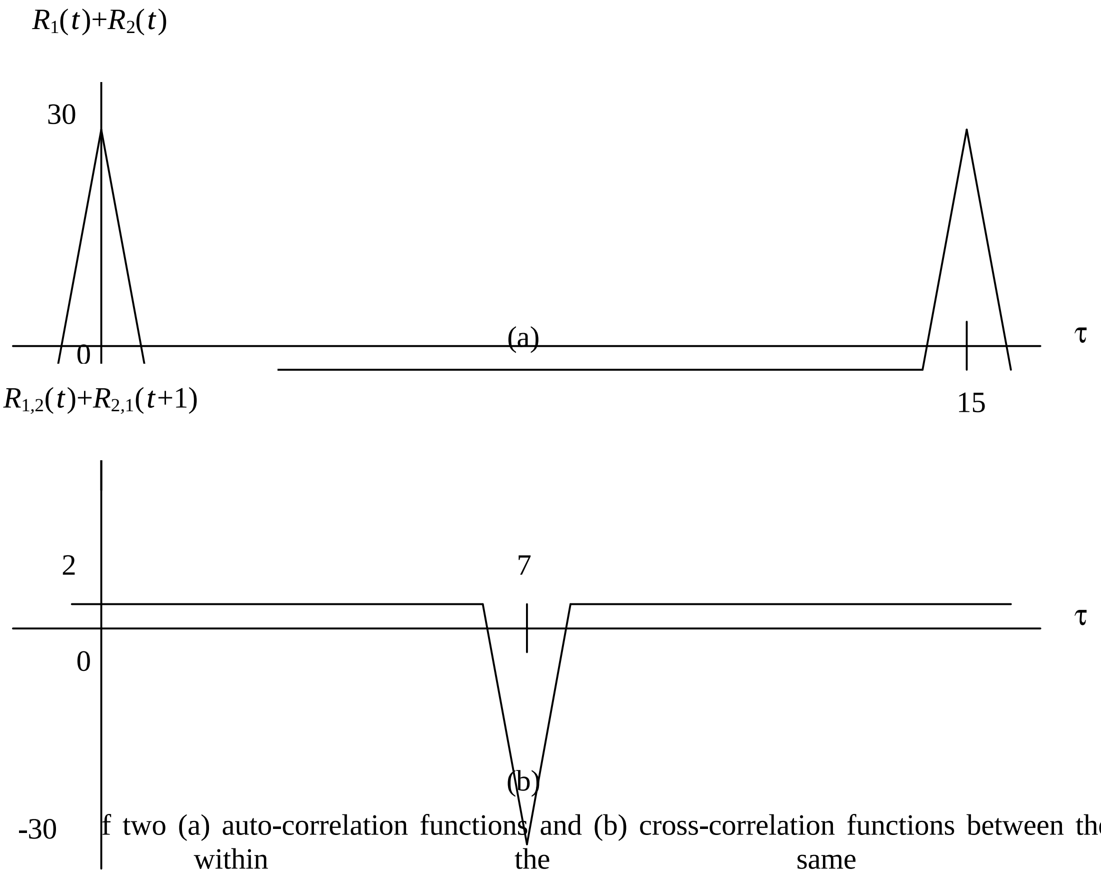


Fig. 1. Ac f two (a) auto-correlation functions and (b) cross-correlation functions between the two codes within the same class.

# 2. Frame synchronization words

## 2.1. Uplink DPCCH

The pilot bit pattern is described in table 2 and table 3. The shadowed part of column pilot bit pattern is defined as frame synchronization word and FSWs can be used to confirm frame synchronization (The value of the pilot bit patterns other than the frame synchronization words shall be "1".)

**Table 2: Pilot bit patterns for uplink DPCCH with $N_{pilot}$ = 3, 4, 5 and 6**

| | $N_{pilot}$ = 3 | | | $N_{pilot}$ = 4 | | | | $N_{pilot}$ = 5 | | | | | $N_{pilot}$ = 6 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit # | 0 | 1 | 2 | 0 | 1 | 2 | 3 | 0 | 1 | 2 | 3 | 4 | 0 | 1 | 2 | 3 | 4 | 5 |
| Slot #0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 2 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 4 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 5 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 6 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 7 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 8 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 9 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 10 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 11 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 12 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 13 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 14 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

**Table 3: Pilot bit patterns for uplink DPCCH with $N_{pilot}$ = 7 and 8**

| | $N_{pilot}$ = 7 | | | | | | | $N_{pilot}$ = 8 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit # | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Slot #0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 2 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 3 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 4 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 5 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 6 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 7 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 8 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 9 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 10 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 11 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 12 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 13 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 14 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

Table 4. Mapping relationship between the FSWs of table 1 and shadowed part of Column pilot bit patterns of table 3 and 4 on uplink DPCCH

| $N_{pilot}$ | Bit # | Corresponding column Pilot bit pattern of length 15 (FSW) |
|---|---|---|
| 3 | 0 | $C_{FSW,1}$ |
| | 1 | $C_{FSW,2}$ |
| 4 | 1 | $C_{FSW,1}$ |
| | 2 | $C_{FSW,2}$ |
| 5 | 0 | $C_{FSW,1}$ |
| | 1 | $C_{FSW,2}$ |
| | 3 | $C_{FSW,3}$ |
| | 4 | $C_{FSW,4}$ |
| 6 | 1 | $C_{FSW,1}$ |
| | 2 | $C_{FSW,2}$ |
| | 4 | $C_{FSW,3}$ |
| | 5 | $C_{FSW,4}$ |
| 7 | 1 | $C_{FSW,1}$ |
| | 2 | $C_{FSW,2}$ |
| | 4 | $C_{FSW,3}$ |
| | 5 | $C_{FSW,4}$ |
| 8 | 1 | $C_{FSW,1}$ |
| | 3 | $C_{FSW,2}$ |
| | 5 | $C_{FSW,3}$ |
| | 7 | $C_{FSW,4}$ |

## 2.1. Downlink DPCCH

The pilot bit patterns are described in table 5. The shadowed part of column pilot bit pattern is defined as frame synchronization word and FSWs can be used to confirm frame synchronization. (The pilot bit pattern other than FSWs shall be "11".) In table 5, the transmission order is from left to right. (Each two-bit pair represents an I/Q pair of QPSK modulation.)

In downlink compressed mode through spreading factor reduction, the number of bits in the TPC and Pilot fields are doubled. Symbol repetition is used to fill up the fields. Denote the bits in one of these fields in normal mode by $x_1$, $x_2$, $x_3$, …, $x_X$. In compressed mode the following bit sequence is sent in corresponding field: $x_1$, $x_2$, $x_1$, $x_2$, $x_3$, $x_4$, $x_3$, $x_4$,…,

**Table 5: Pilot bit patterns for downlink DPCCH with $N_{pilot}$ = 2, 4, 8 and 16**

| | $N_{pilot}$ = 2 | $N_{pilot}$ = 4 | | $N_{pilot}$ = 8 | | | | $N_{pilot}$ = 16 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol # | 0 | 0 | 1 | 0 | 1 | 2 | 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Slot #0 | 11 | 11 | 11 | 11 | 11 | 11 | 10 | 11 | 11 | 11 | 10 | 11 | 11 | 11 | 10 |
| 1 | 00 | 11 | 00 | 11 | 00 | 11 | 10 | 11 | 00 | 11 | 10 | 11 | 11 | 11 | 00 |
| 2 | 01 | 11 | 01 | 11 | 01 | 11 | 01 | 11 | 01 | 11 | 01 | 11 | 10 | 11 | 00 |
| 3 | 00 | 11 | 00 | 11 | 00 | 11 | 00 | 11 | 00 | 11 | 00 | 11 | 01 | 11 | 10 |
| 4 | 10 | 11 | 10 | 11 | 10 | 11 | 01 | 11 | 10 | 11 | 01 | 11 | 11 | 11 | 11 |
| 5 | 11 | 11 | 11 | 11 | 11 | 11 | 10 | 11 | 11 | 11 | 10 | 11 | 01 | 11 | 01 |
| 6 | 11 | 11 | 11 | 11 | 11 | 11 | 00 | 11 | 11 | 11 | 00 | 11 | 10 | 11 | 11 |
| 7 | 10 | 11 | 10 | 11 | 10 | 11 | 00 | 11 | 10 | 11 | 00 | 11 | 10 | 11 | 00 |
| 8 | 01 | 11 | 01 | 11 | 01 | 11 | 10 | 11 | 01 | 11 | 10 | 11 | 00 | 11 | 11 |
| 9 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 00 | 11 | 11 |
| 10 | 01 | 11 | 01 | 11 | 01 | 11 | 01 | 11 | 01 | 11 | 01 | 11 | 11 | 11 | 10 |
| 11 | 10 | 11 | 10 | 11 | 10 | 11 | 11 | 11 | 10 | 11 | 11 | 11 | 00 | 11 | 10 |
| 12 | 10 | 11 | 10 | 11 | 10 | 11 | 00 | 11 | 10 | 11 | 00 | 11 | 01 | 11 | 01 |
| 13 | 00 | 11 | 00 | 11 | 00 | 11 | 11 | 11 | 00 | 11 | 11 | 11 | 00 | 11 | 00 |
| 14 | 00 | 11 | 00 | 11 | 00 | 11 | 11 | 11 | 00 | 11 | 11 | 11 | 10 | 11 | 01 |

NOTE: In compressed mode through spreading factor reduction, symbol repetition is applied to the symbol patterns described in this table.

Table 6 : Mapping relationship between FSWs of table 1 and shadowed part of column pilot bit patterns of table 5 with $N_{pilot}$ = 2, 4, 8, and 16.

| $N_{pilot}$ | Symbol # | I/Q | Corresponding column pilot bit pattern of length 15 |
|---|---|---|---|
| $N_{pilot} = 2$ | 0 | I | $C_{FSW,1}$ |
| | | Q | $C_{FSW,2}$ |
| $N_{pilot} = 4$ | 1 | I | $C_{FSW,1}$ |
| | | Q | $C_{FSW,2}$ |
| $N_{pilot} = 8$ | 1 | I | $C_{FSW,1}$ |
| | | Q | $C_{FSW,2}$ |
| | 3 | I | $C_{FSW,3}$ |
| | | Q | $C_{FSW,4}$ |
| $N_{pilot} = 16$ | 1 | I | $C_{FSW,1}$ |
| | | Q | $C_{FSW,2}$ |
| | 3 | I | $C_{FSW,3}$ |
| | | Q | $C_{FSW,4}$ |
| | 5 | I | $C_{FSW,5}$ |
| | | Q | $C_{FSW,6}$ |
| | 7 | I | $C_{FSW,7}$ |
| | | Q | $C_{FSW,8}$ |

# 3. Relationship between FSWs

The pilot patterns are designed based on the 8 FSWs of table 1. The FSWs are classified as follows:

$$E = \{C_{FSW,1}, C_{FSW,2}\}$$
$$F = \{C_{FSW,3}, C_{FSW,4}\}$$
$$G = \{C_{FSW,5}, C_{FSW,6}\}$$
$$H = \{C_{FSW,7}, C_{FSW,8}\}$$

We see the following relationships exist between two FSWs in the same class E, F, G, and H.

$$C_{FSW,i,j} = -C_{FSW,i+1,(j+7)\bmod 15} \quad (6)$$

$$C_{FSW,i+1,j} = -C_{FSW,i,(j+8)\bmod 15} \quad (7)$$

where $i = 1,3,5,7$ and $j = 0,1,2,\cdots,14$.

## 3.1. Uplink DPCCH

There are two possible compressed slot formats for each normal slot format. They are labeled A and B and the selection between them is dependent on the number of slots that are transmitted in each frame in compressed mode [2].

In the uplink DPCH compressed mode, (6) and (7) enable us to obtain the property of Fig. 1 using FSWs.

## 3.2. Downlink DPCCH

In compressed mode, a different slot format is used compared to normal mode. There are two possible compressed slot formats that are labeled A and B. Format B is used for compressed mode by spreading factor reduction and format A is used for all other transmission time reduction methods [2].

In the downlink DPCCH compressed mode of format A and B, (6) and (7) enable us to obtain the property of Fig. 1 using FSWs

## References

[1] LGIC, “New pilot patterns for 15 slots considering Harmonization”, TSGR1#6(99)829.

[2] “UTRA FDD ; Physical channels and mapping of transport channels onto physical channels”, 3GPP TS25.211 V3.1.1 (1999-12).