**3GPP TSG RAN WG1 Meeting #108-e R1-2202503**

**e-Meeting, February 21 – March 03, 2022**

**Source: Moderator (Intel Corporation)**

**Title: Summary #2 of email discussion on initial access aspect of NR extension up to 71 GHz**

**Agenda item: 8.2.1**

**Document for: Discussion**

# Introduction

In this contribution, moderator summarizes discussions on remaining issues related to initial access for extending NR up to 71 GHz based submitted contributions from RAN1 #108-e.

# Summary of issues

## 2.1 DBTW Application & SSB-PositionQCL signaling in SSB

* From [1] Huawei/HiSilicon:
  + Aligned with the previous RAN1 agreements, indication of ={32,64} in MIB is supported using subCarrierSpacingCommon for 120, 480 and 960 kHz SCS
  + The Note “UE is expected to be configured with =64 in licensed operations” in the agreement in RAN1#107-e is captured in 38.213 by one of the following alternatives:
    - ALT 1: “For operation without shared spectrum channel access in FR2-2, UE assumes =64 and expects that the same value for is indicated in a MIB provided by a SS/PBCH block”.
      * Adopt TP#1-1 in Section 4.1 of TS 38.213.
    - ALT 2: “For operation without shared spectrum channel access in FR2-2, UE expects subCarrierSpacingCommon = ‘scs30or120’ from a MIB provided by a SS/PBCH block.”
      * Adopt TP#1-1A in Section 4.1 of TS 38.213.
* From [2] Futurewei:
  + For the second bit to indicate select one of the following options:
    - Option 1: For FR2-2 use the MSB of the controlResourceSetZero to encode as follows:

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| --- | --- | --- |
| *subCarrierSpacingCommon* | MSB of *controlResourceSetZero* |  |
| scs15or60 | 0 | 8 |
| scs15or60 | 1 | 16 |
| scs30or120 | 0 | 32 |
| scs30or120 | 1 | 64 |

* + - Option 2: For FR2-2 use as a second bit for signaling the least significant bit (LSB) of ssb-SubcarrierOffset.

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| --- | --- | --- |
| *subCarrierSpacingCommon* | LSB of *ssb-SubcarrierOffset* |  |
| scs15or60 | 0 | 8 |
| scs15or60 | 1 | 16 |
| scs30or120 | 0 | 32 |
| scs30or120 | 1 | 64 |

* From [3] Interdigital
  + For SSB blocks in the frequency beyond 52.6GHz, use the index associated to the DMRS in PBCH () as a means of indication for Q parameter in addition to the license regime.
  + The DBTW only applies to operation with shared spectrum channel access.
    - The indication of should not be used in operation without shared spectrum channel access.
* From [4] vivo
  + Support to use only ‘subCarrierSpacingCommon’ to indicate the which value are {32, 64}
  + DBTW is not applied to licensed band and Adopt TP #1-2 in section 4.1 for TS 38.213.
* From [5] OPPO
  + Support 1-bit for Q indication.
  + Support indication of Q = {32, 64}.
  + TP #1-1B
  + UE should be made aware of operation in licensed band or unlicensed band after reading SIB1 via either implicit association with other indication, e.g. LBT mode indication, or explicit indication.
  + UE does not need to expect Q=64 for licensed operation
  + UE assumes there is no DBTW for operation in licensed band.
* From [6] CATT
  + For cid:image001.png@01D7C5AC.DAEE0E00only 2 values {32, 64} are supported since, only 1 bit is available
* From [7] ZTE/Sanechips
  + Revisit the previous agreements of candidate values and indication bits for and support the following methods:
    - reduce the candidate values of and only support {32, 64} for
    - use one bit to indicate : SubcarrierSpacingCommon in MIB
  + For candidate values and indication bits for , adopt TP#1-1C in TS 38.213.
  + To solve inconsistencies between RAN1’s agreements and 38.213 V17.0.0, for operation without shared spectrum channel access, RAN1 should
    - not support DBTW
    - not define
    - clarify the configuration of subCarrierSpacingCommon in the spec to avoid error case
  + For the configuration of subCarrierSpacingCommon, adopt TP#1-2 in TS 38.213 for operation without shared spectrum channel access.
* From [8] NTT Docomo
  + Adopt the following TP#1-1D (i.e., support only 1 bit in MIB indicating Q)
    - If the following is not acceptable in RAN1 in this e-meeting, support to postpone this discussion as well as the one for RB offset between SSB and CORESET#0
  + Adopt the following TP#1-2B to TS38.213 when only 1 bit of subCarrierSpacingCommon is supported for Q indication in MIB.
* From [9] Spreadtrum
  + Confirm the working assumption to use 2 bits for Q values, including SbucarrierSpacingCommon and other additional bit.
  + The reserved codepoint for Q value indication can be used to distinguish the operation in licensed operation and the operation with the short control signalling in unlicensed operation.
* From [11] Nokia/NSB
  + Limit the supported values to {32,64}.
  + Adopt TP#1-2 to Section 4.1 of TS 38.213
* From [12] Intel
  + Working assumption: Use 2 bits for : subcarrierSpacingCommon and 1 bit borrowed from indication.
  + Send an LS to RAN4 for confirming borrowing 1 bit from field of MIB.
* From [13] Ericsson
  + Agree on TP#1-2
  + For operation with shared spectrum channel access, use 1 bit to signal Q (subCarrierSpacingCommon) with the value range for Q = {32, 64}. Update RRC parameter list to reflect this and remove spare from 38.213 according to TP#1-1E (below).
* From [14] Apple
  + Using 1-bit subCarrierSpacingCommon field in MIB to indicate one from <32,64> for .
  + RAN1 to conclude that the DBTW operation is not applicable for licensed band.
  + Adopt TP#1-1F and 1-2 to add the following into clause 4.1 of TS 38.213
    - For operation without shared spectrum channel access in FR2-2, a UE is expected to configure with Q= 64, i.e., subCarrierSpacingCommon = ‘scs30or120’.
* From [15] NEC
  + DBTW should not be supported for licensed operations, i.e. DBTW is disabled in licensed operations.
  + For the value set of Q, {16, 32, 64} should be supported without other additional value.
  + For the indication of Q value and related information in MIB, the subCarrierSpacingCommon and 1 bit from pdcch-ConfigSIB1 should be used.
* From [16] Samsung
  + No need to support DBTW for licensed operation in FR2-2.
    - No specification impact.
  + Down-select one option for the indication of :
    - Option 1: Keep using 2 bits in MIB for the indication of , and send a LS to RAN4 for confirming the use of the LSB of ssb-SubcarrierOffset. Adopt TP#1-1G for TS 38.213.
    - Option 2: Use 1 bit in MIB for the indication of . Adopt TP#1-1H for TS 38.213.
    - Option 3: Don’t indicate in MIB. Adopt TP#1-1I for TS 38.213.
* From [17] Qualcomm
  + for 120/480/960 kHz SCS, consider using only 1 bit in MIB to indicate the , where:
    - ∈ {32, 64}
    - ‘subCarrierSpacingCommon’ is used to signal the 1 bit for
  + Adopt TP#1-1J
  + Adopt TP#1-2F
* From [18] Sharp
  + Use 1 MIB payload bit to partially indicate Q values of {16, 32, 64} and the full indication for Q can be complemented by SIB1. Adopt the following text proposal #1-1K.
* From [19] LG Electronics
  + Use 1 bit (i.e., SubcarrierSpacingCommon) in MIB for indicating values.
  + The value range of is {32, 64}.
  + Adopt TP#1-1L

**TP# 1-1 for TS38.213 [1]**

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| ===========Start of TP#1 for TS 38.213 ===========  4.1 Cell search  \*\*\* unchanged part omitted \*\*\*  For operation without shared spectrum channel access, an SS/PBCH block index is same as a candidate SS/PBCH block index.  \*\*\* unchanged part omitted \*\*\*  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  For operation without shared spectrum channel access in FR2-2, UE assumes =64 and expects that the same value for is indicated in a MIB provided by a SS/PBCH block.  Table 4.1-2: Mapping of *subCarrierSpacingCommon*  to for operation with and without shared spectrum channel access in FR2-2   |  |  | | --- | --- | | *subCarrierSpacingCommon* |  | |  |  | | scs15or60 | 32 | | scs30or120 | 64 | |  |  |   \*\*\* unchanged part omitted \*\*\*  ===========End of TP#1 for TS 38.213 =========== |

**TP# 1-1A for TS38.213 [1]**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ===========Start of TP#1A for TS 38.213 ===========  4.1 Cell search  \*\*\* unchanged part omitted \*\*\*  For operation without shared spectrum channel access, an SS/PBCH block index is same as a candidate SS/PBCH block index.  \*\*\* unchanged part omitted \*\*\*  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  For operation without shared spectrum channel access in FR2-2, a UE expects *subCarrierSpacingCommon* = ‘*scs30or120’* from a *MIB* provided by a SS/PBCH block.  Table 4.1-2: Mappingof *subCarrierSpacingCommon* to for operation with shared spectrum channel access in FR2-2   |  |  | | --- | --- | | *subCarrierSpacingCommon* |  | |  |  | | scs15or60 | 32 | | scs30or120 | 64 | |  |  |   \*\*\* unchanged part omitted \*\*\*  ===========End of TP#1A for TS 38.213 =========== |

**TP# 1-1B for TS38.213 [5]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| <Unchanged parts are omitted>  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  **Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* and *spare* to for operation with shared spectrum channel access in FR2-2**   |  |  |  | | --- | --- | --- | | ***subCarrierSpacingCommon*** | ***~~spare~~*** |  | | ~~scs15or60~~ | ~~0~~ | ~~16~~ | | scs15or60 | ~~1~~ | 32 | | scs30or120 | ~~0~~ | 64 | | ~~scs30or120~~ | ~~1~~ | ~~reserved~~ |   <Unchanged parts are omitted> |

**TP# 1-1C for TS38.213 [7]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| 4 Synchronization procedures  4.1 Cell search  < Unchanged parts are omitted >  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  Table 4.1-2: Mapping between ~~the combination of~~ *subCarrierSpacingCommon* ~~and~~ *~~spare~~* to for operation with shared spectrum channel access in FR2-2   |  |  |  | | --- | --- | --- | | *subCarrierSpacingCommon* | *~~spare~~* |  | | ~~scs15or60~~ | ~~0~~ | ~~16~~ | | scs15or60 | ~~1~~ | 32 | | scs30or120 | ~~0~~ | 64 | | ~~scs30or120~~ | ~~1~~ | ~~reserved~~ |   < Unchanged parts are omitted > |

**TP# 1-1D for TS38.213 [8]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| 4.1 Cell search  **[Unchanged Part Omitted]**  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  **Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* and *spare* to for operation with shared spectrum channel access in FR2-2**   |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  |  |  |  | | --- | --- | | ***subCarrierSpacingCommon*** |  | | scs15or60 | 32 | | scs30or120 | 64 |   **[Unchanged part omitted]** |

**TP# 1-1E for TS38.213 [11]**

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| 4.1 Cell search  [text omitted]  **Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* and *spare* to for operation with shared spectrum channel access in FR2-2**   |  |  |  | | --- | --- | --- | | ***subCarrierSpacingCommon*** | ***~~spare~~*** |  | | ~~scs15or60~~ | ~~0~~ | ~~16~~ | | scs15or60 | ~~1~~ | 32 | | scs30or120 | ~~0~~ | 64 | | ~~scs30or120~~ | ~~1~~ | ~~reserved~~ | |

**TP# 1-1E for TS38.213 [13]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| \*\*\* Unchanged part omitted \*\*\*  Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* to for operation with shared spectrum channel access in FR2-2   |  |  |  | | --- | --- | --- | | *subCarrierSpacingCommon* | *~~spare~~* |  | | ~~scs15or60~~ | ~~0~~ | ~~16~~ | | scs15or60 | ~~1~~ | 32 | | scs30or120 | ~~0~~ | 64 | | ~~scs30or120~~ | ~~1~~ | ~~reserved~~ |   \*\*\* Unchanged part omitted \*\*\* |

**TP# 1-1F for TS38.213 [14]**

|  |  |  |  |  |  |  |  |  |  |
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| 4.1 Cell search \*\*\* Unchanged text omitted \*\*\*  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* and *spare* to for operation with shared spectrum channel access in FR2-2   |  |  |  | | --- | --- | --- | | *subCarrierSpacingCommon* |  |  | | scs15or60 |  | 32 | | scs30or120 |  | 64 |   \*\*\* Unchanged text omitted \*\*\* |

**TP# 1-1G for TS38.213 [16]**

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| 4.1 Cell search  ====================== Unchanged Text Omitted =============================  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* and LSB of *ssb-SubcarrierOffset* *~~spare~~* to for operation with shared spectrum channel access in FR2-2   |  |  |  | | --- | --- | --- | | *subCarrierSpacingCommon* | LSB of *ssb-SubcarrierOffset ~~spare~~* |  | | scs15or60 | 0 | 16 | | scs15or60 | 1 | 32 | | scs30or120 | 0 | 64 | | scs30or120 | 1 | reserved |   ============== Unchanged Text Omitted ====================== |

**TP# 1-1H for TS38.213 [16]**

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| 4.1 Cell search  ====================== Unchanged Text Omitted ===========================  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  Table 4.1-2: Mapping between ~~the combination of~~ *subCarrierSpacingCommon* ~~and~~ *~~spare~~* to for operation with shared spectrum channel access in FR2-2   |  |  |  | | --- | --- | --- | | *subCarrierSpacingCommon* | *spare* |  | | ~~scs15or60~~ | ~~0~~ | ~~16~~ | | scs15or60 | 1 | 32 | | scs30or120 | 0 | 64 | | ~~scs30or120~~ | ~~1~~ | ~~reserved~~ |   ====================== Unchanged Text Omitted ========================= |

**TP# 1-1I for TS38.213 [16]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| 4.1 Cell search  ====================== Unchanged Text Omitted ===========================  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is ~~either~~ provided by *ssb-PositionQCL* ~~or, if~~ *~~ssb-PositionQCL~~* ~~is not provided,~~~~obtained from a~~ *~~MIB~~* ~~provided by a SS/PBCH block according to Table 4.1-2~~. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  ~~Table 4.1-2: Mapping between the combination of~~ *~~subCarrierSpacingCommon~~* ~~and~~ *~~spare~~* ~~to for operation with shared spectrum channel access in FR2-2~~   |  |  |  | | --- | --- | --- | | *~~subCarrierSpacingCommon~~* | *~~spare~~* |  | | ~~scs15or60~~ | ~~0~~ | ~~16~~ | | ~~scs15or60~~ | ~~1~~ | ~~32~~ | | ~~scs30or120~~ | ~~0~~ | ~~64~~ | | ~~scs30or120~~ | ~~1~~ | ~~reserved~~ |   ==================== Unchanged Text Omitted ======================= |

**TP# 1-1J for TS38.213 [17]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* and *spare* to for operation ~~with shared spectrum channel access~~ in FR2-2   |  |  |  | | --- | --- | --- | | *subCarrierSpacingCommon* | *~~spare~~* |  | | ~~scs15or60~~ | ~~0~~ | ~~16~~ | | scs15or60 | ~~1~~ | 32 | | scs30or120 | ~~0~~ | 64 | | ~~scs30or120~~ | ~~1~~ | ~~reserved~~ | |

**TP# 1-1K for TS38.213 [19]**

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| 4 Synchronization procedures  4.1 Cell search  [omitted text]  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one. If *subCarrierSpacingCommon* in the MIB indicates ‘scs15or60’, the UE assumes that for PDCCH monitoring in the Type0-PDCCH CSS set in Clause 13.  Table 4.1-2: Mapping between *subCarrierSpacingCommon* to for operation with shared spectrum channel access in FR2-2   |  |  | | --- | --- | | *subCarrierSpacingCommon* |  | | scs15or60 | 32 | | scs30or120 | 64 | |  |  | |  |  |   [omitted text] |

**TP# 1-1L for TS38.213 [19]**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  **Table 4.1-2: Mapping between the combination of *subCarrierSpacingCommon* and *spare* to for operation with shared spectrum channel access in FR2-2**   |  |  | | --- | --- | | ***subCarrierSpacingCommon*** |  | | scs15or60 | 32 | | scs30or120 | 64 | |

**TP# 1-2 for TS38.213 [1][7][8][11][13][14][17]**

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| --- |
| <unchanged part omitted>  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  For operation without shared spectrum channel access in FR2-2, a UE expects *subCarrierSpacingCommon* = ‘*scs30or120’* from a MIB provided by a SS/PBCH block. |

### Summary of Discussions

There are two main issues, which are somewhat related. First is on the signaling of Q including number of bits allocated for Q. The second issues is whether Q indication is needed for licensed operation or not. From the last meeting several companies commented that these two issues are related and should be discussed together. Therefore, moderator has merge the two issues into Section 2.1.

* Signaling of Q
  + Large number of companies suggest to revise RAN1 working assumption- based on input from RAN2, such that we use only 1 bit for Q with supporting {32, 64} only.
* Indication of Q in licensed operations
  + All companies that provided TP proposed nearly identical TP to resolve the issue for Q indication in licensed operations.

Based on inputs received moderator suggest either TP#1-3 or #1-3A for further discussion.

**TP# 1-3 for TS38.213**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4 Synchronization procedures  4.1 Cell search  < Unchanged parts are omitted >  For operation without shared spectrum channel access, an SS/PBCH block index is same as a candidate SS/PBCH block index.  < Unchanged parts are omitted >  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  For operation without shared spectrum channel access in FR2-2, a UE expects *subCarrierSpacingCommon* = ‘*scs30or120’* from a MIB provided by a SS/PBCH block.  Table 4.1-2: Mapping between ~~the combination of~~ *subCarrierSpacingCommon* ~~and~~ *~~spare~~* to for operation with shared spectrum channel access in FR2-2   |  |  |  | | --- | --- | --- | | *subCarrierSpacingCommon* | *~~spare~~* |  | | ~~scs15or60~~ | ~~0~~ | ~~16~~ | | scs15or60 | ~~1~~ | 32 | | scs30or120 | ~~0~~ | 64 | | ~~scs30or120~~ | ~~1~~ | ~~reserved~~ |   < Unchanged parts are omitted > |

#### TP# 1-3A for TS38.213

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4 Synchronization procedures  4.1 Cell search  < Unchanged parts are omitted >  For operation without shared spectrum channel access, an SS/PBCH block index is same as a candidate SS/PBCH block index.  < Unchanged parts are omitted >  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  For operation without shared spectrum channel access in FR2-2, a UE expects *subCarrierSpacingCommon* = ‘*scs30or120’* from a MIB provided by a SS/PBCH block.  Table 4.1-2: Mapping between ~~the combination of~~ *subCarrierSpacingCommon* ~~and~~ *~~spare~~* to for operation ~~with shared spectrum channel access~~ in FR2-2   |  |  |  | | --- | --- | --- | | *subCarrierSpacingCommon* | *~~spare~~* |  | | ~~scs15or60~~ | ~~0~~ | ~~16~~ | | scs15or60 | ~~1~~ | 32 | | scs30or120 | ~~0~~ | 64 | | ~~scs30or120~~ | ~~1~~ | ~~reserved~~ |   < Unchanged parts are omitted > |

### [CLOSED] 1st Round Discussion

Please comment further on Proposal #1-1, and TP#1-3 and #1-3A. If you have any other suggestions, please comment them as well.

#### Proposal #1-1

* Use 1 bit for Q in MIB
  + SubcarrierSpacingCommon field will be used to convey value of {32, 64}
  + Note that this is revising the working assumption made in RAN1#107-e on “use 2 bits for Q, {SubcarrierSpacingCommon, spare bit in MIB}”

**Proposal #1-1A**

* Use 1 bit for Q in MIB
  + SubcarrierSpacingCommon field will be used to convey value of {32, 64} for operation with~~out~~ shared spectrum channel access
  + Note that this is revising the working assumption made in RAN1#107-e on “use 2 bits for Q, {SubcarrierSpacingCommon, spare bit in MIB}”

|  |  |
| --- | --- |
| Company | Comments |
| InterDigital | Do not support Proposal #1-1.  We propose using {8, 16, 32, 64}, where the indication can be based on combination of *SubcarrierSpacingCommon* and one additional bit. We think that the one additional bit can be one of   * MSB of *controlResourceSetZero*, * LSB of *ssb-SubcarrierOffset*, or * MSB of the DMRS index in PBCH ()   , but we are also open for other possible bits. |
| Nokia | We support Proposal #1-1.  We would prefer TP# 1-3 for further discussion, we think that Table 4.1.2 applies only in shared spectrum access. |
| Samsung | We fixed the revision marks for our TPs in 1-1G, H, and I.  We are ok with Proposal #1-1.  Although we don’t think the description for licensed operation is needed, we can be ok with TP# 1-3. We don’t support TP# 1-4 since there is no need to define Q for licensed operation. |
| Qualcomm | We support proposal #1-1.  We prefer TP #1-3A but also fine with TP #1-3. |
| Intel | We still prefer to have 2 bits for Q value indication.  For this purpose, 1 bit could be borrowed from kSSB indication from MIB assuming, for example, that only even kSSB values are supported. Based on agreements in RAN4 regarding channel needing to be multiple integers of the largest SCS, 960 kHz, our understanding is that it should be possible to limit kSSB to be even values without significant impact the RAN4 channelization. As it potentially could affect RAN4 work on channel/sync raster, which is currently ongoing, we propose to send an LS to RAN4 asking them whether borrowing 1 bit from kSSB indication in MIB is possible. |
| LG Electronics | We support proposal #1-1, but we are open to discuss on the possibility of borrowing another 1 bit, if appropriate. In that sense, we have one question to Intel.  @ Intel,  If {16, 32, 64} can be signaled for 960 kHz by using the LSB of k\_ssb, our understanding is that RAN4 need to design channel raster for 960 kHz with an interval of 2\*960 kHz. Is this the correct understanding?  For TPs, we are OK with TP#1-3, but prefer NOT to have a sentence for licensed band operation.  @ Samsung,  Could you elaborate on why ‘1’ for spare bit should not be crossed? |
| DOCOMO | Support proposal#1-1.  The use of controlResourceSetZero should prioritize the discussion on RB offset. We understand that RAN4 decided to use floating sync raster for licensed band. For this design, to implement the previous agreements, more than 8 entries are required for the original purpose of this field. So it is impossible to use for Q indication.  The use of kSSB is indeed dependent on RAN4. But we do not prefer to take such way since, again, floating sync raster is supported in licensed band per RAN4’s decision.  The use of DM-RS index seems to be changing the legacy UE behavior for DM-RS decoding. We do not think additional Q value deserve such drawback. |
| Samsung2 | Thanks for the comment from LG. We retreat our comment on leaving “1” in the table. I misunderstand the table with the one we modified for our TPs, and sorry for the confusion.  Also, we are open to have another bit in MIB to indicate Q, but we indeed doubt the availability of such bit. |
| Apple | We support Proposal #1-1 and TP 1-3.  On the repurposing other bit in addition to *subCarrierSpacingCommon,* it has a clear impact on other functions e.g., CORESET#0 location or sub-carrier offset of SSB, which is not preferrable due to dependency/impacts on RAN4 design and creating risk of deferring the competition of this Rel-17 WI. |
| Futurewei | We prefer to have at least three values for Q as was agreed before rather than change an existing agreement. If only one value of Q<64 is provided, we should ask whether DBTW should be supported at all. We are open to discuss how and where the second bit will be provided. For instance, we can agree with the above proposal provided that there is a package with the SSB-PositionQCL signaling of at least three values. |
| Huawei, HiSilicon | **First preference**-  If possible to reach a consensus, we support 2 bits to indicate in MIB. Other than *SubcarrierSpacingCommon,*  the second bit can be either of the following   * LSB of *ssb-SubcarrierOffset*, * A bit from *controlResourceSetZero*,   **Second preference-**  If not possible to reach a consensus to support 2 bits to indicate , we **conditionally** support proposal 1-1 **if** 2 bits are still used to indicate *SSB-PositionQCL-Relation* () in SIB2, SIB3, SIB4, MeasObjectNR, and ServingCellConfigCommon with parameter values {16,32,64}. Similar to the current supported mechanism in Rel-16, *SSB-PositionQCL-Relation* applicable to a serving cell overwrites ={32,64} acquired from the MIB of that cell.  The rationale behind using 2 bits to configure *SSB-PositionQCL-Relation* while having only 1 bit in MIB to indicate is that, for operation with shared spectrum, indicating =32 in MIB does not restrict the gNB to transmit 32 distinct SSB beams. For instance, while =32 is indicated in MIB, gNB can still transmit only M distinct SSB beams where (for instance, M=16). In such a case, a UE that has detected the SSB with candidate index would monitor Type0-PDCCH in monitoring occasions corresponding to candidate SSB indexes where and, further, may soft combine the PDSCH associated with Type0-PDCCH corresponding to such candidate SSB indexes and . Note that, as , implies that which, in turns, means that the detected SSB with candidate index is actually QCL with the SSB with candidate index After RRC connection, gNB may configure the exact value of (eg *SSB-PositionQCL-Relation* = 16) to the UE.  If our second preference is agreed, our preferred **TP is TP#1-1**.  TP#1-1 is aligned with the Note in the Agreement in RAN1 107 “UE is expected to be configured with =64 in licensed operations” and using the following text:  “For operation without shared spectrum channel access in FR2-2, UE assumes =64 and expects that the same value for is indicated in a MIB provided by a SS/PBCH block.”  also addresses the concern from some companies that specifications should not imply that gNB configures through SSB-PositionQCL-Relation in a licensed band deployment. |
| NEC | We prefer to use 2 bits in MIB to convey value of Q={16,32,64}, and share the same view with Intel about borrowing one bit from k\_SSB indication similar to that of the NR-U. |
| Sharp | We do not support Proposal #1-1 with restrictive value range of {32, 64} with only one effective value for Q mechanism. Although we are open to repurposing another bit, it seems difficult to obtain another MIB bit for Q indication, without dependency on other WGs or topics.  Thus, the above is the exact motivation of our proposal of partial Q indication of {16, 32, 64} by one MIB bit (TP#1-1K). More specifically, *subCarrierSpacingCommon =* ‘scs15or60’ indicates Q = {16, 32}, which means the gNB may transmit SSB with ether Q = 16 or 32. Before decoding SIB1, for the reception of SSB, the UE makes QCL assumption of Q = 32 for soft combing (when gNB actually transmits SSB according to Q = 16, the cost is that soft combing uses half of SSB receptions). While for the reception of Type0 PDCCH, the UE makes QCL assumption of Q = 16 (when gNB actually transmits SSB according to Q = 32, the cost is two more PDCCH blind decodings). |
| Ericsson | We support TP #1-3  We have strong concerns about Proposal #1-3a since it defines Q (and requires signaling of Q) for operation without shared spectrum channel access. Q is irrelevant for a licensed only implementation, hence we cannot agree to removing the text "with shared spectrum channel access" from the caption of Table 4.1-2.  We support Proposal 1.1 with the following update to be consistent with TP #1-3. We think this is the most reasonable path forward. We are doubtful an additional bit can be repurposed, and we think placing yet another constraint on RAN4 channelization design is not productive and will only delay WI completion, especially at this stage of maintenance. Proposal #1-1a  * Use 1 bit for Q in MIB   + SubcarrierSpacingCommon field will be used to convey value of {32, 64} for operation without shared spectrum channel access   + Note that this is revising the working assumption made in RAN1#107-e on “use 2 bits for Q, {SubcarrierSpacingCommon, spare bit in MIB}” |
| Mediatek | We are ok with proposal 1-1. We also prefer TP# 1-3A since it’s closer to the original agreement. |
| CATT | Support proposal 1-1. Note this alternative (if RAN2 indicates 2 bit is not possible) is already agreed previously. |
| Moderator | Updated Proposal based on Ericsson’s comments.  Following is tentative summary of comments so far.  Supportive of Proposal 1-1 (or 1-1a)   * Ericsson, Nokia, Samsung, Qualcomm, LGE, Docomo, Apple, Huawei/HiSilicon (2nd preference), Mediatek, CATT   + Main reasons: doubtful of obtaining another bit in MIB, do not want to create another RAN4 dependency   Not supportive of Proposal 1-1   * Interdigital, Intel, Futurewei, Huawei/HiSilicon (1st preference), NEC, Sharp   + Main reasons: supporting 2 bits is feasible, only supporting 2 states seems to negate the benefits of Q altogether   Moderator suggest discussing the TP#1-3 or 1-3A after the conclusion has been made first. |
| ZTE, Sanechips | We support Proposal #1-1 and prefer TP# 1-3. We do not see a need to add such limitation since Q is just used for operation with shared spectrum channel access, not for licensed band. We propose the following update: Proposal #1-1A  * Use 1 bit for Q in MIB   + SubcarrierSpacingCommon field will be used to convey value of {32, 64} for operation with~~out~~ shared spectrum channel access   + Note that this is revising the working assumption made in RAN1#107-e on “use 2 bits for Q, {SubcarrierSpacingCommon, spare bit in MIB}”   For three options of additional bit provided by InterDigital, we have the same views as DOCOMO. |
| vivo | We support TP #1-3.  For proposal 1-1, with some company’s comments that, if two bits are used, the other bit could only from ‘*controlResourceSetZero’* or LSB of ‘*ssb-SubcarrierOffset’.* However, with the working assumption in RAN1#106b-e meeting:  Working assumption:  For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW   * If only 1 bit is needed: subCarrierSpacingCommon * If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 (pending CORESET0 or search space design would allows for this bit), else, use the spare-bit (not the Msg Extension bit)   + The design of CORESET0 and search space shall be done without any consideration to this proposal   + If 2 bits are needed for both 120kHz and 480/960kHz cases, then use the same bit field combination (i.e. use pdcch-ConfigSIB1 bit for 120/480/960 kHz or spare-bit for 120/480.960 kHz)   + Note: If pdcch-ConfigSIB1 bit is used, the use of controlResourceSetZero (searchSpaceZero) for 120 kHz and   searchSpaceZero (controlResourceSetZero) for 480/960 kHz is not precluded * FFS: if 3 bits are required * Note: the working assumption can be confirmed after RAN1 agrees on the number of needed SSB-CORESET0 offsets based on RAN4 channelization design     It has been concluded that this 1 bit can only from ‘pdcch-ConfigSIB1’. Moreover, whether this 1 bit could be used depends on the CORESET 0 design. Thus, we prefer to postpone this discussion after the CORESET 0 design. |
| LG Electronics | We believe ZTE’s modification is the intention from Ericsson. ☺  We are OK with ZTE’s modification. |
| Lenovo | We support proposal 1-1, as for the TBs, our preference is TP #1-3 |
| OPPO | We support proposal 1-1 or proposal 1-1A with ZTE’s modification.  We are in general fine with TP #1-3, but we still don’t know how to distinguish operation with or without shared spectrum channel access in FR2-2 from UE side? |
| Samsung | We are ok with Proposal 1-1A with ZTE’s modification |
| Ericsson | Oooops ☺  Indeed, my intention for Proposal 1.1a was as follows. Sorry for the confusion. Proposal #1-1A  * Use 1 bit for Q in MIB   + SubcarrierSpacingCommon field will be used to convey value of {32, 64} for operation with~~out~~ shared spectrum channel access   Note that this is revising the working assumption made in RAN1#107-e on “use 2 bits for Q, {SubcarrierSpacingCommon, spare bit in MIB}” |
| Moderator | Fixed the error in Proposal 1-1A. |

### <Summary of 1st Round Discussion>

#### Proposal #1-1A

* Use 1 bit for Q in MIB
  + SubcarrierSpacingCommon field will be used to convey value of {32, 64} for operation with~~out~~ shared spectrum channel access
  + Note that this is revising the working assumption made in RAN1#107-e on “use 2 bits for Q, {SubcarrierSpacingCommon, spare bit in MIB}”

Supportive of Proposal 1-1 or 1-1A

* Ericsson, Nokia, Samsung, Qualcomm, LGE, Docomo, Apple, Huawei/HiSilicon (2nd preference), Mediatek, CATT, ZTE/Sanechips, [vivo], Lenovo/Motorola Mobility, OPPO,
  + Main reasons: doubtful of obtaining another bit in MIB, do not want to create another RAN4 dependency

Not supportive of Proposal 1-1/1-1A

* Interdigital, Intel, Futurewei, Huawei/HiSilicon (1st preference), NEC, Sharp
  + Main reasons: supporting 2 bits is feasible, only supporting 2 states seems to negate the benefits of Q altogether

Company views are split. Moderator suggests discussing this issue during GTW. Once decided RAN1 can work further on required TP to the specification.

### GTW Outcome – Tue Feb 22

**Working Assumption**

* Use 1 bit for Q in MIB
  + SubcarrierSpacingCommon field will be used to convey value of {32, 64} for operation with~~out~~ shared spectrum channel access
  + Note that this is revising the working assumption made in RAN1#107-e on “use 2 bits for Q, {SubcarrierSpacingCommon, spare bit in MIB}”

### [ACTIVE] 2nd Round Discussion

During GTW the following working assumption was made.

**Working Assumption**

* Use 1 bit for Q in MIB
  + SubcarrierSpacingCommon field will be used to convey value of {32, 64} for operation with~~out~~ shared spectrum channel access
  + Note that this is revising the working assumption made in RAN1#107-e on “use 2 bits for Q, {SubcarrierSpacingCommon, spare bit in MIB}”

With the working assumption, moderator suggest focusing the efforts in finalizing the require TP based on the working assumption. Can companies comment if you can accept TP#1-3 based on working assumption based in GTW?

#### TP# 1-3 for TS38.213

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4 Synchronization procedures  4.1 Cell search  < Unchanged parts are omitted >  For operation without shared spectrum channel access, an SS/PBCH block index is same as a candidate SS/PBCH block index.  < Unchanged parts are omitted >  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  For operation without shared spectrum channel access in FR2-2, a UE expects *subCarrierSpacingCommon* = ‘*scs30or120’* from a MIB provided by a SS/PBCH block.  Table 4.1-2: Mapping between ~~the combination of~~ *subCarrierSpacingCommon* ~~and~~ *~~spare~~* to for operation with shared spectrum channel access in FR2-2   |  |  |  | | --- | --- | --- | | *subCarrierSpacingCommon* | *~~spare~~* |  | | ~~scs15or60~~ | ~~0~~ | ~~16~~ | | scs15or60 | ~~1~~ | 32 | | scs30or120 | ~~0~~ | 64 | | ~~scs30or120~~ | ~~1~~ | ~~reserved~~ |   < Unchanged parts are omitted > |

#### Company Comments

Please only comment if you have concerns on TP#1-3. If you have concerns, please provide information on the exact concerns.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | We prefer to delete the sentence for UE assumption on subCarrierSpacingCommon for licensed band since it is mis-configuration. But we can accept TP#1-3 if majority supports it. |
| Ericsson | Support TP#1-3. We think it is fine to provide a UE expectation on subCarrierSpacingCommon. |
| Nokia\_2 | We are OK with the TP#1-3. |
| ZTE, Sanechips | Support TP#1-3. |
| OPPO | Support TP#1-3. |
| Samsung | We are ok with TP#1-3. |
| vivo | Support TP#1-3. |
| Huawei, HiSilicon | We can support TP#1-3 |

## 2.2 SSB-PositionQCL signaling in RRC

* From [1] Huawei/HiSilicon:
  + For operations with shared spectrum, support indicating SSB-PositionQCL-Relation in SIB2, SIB3, SIB4, MeasObjectNR, and ServingCellConfigCommon with parameter values {16,32,64}.
    - SSB-PositionQCL-Relation applicable to a serving cell overwrites ={32,64} acquired from the MIB of that cell.
    - Note: Such overwriting mechanism is already supported in 38.213.
  + Include SSB-PositionQCL-Relation-r17 in the RRC parameter list as per the conclusion in RAN1 #107b-e.
* From [11] Nokia/NSB
  + Range of SSB-PositionQCL-Relation-r17 is restricted to {32,64}.
* From [13] Ericsson
  + For operation with shared spectrum channel access, use 1 bit to signal Q (subCarrierSpacingCommon) with the value range for Q = {32, 64}. Update RRC parameter list to reflect this and remove spare from 38.213 according to TP#1-1E (below).
  + Update the RRC parameter spreadsheet regarding information element SSB-PositionQCL-Relation-r16 to clarify that for operation with shared spectrum channel access in FR2-2, the value range is {32,64}. Mark the row as 'stable' and include it in the RRC parameter LS to RAN2.

|  |  |  |
| --- | --- | --- |
| Parent IE | Field name | Description |
| *SIB2* | *ssb-PositionQCL-Common-r16* | Frequency specific:  QCL relation between SSB candidate indexes common for intra-frequency neighbor cells |
| *SIB3* | *ssb-PositionQCL-r16* | Cell specific:  QCL relation between SSB candidate indexes for a specific intra-frequency neighbor cell. If provided, this overwrites the value provided by *ssb-PositionQCL-Common-r16* in *SIB2* for the indicated cell. |
| *SIB4* | *ssb-PositionQCL-Common-r16* | Frequency specific:  QCL relation between SSBs common among inter-frequency neighbor cells on a specific frequency. |
| *SIB4* | *ssb-PositionQCL-r16* | Cell specific:  QCL relation between SSB candidate indexes for a specific inter-frequency neighbor cell. If provided, this overwrites the value provided by *ssb-PositionQCL-Common-r16* in *SIB4* for the indicated cell. |
| *MeasObjectNR* | *ssb-PositionQCL-Common-r16* | Frequency specific:  QCL relation between SSB candidate indexes for all measured cells in this *MeasObjectNR* (the SSBs have the same frequency and SCS) |
| *MeasObjectNR* | *ssb-PositionQCL-r16* | Cell specific:  QCL relation between SSB candidate indexes for a specific measured cell as specified in this *MeasObjectNR*. If provided, this overwrites the value signaled by *ssb-PositionQCL-Common-r16* in this *MeasObjectNR*. |
| *ServingCellConfigCommon* | *ssb-PositionQCL-r16* | Cell specific:  QCL relation between SSB candidate indexes for the serving cell configured in this *ServingCellConfigCommon* |

### Summary of Discussions

Huawei has provided a good summary of all effected RRC for signaling of ssb-PostiionQCL

* Option 1) Update the ssb-PositionQCL to be limited to {32, 64} (assuming that will be the case for MIB)
  + Nokia/NSB, Ericsson
* Option 2) Keep the ssb-PositionQCL to be {16, 32, 64}
  + Huawei/HiSilicon

Discuss further on the following ssb-PositionQCL signaling in RRC (other than MIB)

* SIB2:: ssb-PositionQCL-Common-r16
* SIB3:: ssb-PositionQCL-r16
* SIB4:: ssb-PositionQCL-Common-r16
* SIB4:: ssb-PositionQCL-r16
* MeasObjectNR:: ssb-PositionQCL-Common-r16
* MeasObjectNR:: ssb-PositionQCL-r16
* ServingCellConfigCommon:: ssb-PositionQCL-r16

### [CLOSED] 1st Round Discussion

Please comment further on option 1 and 2.

* Option 1) Update the ssb-PositionQCL to be limited to {32, 64} (assuming that will be the case for MIB)
  + Nokia/NSB, Ericsson
* Option 2) Keep the ssb-PositionQCL to be {16, 32, 64}
  + Huawei/HiSilicon

Based on the conclusion between option 1 and 2, moderator will formulate agreement/conclusion to suggest updates to all relevant RRC parameters (that Huawei has identified). If you have any other suggestions, please comment them as well.

|  |  |
| --- | --- |
| Company | Comments |
| InterDigital | We do not support Option 1 on limiting the values of ssb-PositionQCL and support Option 2.  For Option 2, we prefer to include the option for Q=8 to support the scenarios with higher demand for frequent monitoring and/or with lower number of SSB beams. |
| Nokia | We prefer option 1 as option 2 would require further discussion how having different range for and ssb-PositionQCL and resulted different understanding would be accounted. |
| Samsung | We support Option 2) with the understanding that the value provided by ssb-PositionQCL would override the value determined by MIB, and no other spec impact is expected. |
| Qualcomm | We prefer option 1 for the same reason as Nokia’s |
| Intel | Prefer to postpone till decision on number of bits for Q value indication as it affects the number of SSB candidates. |
| LG Electronics | If we are not missing something, Option 2 seems not aligned with the following previous agreement.  **Agreement (RAN1#107-e)**  SSB-PositionQCL-Relation IE to indicate QCL relationship between SSB positions for FR2-2 are same set of values supported for in MIB. |
| DOCOMO | Good to postpone the decision till Q values in MIB is decided in 2.1.  But we agree with LGE. As long as we do not revert the agreement, the only choice remained seems to be option 1 if only 1 bit in MIB is available for Q. |
| Apple | We first second the comments from LGe.  Support Option 1.  Assuming the candidate values of Q parameter on FR2-2 are limited to {32, 64} and applied for all serving cells on FR2-2, we do not see any reason to allow SIB2 (intra-frequency) or SIB4 (inter-frequency) indicating different values than those values that can be broadcasted by MIB. |
| Futurewei | We prefer Option2. We agree with LGE on the necessity to align the values to be consistent with an early agreement. We also want to point out another agreement in the same session that indicates the support of three values.  **Agreement**   * Same values using the same set of signaling bits are supported for 120, 480, and 960 kHz. * Supported values of : {16, 32, 64}   + Note:     - For operation with shared spectrum channel access, any supported value of can be indicated and value < 64 indicates DBTW enabled     - UE is expected to be configured with =64 in licensed operations     - For operation with and without shared spectrum channel access, =64 indicates that the SS/PBCH block index and the candidate SS/PBCH block index have a one-to-one mapping relationship. |
| Huawei, HiSilicon | As a proponent company, we support Option 2.  Unlike **Nokia and Qualcomm**, we don’t see why using 1 bit in MIB and 2 bits in RRC (SIB2, SIB3, SIB4, MeasObjectNR, and ServingCellConfigCommon) to indicate could result in different understanding and would require further discussions. Even in Rel-16 what is indicated in MIB is overwritten by RRC. Please refer to the following from 38.213:   |  | | --- | | “ is either provided by ssb-PositionQCL or, if ssb-PositionQCL is not provided, obtained from a MIB provided by a SS/PBCH block” |   In our view, above text clarifies that if is provided by ssb-PositionQCL, UE would ignore the value of that is indicated in MIB. In principle, even in Rel-16, the in MIB can be different from the dedicated value in RRC. So, Similar to the current supported mechanism in Rel-16, *SSB-PositionQCL-Relation* applicable to a serving cell overwrites ={32,64} acquired from the MIB of that cell. The only difference with Rel-16 behavior is that, RRC can additionally configure, eg, =16 while MIB can only indicate ={32,64}. The rationale behind using 2 bits to configure *SSB-PositionQCL-Relation* while having only 1 bit in MIB to indicate is that, for operation with shared spectrum, indicating =32 in MIB does not restrict the gNB to transmit 32 distinct SSB beams. For instance, while =32 is indicated in MIB, gNB can still transmit only M distinct SSB beams where (for instance, M=16). In such a case, a UE that has detected the SSB with candidate index would monitor Type0-PDCCH in monitoring occasions corresponding to candidate SSB indexes where and, further, may soft combine the PDSCH associated with Type0-PDCCH corresponding to such candidate SSB indexes and . Note that, as , implies that which, in turns, means that the detected SSB with candidate index is actually QCL with the SSB with candidate index After RRC connection, gNB may configure the exact value of (eg *SSB-PositionQCL-Relation* = 16) to the UE.  Finally, note that Rel-16 not only supports the RRC configured value of to overwrite the indicated value of in MIB but also supports a Cell-specific RRC configured value of (eg in SIB3) to overwrite the frequency-specific configured value of (eg in SIB2). |
| NEC | As pointed out by several companies, we prefer to postpone this discussion till Q value is decided although we support Option 2, and we also think SSB-PositionQCL-Relation IE should be in line with Q value set in MIB based on previous Agreements. |
| Sharp | We share the view from Intel on that this discussion can be postponed before decision of Section 2.1. |
| Ericsson | We prefer Option 1, and we agree with LGE.  Furthermore, we don't see the need/benefit of discussing and then specifying behavior for the various configuration options inherent in Option 2. For example, how will the gNB operate if it signals 32 in MIB and 16 in some other message (SIB2,3,4)? Should it transmit SSB in k+16\*n or k+32\*n? If it succeeds in k+16\*n then it will not transmit in k+32\*n, so then a UE getting Q from MIB will miss the SSB. |
| Mediatek | Support option 1. Ok to postpone the discussion. |
| Moderator | LGE pointed out an agreement previously made. We would need a good reason and consensus to change previous agreement.  **Agreement (RAN1#107-e)**  SSB-PositionQCL-Relation IE to indicate QCL relationship between SSB positions for FR2-2 are same set of values supported for in MIB.  Moderator suggests waiting for conclusion on the Q signaling in MIB first, and based on the conclusion for Q signaling in MIB, we follow the same set of values for RRC signaling as per agreement.  With that said, please provide further comments until the GTW. |
| CATT | We prefer Option 1, and we agree with LGE |
| ZTE, Sanechips | We prefer Option 1 and we agree with FL suggestion. |
| vivo | We prefer Option 1 and agree with LGE |
| Lenovo | We support option 1. However, we agree with many companies to wait for conclusion on Q value |
| OPPO | Support Option 1. |
| Huawei/HiSilicon2 | We still believe that Option 2 is the good compromise and we support it. Below, we try to reply to a few comments:  **LGE, Moderator:**  We agree that using two bits for indicating Q in RRC and 1 bit for indicating Q in MIB is not exactly aligned with the following agreement:  Agreement 1: “SSB-PositionQCL-Relation IE to indicate QCL relationship between SSB positions for FR2-2 are same set of values supported for in MIB.”  However, this agreement was made when it was assumed that 2 bits are available in MIB to indicate Q and, as pointed out by Futurewei, we have the following agreement in the same meeting RAN1 107-e too  Agreement 2: “Supported values of : {16, 32, 64}”  We don’t think referring to only Agreement 1 would be sufficient to make a conclusion for this discussion as one may instead refer to Agreement 2 and suggest that a second bit should be used in MIB to indicate the agreed values of : {16, 32, 64}.  Overall, considering the input from RAN2 on unavailability of the spare bit, we think that RAN1 should not put too much emphasis on the previous agreements regarding the number of bits/values which were achieved mainly assuming two bits are available and, instead, think of the best compromise solution given the constraint of unavailability of the spare bit.  **Ericsson:**  **Regarding “specifying behavior” concern:**  As explained in our earlier entry to this discussion, using 1 bit in MIB and 2 bits in RRC (SIB2, SIB3, SIB4, MeasObjectNR, and ServingCellConfigCommon) to indicate does not have any spec impact as even in Rel-16 what is indicated in MIB is overwritten by RRC. Please refer to the following from 38.213:   |  | | --- | | “ is either provided by ssb-PositionQCL or, if ssb-PositionQCL is not provided, obtained from a MIB provided by a SS/PBCH block” |   In our view, above text clarifies that if is provided by ssb-PositionQCL, UE would ignore the value of that is indicated in MIB. In principle, even in Rel-16, the in MIB can be different from the dedicated value in RRC. So, Similar to the current supported mechanism in Rel-16, SSB-PositionQCL-Relation applicable to a serving cell overwrites ={32,64} acquired from the MIB of that cell. The only difference with Rel-16 behavior is that, RRC can additionally configure, eg, =16 while MIB can only indicate ={32,64}.  **Regarding the “need/benefit” concern:**  For operation with shared spectrum, indicating =32 in MIB does not restrict the gNB to transmit 32 distinct SSB beams. For instance, while =32 is indicated in MIB, gNB can still transmit only 16 distinct SSB beams. In such a case, a UE that has detected the SSB with candidate index would monitor Type0-PDCCH in monitoring occasions corresponding to candidate SSB indexes where and, further, may soft combine the PDSCH associated with Type0-PDCCH corresponding to such candidate SSB indexes and . Note that, since , then which, in turns, means that the detected SSB with candidate index is actually QCL with the SSB with candidate index After RRC connection, gNB may configure the exact value of (eg *SSB-PositionQCL-Relation* = 16) to the UE.  So, in summary, if Option 2 is used, when gNB transmits only 16 SSB beams, an initial access UE that assumes Q=32 can still benefit from DBTW by soft-combining SIB1 associated with candidate SSB0 and SSB32 (while missing the opportunity to also use the SIB1 associated with SSB16 in soft combining). However, after initial access, UE would know the exact value of Q=16 for RRM purposes.  **Regarding the following specific question:**  **“how will the gNB operate if it signals 32 in MIB and 16 in some other message (SIB2,3,4)? Should it transmit SSB in k+16\*n or k+32\*n? If it succeeds in k+16\*n then it will not transmit in k+32\*n, so then a UE getting Q from MIB will miss the SSB.”**  We are not sure we understand the question. If gNB transmits 16 SSB beams and Option 2 is used, it would make sense that Q=32 is indicated in MIB and Q=16 is indicated in RRC (*SIB2/SIB3/SIB4/ MeasObjectNR/ ServingCellConfigCommon).* However, **similar toRel-16,** gNB behavior is not specified. gNB can even indicate Q=64 in MIB if it decides to. We also don’t understand how an initial access UE “misses” an SSB? An initial access UE first detect the candidate SSB and then uses the indicated value of Q in MIB to its advantage for to monitor Type0-PDCCH in monitoring occasions corresponding to candidate SSB indexes where and, further, may soft combine the RMSI-PDSCH corresponding to such candidate SSB indexes and . So, even if only 16 SSB beams are actually transmitted, indicating Q=32 would help UE to use RMSI-PDSCH associated with and for soft-combining while missing the opportunity to use RMSI-PDSCH associated for for soft-combining. After initial access, the actual value of Q=16 is indicated to the UE. We think it is clear that it is advantageous for the UE to know the actual value of Q(=16) and not the indicated value of Q(=32) in MIB after RRC connection. |

### <Summary of 1st Round Discussion>

Summary of company views on Q signaling other than MIB.

* Option 1) Update the ssb-PositionQCL to be limited to {32, 64} (assuming that will be the case for MIB)
  + Nokia/NSB, Ericsson, Qualcomm, LGE, Docomo, Apple, MediaTek, CATT, ZTE/Sanechips, vivo, Lenovo/Motorola Mobility, OPPO
  + Main reasons:
    - Not aligned with previous agreement “SSB-PositionQCL-Relation IE to indicate QCL relationship between SSB positions for FR2-2 are same set of values supported for in MIB.”
    - Further discussion on handling cases when Q from MIB and Q from RRC do not match up is needed.
* Option 2) Keep the ssb-PositionQCL to be {16, 32, 64}
  + Huawei/HiSilicon, Interdigital, Samsung, Futurewei, NEC

Moderator suggests waiting for conclusion on the Q signaling in MIB first, and based on the conclusion for Q signaling in MIB, we follow the same set of values for RRC signaling as per agreement.

### [ACTIVE] 2nd Round Discussion

During the GTW discussion, it was clear having different values indicated by MIB and RRC is something that is not agreeable. Therefore, moderator assumes RAN1 can focus on option 1.

#### Conclusion #1-2

* Update the ssb-PositionQCL in RRC to {32, 64} values.
  + For reference, the following are list of RRC IEs that references ssb-PositionQCL in release 16.
    - SIB2:: ssb-PositionQCL-Common-r16
    - SIB3:: ssb-PositionQCL-r16
    - SIB4:: ssb-PositionQCL-Common-r16
    - SIB4:: ssb-PositionQCL-r16
    - MeasObjectNR:: ssb-PositionQCL-Common-r16
    - MeasObjectNR:: ssb-PositionQCL-r16
    - ServingCellConfigCommon:: ssb-PositionQCL-r16

If conclusion #1-2 is agreeable, moderator would like to ask Huawei (originating company) to provide comments to the RRC directly.

Please only comment if you have concerns on Conclusion #1-2. If you have concerns, please provide information on the exact concerns.

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| --- | --- |
| Company | Comments |
| Ericsson | We think the Moderator's intention was to include the word "not" above. Please inform if that is not the case.  Support Conclusion #1-2. |
| Moderator | Yes. Sorry for the typo. ‘not’ was missing. |
| Nokia\_2 | We are OK with Conclusion#1-2 |
| ZTE, Sanechips | Support Conclusion #1-2. |
| OPPO | Support Conclusion #1-2. |
| Samsung | We are ok with conclusion #1-2 |
| Moderator | Based on vice chairman’s guidance, since this relates to RRC, I will suggest to check if companies are ok directly over email, and ask Huawei to put input to the RRC agenda. |
| vivo | Support Conclusion #1-2. |

## 2.3 DBTW Length

* From [1] Huawei/HiSilicon:
  + Support default DBTW length of 5ms if discoveryBurstWindowLength is not provided in FR2-2.
    - No specification change is needed.
* From [5] OPPO
  + When the DBTW length is not configured, UE can assume the DBTW length for all supported SCSs (120/480/960 kHz) in FR2-2 is a half frame for operation in unlicensed band.
* From [7] ZTE/Sanechips
  + If the DBTW length is not configured (i.e. discoveryBurstWindowLength is not provided), UE can assume the DBTW length for all supported SCSs (120/480/960 kHz) in FR2-2 is a half frame.
    - Note: This is same as Rel-16 NR-U, and no specification change is needed.
* From [11] Nokia/NSB
  + Either confirm the DBTW length values to {1.25, 1, 0.75, 0.5, 0.25, 0.125} or, accounting the range, limit it to {1.25, 1, 0.75, 0.5, 0.25}
  + When DBTW is supported, and the DBTW length is not configured (i.e. discoveryBurstWindowLength is not provided), UE can assume the DBTW length for all supported SCSs (120/480/960 kHz) in FR2-2 is a half frame.
* From [14] Apple
  + Keep the default DBTW length to be half a frame i.e., 5ms for 480kHz and 960kHz SCS as in current specification.

### Summary of Discussions

The following is a summary of company views on DBTW lengths.

* Several companies commented that default value for DBTW should be 5 msec. (No change in specification)
* One company has suggest to confirm the DBTW lengths.

Moderator suggests checking if the following conclusion is acceptable.

Proposed Conclusion:

* Support default DBTW length of 5ms if discoveryBurstWindowLength is not provided in FR2-2.
* RAN1 concludes that as Q = 8 is not supported, DBTW length of 0.0625 msec is not supported for 480 and 960 kHz.
* No change to specification is needed

### [CLOSED] 1st Round Discussion

Discuss further on the following conclusion.

#### Conclusion #3-1

* Support default DBTW length of 5ms if discoveryBurstWindowLength is not provided in FR2-2.
* RAN1 concludes that as Q = 8 is not supported, DBTW length of 0.0625 msec is not supported for 480 and 960 kHz.
* No change to specification is needed

**Conclusion #3-1A**

* Support default DBTW length of 5ms if discoveryBurstWindowLength is not provided in FR2-2.
* ~~RAN1 concludes that as Q = 8 is not supported, DBTW length of 0.0625 msec is not supported for 480 and 960 kHz.~~
* No change to specification is needed

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| Company | Comments |
| InterDigital | Do not support Conclusion #3-1. Supporting Q=8 enables supporting systems with higher demand for frequent monitoring, lower latency requirements, and/or with lower number of SSB beams. |
| Nokia | Support the Conclusion #3-1 |
| Samsung | We support Conclusion #3-1 |
| Qualcomm | Fine with Conclusion #3-1 |
| Intel | Support Conclusion #3-1 |
| LG Electronics | Support Conclusion #3-1 |
| DOCOMO | Support Conclusion #3-1. |
| Apple | Support Conclusion #3-1. |
| Futurewei | Support Conclusion #3-1 |
| Huawei, HiSilicon | We can support the first bullet.  The second bullet is the active subject of discussion and can be revisited later. Note that the value of 0.0625 was not included in the RRC parameter list and is not reflected in the running RRC CR R2-2202435. So, there is no need to agree on it at this point. We suggest the following alternative conclusion: Conclusion #3-1B  * Support default DBTW length of 5ms if discoveryBurstWindowLength is not provided in FR2-2. * ~~RAN1 concludes that as Q = 8 is not supported, DBTW length of 0.0625 msec is not supported for 480 and 960 kHz.~~ * No change to specification is needed |
| NEC | Support Conclusion #3-1 |
| Sharp | We support Conclusion#3-1. |
| Ericsson | Support Conclusion #3-1 |
| Mediatek | Support conclusion #3-1. |
| Moderator | Updated the conclusion based on Huawei’s comment. In #3-1A |
| CATT | We support Conclusion #3-1 |
| ZTE, Sanechips | Support Conclusion #3-1 or #3-1A |
| vivo | We support Conclusion #3-1 |
| Lenovo | We support Conclusion #3-1, fine with #3-1A |
| OPPO | We support Conclusion #3-1 |

### <Summary of 1st Round Discussion>

Most companies seem to be comfortable with Proposed conclusion #3-1. Suggest approving the conclusion over email.

#### Conclusion #3-1A

* Support default DBTW length of 5ms if discoveryBurstWindowLength is not provided in FR2-2.
* No change to specification is needed

### [ACTIVE] 2nd Round Discussion

Please only comment if you have concerns on conclusion #3-1A.

#### Conclusion #3-1B

* For operation with shared spectrum channel access, support default DBTW length of 5ms if discoveryBurstWindowLength is not provided in FR2-2.
* No change to specification is needed

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| Company | Comments |
| Ericsson | Support Conclusion #3-1A with the addition "For operation with shared spectrum channel access, …" to the first bullet. |
| Moderator | Updated the Conclusion based on Ericsson’s comments. Hopefully this should not be controversial. |
| Nokia | We are OK with the Conclusion#3-1B |
| ZTE, Sanechips | Support Conclusion #3-1B. |
| OPPO | Support Conclusion #3-1B. |
| Samsung | We support Conclusion #3-1B. |
| InterDigital | We are ok with Conclusion #3-1B. |
| vivo | Support Conclusion #3-1B. |
| LG Electronics | Support Conclusion #3-1B. |
| Huawei, HiSilicon | We can support Conclusion #3-1B |

## 2.4 CORESET#0 Configuration

* From [1] Huawei/HiSilicon:
  + Support the following CORESET#0 RB offsets for {SSB, CORESET#0} SCS={120, 120} kHz:
    - For CORESET#0 with 24 RBs: The same as supported values in Table 13-8 of 38.213.
    - For CORESET#0 with 48 RBs: The same as supported values in Table 13-8 of 38.213 in addition to RB offset values of [0] and [28] RBs for multiplexing pattern 1.
    - For CORESET#0 with 96 RBs: RB offsets of [0] and [76] RBs for multiplexing pattern 1.
  + Support the following CORESET#0 RB offsets values for {SSB, CORESET#0} SCS={480, 480} kHz and {960, 960} kHz:
    - For CORESET#0 with 24 RBs: The same as supported values in Table 13-8 of 38.213.
    - For CORESET#0 with 48 RBs: The same as supported values in Table 13-8 of 38.213 in addition to RB offset values of [0] and [28] RBs for multiplexing pattern 1.
    - For CORESET#0 with 96 RBs: RB offsets of [0] and [76] RBs for multiplexing pattern 1.
* From [3] Interdigital
  + Support two RB offset values for MUX 3 (if supported) in CORESET#0 configuration. The two values could be (-20 if kssb=0, -21 if kssb>0) and X, where X is the number of RBs in the respective CORESET#0 and can be 24 or 48.
* From [4] vivo
  + Support Multiplexing pattern 3 for SCS 480 kHz and 960 kHz.
  + Support 96 RB for SCS 120kHz and 480 kHz and do not support 96 RB for SCS 960kHz.
  + For ‘controlResourceSetZero’ configuration for {120K, 120K} pair in FR2-2:
    - Support 2 RB offset values for multiplexing pattern 1 with 24 PRB cases: [0] and [4]
    - Support 3 RB offset values for multiplexing pattern 1 with 48 PRB cases: [0], [14], and [28]
    - Support 2 RB offset values for multiplexing pattern 1 with 96 PRB cases: [0], and [76]
    - Support following two RB offset values for multiplexing pattern 3: -20 if kssb=0, -21 if kssb>0
  + For ‘controlResourceSetZero’ configuration for {480K, 480K} pair in FR2-2:
    - Support 2 RB offset values for multiplexing pattern 1 with 24 PRB cases: [0] and [4]
    - Support 3 RB offset values for multiplexing pattern 1 with 48 PRB cases: [0], [14], and [28]
    - Support 2 RB offset values for multiplexing pattern 1 with 96 PRB cases: [0], and [76]
    - Support following two RB offset values for multiplexing pattern 3: -20 if kssb=0, -21 if kssb>0
  + For ‘controlResourceSetZero’ configuration for {960K, 960K} pair in FR2-2:
    - Support 2 RB offset values for multiplexing pattern 1 with 24 PRB cases: [0] and [4]
    - Support 3 RB offset values for multiplexing pattern 1 with 48 PRB cases: [0], [14], and [28]
    - Support following two RB offset values for multiplexing pattern 3: -20 if kssb=0, -21 if kssb>0
* From [6] CATT
  + For CORESET#0 configuration can be decided after RAN4 finalize channelization design.
  + If multiplexing pattern 3 for 480 kHz and 960 kHz is supported, the first symbols index of Type0-PDCCH monitoring occasions can be 2 for even SSB index and can be 9 for odd SSB index.
* From [8] NTT Docomo
  + Postpone the discussion on RB offset between SSB and CORESET#0 until RAN4 decides sync raster in unlicensed band.
* From [11] Nokia/NSB
  + For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, support multiplex pattern 3 with 24 PRB and 2 symbol duration, and multiplexing pattern 3 with 48 PRB and 2 symbol duration.
  + For 480 kHz and 960kHz , support multiplexing pattern 1 with 96 PRB with 2-symbol duration, with four RB offsets: 0, 36, 72, 76.
  + For 120kHz, support multiplexing pattern 1 with 96 PRB with 2-symbol duration, with three RB offsets: 0, 38, 76.
  + Confirm the support of CORESET#0 with = {96} for 120kHz, 480kHz and 960kHz sub-carrier spacing.
* From [12] Intel
  + For 120 kHz
    - Multiplexing pattern 1 with 24 RBs: 0 RB offset
    - Multiplexing pattern 1 with 48 RBs: {0, 14, 28} RB offset
    - Multiplexing pattern 1 with 96 RBs: 0 RB offset
    - Multiplexing pattern 3 with 24 RB: -20 or -21 (depending on k\_ssb) RB offset
    - Multiplexing pattern 3 with 48 RB: -20 or -21 (depending on k\_ssb) RB offset
  + For 480 kHz
    - Multiplexing pattern 1 with 24 RBs: 0 RB offset
    - Multiplexing pattern 1 with 48 RBs: {0, 14, 28} RB offset
    - Multiplexing pattern 1 with 96 RBs: {0, 38} RB offset
    - Multiplexing pattern 3 with 24 RB: -20 or -21 (depending on k\_ssb) RB offset
    - Multiplexing pattern 3 with 48 RB: -20 or -21 (depending on k\_ssb) RB offset
  + For 960 kHz
    - Multiplexing pattern 1 with 24 RBs: {0, 4} RB offset
    - Multiplexing pattern 1 with 48 RBs: 0 RB offset
    - Multiplexing pattern 1 with 96 RBs: 0 RB offset
    - Multiplexing pattern 3 with 24 RB: -20 or -21 (depending on k\_ssb) RB offset
    - Multiplexing pattern 3 with 48 RB: -20 or -21 (depending on k\_ssb) RB offset
  + Additionally support 1 symbol duration 96 RB CORESET for 480 and 960 kHz for multiplexing pattern 1.
* From [13] Ericsson
  + Support the SSB-CORESET0 offset values shown in TP#6-1D (Tables 13-10A, B, and C below for 120, 480, and 960 kHz, respectively).
  + For the 57 – 66 GHz band, the SSB-CORESET0 offsets proposed in Section 5.1 for the floating channelization design are also valid for the fixed design, and no additional offset values need to be defined.
* From [16] Samsung
  + Support the same CORESET#0 configuration table for licensed and unlicensed bands.
  + For 120 kHz SCS:
    - Support one RB offset for 24 RB CORESET#0 bandwidth in Pattern 1;
    - Support two RB offsets for 48 RB CORESET#0 bandwidth in Pattern 1;
    - Support one RB offset for 96 RB CORESET#0 bandwidth in Pattern 1;
    - Support same RB offsets as Rel-15 FR 2-1 in Pattern 3;
    - Adopt TP#4-1E for TS 38.213.
  + For 480 kHz and 960 kHz SCS:
    - Support the same CORESET#0 configuration table;
    - Support multiplexing pattern 3 with same RB offsets as in Rel-15 FR2-1;
    - Support two RB offsets for 24 RB CORESET#0 bandwidth in Pattern 1;
    - Support three RB offsets for 48 RB CORESET#0 bandwidth in Pattern 1;
    - Support two RB offsets for 48 RB CORESET#0 bandwidth in Pattern 1;
    - Support 1 symbol for CORESET#0 when the bandwidth of CORESET#0 is 96;
    - Adopt TP#4-1E for TS 38.213.
* From [17] Qualcomm
  + consider adopting the following design principles (as much as possible) for CORESET0 RB offsets for both licensed and unlicensed operation for SCS = 120 kHz, 480 kHz, and 960 kHz (per # of symbols):
    - For multiplexing pattern 1:
      * 24 RBs: 2 configs aligning CORESET 0 edges with the upper and lower edges of the 20 RB SSB
      * 48 RBs: 1 config aligning the center of the CORESET 0 with the center of the 20 RB SSB
      * 96 RBs: 1 config aligning the center of the CORESET 0 with the center of the 20 RB SSB
      * 48 RBs (open for discussion): 2 configs aligning CORESET 0 edges with the upper and lower edges of the 20 RB SSB
    - For multiplexing pattern 3:
      * 24 RBs: 2 configs placing the CORESET 0 at either side of the 20 RB SSB
      * 48 RBs: 2 configs placing the CORESET 0 at either side of the 20 RB SSB

**TP# 4-1 for TS38.213 [4]**

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| <unchanged part omitted>  Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 14 | | 3 | 1 | 48 | 2 | 14 | | 4 | 3 | 24 | 2 | -20 if  -21 if | | 5 | 3 | 24 | 2 | 24 | | 6 | 3 | 48 | 2 | -20 if  -21 if | | 7 | 3 | 48 | 2 | 48 | | 8 | 1 | 48 | 1 | 0 | | 9 | 1 | 48 | 1 | 28 | | 10 | 1 | 48 | 2 | 0 | | 11 | 1 | 48 | 2 | 28 | | 12 | 1 | 96 | 1 | 0 | | 13 | 1 | 96 | 1 | 76 | | 14 | 1 | 96 | 2 | 0 | | 15 | 1 | 96 | 2 | 76 |   <unchanged part omitted>  Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz and {960, 960}   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 14 | | 3 | 1 | 48 | 2 | 14 | | 4 | 1 | 48 | 1 | 0 | | 5 | 1 | 48 | 1 | 28 | | 6 | 1 | 48 | 2 | 0 | | 7 | 1 | 48 | 2 | 28 | | 8 | 3 | 24 | 2 | -20 if  -21 if | | 9 | 3 | 24 | 2 | 24 | | 10 | 3 | 48 | 2 | -20 if  -21 if | | 11 | 3 | 48 | 2 | 48 | | 12 | 1 | 96 | 2 | 0 | | 13 | 1 | 96 | 2 | 76 | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 |   <unchanged part omitted> |

**TP# 4-1A for TS38.213 [4]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 2 | 0 | | 4 | 1 | 48 | 1 | 14 | | 5 | 1 | 48 | 2 | 14 | | 6 | 1 | 48 | 1 | 28 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 2 | 0 | | 10 | 1 | 96 | 1 | 76 | | 11 | 1 | 96 | 2 | 76 | | 12 | 3 | 24 | 2 | -20 if  -21 if | | 13 | 3 | 48 | 2 | -20 if  -21 if | | 14 |  |  |  |  | | 15 |  |  |  |  |   <unchanged part omitted>  Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 2 | 0 | | 4 | 1 | 48 | 1 | 14 | | 5 | 1 | 48 | 2 | 14 | | 6 | 1 | 48 | 1 | 28 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 2 | 0 | | 10 | 1 | 96 | 1 | 76 | | 11 | 1 | 96 | 2 | 76 | | 12 | 3 | 24 | 2 | -20 if  -21 if | | 13 | 3 | 48 | 2 | -20 if  -21 if | | 14 | 3 | 96 | 2 | -20 if  -21 if | | 15 |  |  |  |  |   <unchanged part omitted>  Table 13-10C: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {960, 960} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 2 | 0 | | 4 | 1 | 48 | 1 | 14 | | 5 | 1 | 48 | 2 | 14 | | 6 | 1 | 48 | 1 | 28 | | 7 | 1 | 48 | 2 | 28 | | 8 | 3 | 24 | 2 | -20 if  -21 if | | 9 | 3 | 48 | 2 | -20 if  -21 if | | 10 |  |  |  |  | | 11 |  |  |  |  | | 12 |  |  |  |  | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  |   <unchanged part omitted> |

**TP# 4-1B for TS38.213 [11]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 14 | | 3 | 1 | 48 | 2 | 14 | | 4 | 3 | 24 | 2 | -20 if  -21 if | | 5 | 3 | 24 | 2 | 24 | | 6 | 3 | 48 | 2 | -20 if  -21 if | | 7 | 3 | 48 | 2 | 48 | | 8 | 1 | 48 | 1 | 0 | | 9 | 1 | 48 | 2 | 0 | | 10 | 1 | 48 | 1 | 28 | | 11 | 1 | 48 | 2 | 28 | | 12 | 1 | 96 | 2 | 0 | | 13 | 1 | 96 | 2 | 38 | | 14 | 1 | 96 | 2 | 76 | | 15 | Reserved |  |  |  |   Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 2 | 0 | | 4 | 1 | 48 | 1 | 14 | | 5 | 1 | 48 | 2 | 14 | | 6 | 1 | 48 | 1 | 28 | | 7 | 1 | 48 | 2 | 28 | | 8 | 3 | 24 | 2 | -20 if  -21 if | | 9 | 3 | 24 | 2 | 24 | | 10 | 3 | 48 | 2 | -20 if  -21 if | | 11 | 3 | 48 | 2 | 48 | | 12 | 1 | 96 | 2 | 0 | | 13 | 1 | 96 | 2 | 36 | | 14 | 1 | 96 | 2 | 72 | | 15 | 1 | 96 | 2 | 76 |   Table 13-10C: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {960, 960} kHz   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 2 | 0 | | 4 | 1 | 48 | 1 | 14 | | 5 | 1 | 48 | 2 | 14 | | 6 | 1 | 48 | 1 | 28 | | 7 | 1 | 48 | 2 | 28 | | 8 | 3 | 24 | 2 | -20 if  -21 if | | 9 | 3 | 24 | 2 | 24 | | 10 | 3 | 48 | 2 | -20 if  -21 if | | 11 | 3 | 48 | 2 | 48 | | 12 | 1 | 96 | 2 | 0 | | 13 | 1 | 96 | 2 | 36 | | 14 | 1 | 96 | 2 | 72 | | 15 | 1 | 96 | 2 | 76 | |

**TP# 4-1C for TS38.213 [12]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 48 | 1 | 0 | | 2 | 1 | 48 | 1 | 14 | | 3 | 1 | 48 | 1 | 28 | | 4 | 1 | 48 | 2 | 0 | | 5 | 1 | 48 | 2 | 14 | | 6 | 1 | 48 | 2 | 28 | | 7 | 1 | 96 | 1 | 0 | | 8 | 1 | 96 | 2 | 0 | | 9 | 3 | 24 | 2 | -20 if k\_ssb =0  -21 if k\_ssb >0 | | 10 | 3 | 48 | 2 | -20 if k\_ssb =0  -21 if k\_ssb >0 | | 11 |  |  |  |  | | 12 |  |  |  |  | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  |   Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 48 | 1 | 0 | | 2 | 1 | 48 | 1 | 14 | | 3 | 1 | 48 | 1 | 28 | | 4 | 1 | 48 | 2 | 0 | | 5 | 1 | 48 | 2 | 14 | | 6 | 1 | 48 | 2 | 28 | | 7 | 1 | 96 | 2 | 0 | | 8 | 1 | 96 | 2 | 38 | | 9 | 3 | 24 | 2 | -20 if k\_ssb =0  -21 if k\_ssb >0 | | 10 | 3 | 48 | 2 | -20 if k\_ssb =0  -21 if k\_ssb >0 | | 11 |  |  |  |  | | 12 |  |  |  |  | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  |   Table 13-10C: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {960, 960} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 2 | 0 | | 4 | 1 | 96 | 2 | 0 | | 5 | 3 | 24 | 2 | -20 if k\_ssb =0  -21 if k\_ssb >0 | | 6 | 3 | 48 | 2 | -20 if k\_ssb =0  -21 if k\_ssb >0 | | 7 |  |  |  |  | | 8 |  |  |  |  | | 9 |  |  |  |  | | 10 |  |  |  |  | | 11 |  |  |  |  | | 12 |  |  |  |  | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  | |

**TP# 4-1D for TS38.213 [13]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| **Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz for FR2-2**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 48 | 1 | 0 | | 2 | 1 | 48 | 1 | 14 | | 3 | 1 | 48 | 1 | 28 | | 4 | 1 | 48 | 2 | 0 | | 5 | 1 | 48 | 2 | 14 | | 6 | 1 | 48 | 2 | 28 | | 7 | 1 | 96 | 1 | 0 | | 8 | 1 | 96 | 2 | 0 | | 9 | 3 | 24 | 2 | -20 if  -21 if > 0 | | 10 | 3 | 24 | 2 | 24 | | 11 | 3 | 48 | 2 | -20 if  -21 if > 0 | | 12 | 3 | 48 | 2 | 48 | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  |   **Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz for FR2-2**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 48 | 1 | 0 | | 2 | 1 | 48 | 1 | 14 | | 3 | 1 | 48 | 1 | 28 | | 4 | 1 | 48 | 2 | 0 | | 5 | 1 | 48 | 2 | 14 | | 6 | 1 | 48 | 2 | 28 | | 7 | 1 | 96 | 2 | 0 | | 8 | 1 | 96 | 2 | 56 | | 9 | 3 | 24 | 2 | -20 if  -21 if > 0 | | 10 | 3 | 24 | 2 | 24 | | 11 | 3 | 48 | 2 | -20 if  -21 if > 0 | | 12 | 3 | 48 | 2 | 48 | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  |   **Table 13-10C: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {960, 960} kHz for FR2-2**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 2 | 0 | | 4 | 1 | 96 | 2 | 0 | | 5 | 1 | 96 | 2 | 56 | | 6 | 3 | 24 | 2 | -20 if  -21 if > 0 | | 7 | 3 | 24 | 2 | 24 | | 8 | 3 | 48 | 2 | -20 if  -21 if > 0 | | 9 | 3 | 48 | 2 | 48 | | 10 |  |  |  |  | | 11 |  |  |  |  | | 12 |  |  |  |  | | 13 |  |  |  |  | | 14 |  |  |  |  | | 15 |  |  |  |  | |

**TP# 4-1E for TS38.213 [16]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 2 | | 1 | 1 | 48 | 1 | 0 | | 2 | 1 | 48 | 1 | 28 | | 3 | 1 | 48 | 2 | 0 | | 4 | 1 | 48 | 2 | 28 | | 5 | 1 | 96 | 1 | 38 | | 6 | 1 | 96 | 2 | 38 | | 7 | 3 | 24 | 2 | -20 if ,  -21 if | | 8 | 3 | 24 | 2 | 24 | | 9 | 3 | 48 | 2 | -20 if ,  -21 if | | 10 | 3 | 48 | 2 | 48 | | 11 | Reserved | | | | | 12 | Reserved | | | | | 13 | Reserved | | | | | 14 | Reserved | | | | | 15 | Reserved | | | |   Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz or {960, 960} for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 1 | 14 | | 4 | 1 | 48 | 1 | 28 | | 5 | 1 | 48 | 2 | 0 | | 6 | 1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 1 | 76 | | 10 | 1 | 96 | 2 | 0 | | 11 | 1 | 96 | 2 | 76 | | 12 | 3 | 24 | 2 | -20 if ,  -21 if | | 13 | 3 | 24 | 2 | 24 | | 14 | 3 | 48 | 2 | -20 if ,  -21 if | | 15 | 3 | 48 | 2 | 48 |   ======================= Unchanged Text Omitted ============================= |

### Summary of Discussions

The following is a summary of company views on the CORESET#0 configuration in MIB.

* For 120 kHz
  + Finalize later once RAN4 finishes channelization: CATT, NTT Docomo
  + Multiplexing pattern 1 with 24 RBs:
    - 0 RB offset: Intel, Ericsson
    - 2 RB offset: Samsung
    - {0, 4} RB offset : Huawei/HiSilicon, vivo, Qualcomm
  + Multiplexing pattern 1 with 48 RBs:
    - 14 RB offset: Qualcomm
    - {0, 28} RB offset: Samsung
    - {0, 14, 28} RB offset: Huawei/HiliSicon, Intel, vivo, Ericsson
  + Multiplexing pattern 1 with 96 RBs:
    - 0 RB offset: Intel, Ericsson
    - {0, 76} RB offset: Huawei/HiSilicon, vivo
    - {0, 38, 76} RB offset: Nokia/NSB
    - 38 RB offset: Samsung
  + Multiplexing pattern 3 with 24 RB:
    - -20 or -21 (depending on k\_ssb) RB offset: Intel, vivo
    - {-20 or -21 (depending on k\_ssb) or 24} RB offset: Interdigital, Samsung, Ericsson, Qualcomm
  + Multiplexing pattern 3 with 48 RB:
    - -20 or -21 (depending on k\_ssb) RB offset: Intel, vivo
    - {-20 or -21 (depending on k\_ssb) or 48} RB offset: Interdigital, Samsung, Ericsson, Qualcomm
* For 480 kHz
  + Multiplexing pattern 1 with 24 RBs:
    - 0 RB offset: Intel, Ericsson
    - {0, 4} RB offset: Huawei/HiSilicon, vivo, Samsung, Qualcomm
  + Multiplexing pattern 1 with 48 RBs:
    - 14 RB offset: Qualcomm
    - {0, 14, 28} RB offset: Huawei/HiSilicon, Intel, vivo, Samsung, Ericsson
  + Multiplexing pattern 1 with 96 RBs:
    - {0, 38} RB offset: Intel
    - {0, 56} RB offset: Ericsson
    - {0, 76} RB offset: Huawei/HiSilicon, vivo, Samsung
    - {0, 36, 72, 76} RB offset: Nokia/NSB
  + Multiplexing pattern 3 with 24 RB:
    - -20 or -21 (depending on k\_ssb) RB offset: Intel, vivo
    - {-20 or -21 (depending on k\_ssb) or 24} RB offset: Interdigital, Ericsson, Qualcomm
  + Multiplexing pattern 3 with 48 RB:
    - -20 or -21 (depending on k\_ssb) RB offset: Intel, vivo
    - {-20 or -21 (depending on k\_ssb) or 48} RB offset: Interdigital, Ericsson, Qualcomm
* For 960 kHz
  + Multiplexing pattern 1 with 24 RBs:
    - {0, 4} RB offset: Huawei/HiSilicon, Intel, vivo, Samsung, Qualcomm, Ericsson
  + Multiplexing pattern 1 with 48 RBs:
    - 14 RB offset: Qualcomm
    - 0 RB offset: Intel, Ericsson
    - {0, 14, 28} RB offset: Huawei/HiSilicon, vivo, Samsung
  + Multiplexing pattern 1 with 96 RBs:
    - 0 RB offset: Intel
    - {0, 56} RB offset: Ericsson
    - {0, 76} RB offset: Huawei/HiSilicon, Samsung
  + Multiplexing pattern 3 with 24 RB:
    - -20 or -21 (depending on k\_ssb) RB offset: Intel, vivo
    - {-20 or -21 (depending on k\_ssb) or 24} RB offset: Interdigital, Samsung, Ericsson, Qualcomm
  + Multiplexing pattern 3 with 48 RB:
    - -20 or -21 (depending on k\_ssb) RB offset: Intel, vivo
    - {-20 or -21 (depending on k\_ssb) or 48} RB offset: Interdigital, Samsung, Ericsson, Qualcomm
* For the 57 – 66 GHz band, the SSB-CORESET0 offsets proposed in Section 5.1 for the floating channelization design are also valid for the fixed design, and no additional offset values need to be defined
  + Ericsson, [Intel]
* Additionally support 1 symbol duration 96 RB CORESET for 480 and 960 kHz for multiplexing pattern 1.
  + Intel

Discuss further on the RB offset values and the proposals discussed above.

### [CLOSED] 1st Round Discussion

It looks like few companies like Intel and Ericsson has provided some quantitative analysis of required RB offsets. Moderator thinks it will be highly useful if companies can provide some quantitative analysis of which RB offsets are required to support both licensed and unlicensed operation based on RAN4 LS.

Companies are asked to provide further comments (including preferences, or whether they can accept specific options) on the following summary (e.g. provide further information or quantitative analysis about reasons behind the RB offset)

* For 120 kHz
  + Finalize later once RAN4 finishes channelization: CATT~~, NTT Docomo~~
  + Multiplexing pattern 1 with 24 RBs:
    - 0 RB offset: Intel, Ericsson, NTT Docomo, CATT
    - 2 RB offset: Samsung
    - {0, 4} RB offset : Huawei/HiSilicon, vivo, Qualcomm, Nokia, Samsung, LG Electronics, Apple, Futurewei
  + Multiplexing pattern 1 with 48 RBs:
    - 14 RB offset: Qualcomm
    - {0, 28} RB offset: Samsung
    - {0, 14, 28} RB offset: Huawei/HiliSicon, Intel, vivo, Ericsson, Nokia, Samsung, LG Electronics, NTT Docomo, Apple, Futurewei, CATT
  + Multiplexing pattern 1 with 96 RBs:
    - 0 RB offset: Intel, Ericsson, NTT Docomo, CATT
    - {0, 76} RB offset: Huawei/HiSilicon, vivo, Samsung,
    - {0, 38, 76} RB offset: Nokia/NSB, Samsung
    - 38 RB offset: Samsung
  + Multiplexing pattern 3 with 24 RB:
    - -20 or -21 (depending on k\_ssb) RB offset: Intel, vivo, CATT
    - {-20 or -21 (depending on k\_ssb) or 24} RB offset: Interdigital, Samsung, Ericsson, Qualcomm, LG Electronics, NTT Docomo, Apple, Futurewei, Huawei/HiliSicon
  + Multiplexing pattern 3 with 48 RB:
    - -20 or -21 (depending on k\_ssb) RB offset: Intel, vivo, CATT
    - {-20 or -21 (depending on k\_ssb) or 48} RB offset: Interdigital, Samsung, Ericsson, Qualcomm, LG Electronics, NTT Docomo, Apple, Futurewei, Huawei/HiliSicon
* For 480 kHz
  + Multiplexing pattern 1 with 24 RBs:
    - 0 RB offset: Intel, Ericsson, NTT Docomo, CATT
    - {0, 4} RB offset: Huawei/HiSilicon, vivo, Samsung, Qualcomm, Nokia, LG Electronics, Apple, Futurewei
  + Multiplexing pattern 1 with 48 RBs:
    - 14 RB offset: Qualcomm
    - {0, 14, 28} RB offset: Huawei/HiSilicon, Intel, vivo, Samsung, Ericsson, Nokia, LG Electronics, NTT Docomo, Apple, Futurewei, CATT
  + Multiplexing pattern 1 with 96 RBs:
    - {0, 38} RB offset: Intel
    - {0, 56} RB offset: Ericsson
    - {0, 76} RB offset: Huawei/HiSilicon, vivo, Samsung
    - [{0, 36, 72, 76}] RB offset: Nokia/NSB
    - {0, x} RB offset, open to discuss on x value: NTT Docomo, CATT
  + Multiplexing pattern 3 with 24 RB:
    - -20 or -21 (depending on k\_ssb) RB offset: Intel, vivo, CATT
    - {-20 or -21 (depending on k\_ssb) or 24} RB offset: Interdigital, Ericsson, Qualcomm, Samsung, LG Electronics, NTT Docomo, Apple, Futurewei, Huawei/HiliSicon
  + Multiplexing pattern 3 with 48 RB:
    - -20 or -21 (depending on k\_ssb) RB offset: Intel, vivo, CATT
    - {-20 or -21 (depending on k\_ssb) or 48} RB offset: Interdigital, Ericsson, Qualcomm, Samsung, LG Electronics, NTT Docomo, Apple, Futurewei, Huawei/HiliSicon
* For 960 kHz
  + Multiplexing pattern 1 with 24 RBs:
    - {0, 4} RB offset: Huawei/HiSilicon, Intel, vivo, Samsung, Qualcomm, Ericsson, Nokia, LG Electronics, NTT Docomo, Apple, Futurewei, CATT
  + Multiplexing pattern 1 with 48 RBs:
    - 14 RB offset: Qualcomm
    - 0 RB offset: Intel, Ericsson, NTT Docomo
    - {0, 14, 28} RB offset: Huawei/HiSilicon, vivo, Samsung, Nokia, LG Electronics, Apple, Futurewei
  + Multiplexing pattern 1 with 96 RBs:
    - 0 RB offset: Intel, CATT
    - {0, 56} RB offset: Ericsson
    - {0, 76} RB offset: Huawei/HiSilicon, Samsung
    - {0, 36, 72, 76} RB offset: Nokia/NSB
    - {0, x} RB offset, open to discuss on x value: NTT Docomo
  + Multiplexing pattern 3 with 24 RB:
    - -20 or -21 (depending on k\_ssb) RB offset: Intel, vivo, CATT
    - {-20 or -21 (depending on k\_ssb) or 24} RB offset: Interdigital, Samsung, Ericsson, Qualcomm, LG Electronics, NTT Docomo, Futurewei, Huawei/HiliSicon
  + Multiplexing pattern 3 with 48 RB:
    - -20 or -21 (depending on k\_ssb) RB offset: Intel, vivo, CATT
    - {-20 or -21 (depending on k\_ssb) or 48} RB offset: Interdigital, Samsung, Ericsson, Qualcomm, LG Electronics, NTT Docomo, Futurewei, Huawei/HiliSicon

#### Proposal# 4-1

* Proposed Agreement:
  + The following table are used for set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120}, {480, 480}, and {960, 960} kHz for FR2-2.
    - Note: Values in [ ] are agreed as working assumption, and can be revisited once RAN4 finalizes the further details of the channelization.
  + Endorse TP#4-2 for TS38.213 from R1-2202502

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** |
| 0 | 1 | 24 | 2 | 0 |
| 1 | 1 | 24 | 2 | 4 |
| 2 | 1 | 48 | 1 | 0 |
| 3 | 1 | 48 | 1 | 14 |
| 4 | 1 | 48 | 1 | 28 |
| 5 | 1 | 48 | 2 | 0 |
| 6 | 1 | 48 | 2 | 14 |
| 7 | 1 | 48 | 2 | 28 |
| 8 | 1 | 96 | 1 | 0 |
| 9 | 1 | 96 | 1 | [56] |
| 10 | 1 | 96 | 2 | 0 |
| 11 | 1 | 96 | 2 | [56] |
| 12 | 3 | 24 | 2 | -20 if  -21 if > 0 |
| 13 | 3 | 24 | 2 | 24 |
| 14 | 3 | 48 | 2 | -20 if  -21 if > 0 |
| 15 | 3 | 48 | 2 | 48 |

#### TP# 4-2 for TS38.213

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 13 UE procedure for monitoring Type0-PDCCH CSS sets ======================= Unchanged Text Omitted =============================  Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120}, {480, 480}, or {960, 960} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | ~~48~~24 | ~~1~~2 | 4 | | 2 | 1 | 48 | ~~2~~1 | 0 | | 3 | 1 | ~~96~~48 | 1 | 14 | | 4 | 1 | ~~96~~48 | ~~2~~1 | 28 | | 5 | ~~3~~1 | ~~24~~48 | 2 | 0 | | 6 | ~~3~~1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 1 | 56 | | 10 | 1 | 96 | 2 | 0 | | 11 | 1 | 96 | 2 | 56 | | 12 | 3 | 24 | 2 | -20 if  -21 if > 0 | | 13 | 3 | 24 | 2 | 24 | | 14 | 3 | 48 | 2 | -20 if  -21 if > 0 | | 15 | 3 | 48 | 2 | 48 |   ~~Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz for FR2-2~~   |  |  |  |  |  | | --- | --- | --- | --- | --- | | ~~Index~~ | ~~SS/PBCH block and CORESET multiplexing pattern~~ | ~~Number of RBs~~ | ~~Number of Symbols~~ | ~~Offset (RBs)~~ | | ~~0~~ | ~~1~~ | ~~24~~ | ~~2~~ |  | | ~~1~~ | ~~1~~ | ~~48~~ | ~~1~~ |  | | ~~2~~ | ~~1~~ | ~~48~~ | ~~2~~ |  | | ~~3~~ | ~~1~~ | ~~96~~ | ~~2~~ |  | | ~~4~~ | ~~3~~ | ~~24~~ | ~~2~~ |  | | ~~5~~ | ~~3~~ | ~~48~~ | ~~2~~ |  | | ~~6~~ |  |  |  |  | | ~~7~~ |  |  |  |  | | ~~8~~ |  |  |  |  | | ~~9~~ |  |  |  |  | | ~~10~~ |  |  |  |  | | ~~11~~ |  |  |  |  | | ~~12~~ |  |  |  |  | | ~~13~~ |  |  |  |  | | ~~14~~ |  |  |  |  | | ~~15~~ |  |  |  |  |   ~~Table 13-10C: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {960, 960} kHz for FR2-2~~   |  |  |  |  |  | | --- | --- | --- | --- | --- | | ~~Index~~ | ~~SS/PBCH block and CORESET multiplexing pattern~~ | ~~Number of RBs~~ | ~~Number of Symbols~~ | ~~Offset (RBs)~~ | | ~~0~~ | ~~1~~ | ~~24~~ | ~~2~~ |  | | ~~1~~ | ~~1~~ | ~~48~~ | ~~1~~ |  | | ~~2~~ | ~~1~~ | ~~48~~ | ~~2~~ |  | | ~~3~~ | ~~1~~ | ~~96~~ | ~~2~~ |  | | ~~4~~ | ~~3~~ | ~~24~~ | ~~2~~ |  | | ~~5~~ | ~~3~~ | ~~48~~ | ~~2~~ |  | | ~~6~~ |  |  |  |  | | ~~7~~ |  |  |  |  | | ~~8~~ |  |  |  |  | | ~~9~~ |  |  |  |  | | ~~10~~ |  |  |  |  | | ~~11~~ |  |  |  |  | | ~~12~~ |  |  |  |  | | ~~13~~ |  |  |  |  | | ~~14~~ |  |  |  |  | | ~~15~~ |  |  |  |  |   ======================= Unchanged Text Omitted ============================= |

#### Company Comments

|  |  |
| --- | --- |
| Company | Comments |
| InterDigital | If multiplexing pattern 3 is supported in CORESET#0 configuration, we prefer to use the currently existing RB offset configuration in Rel. 16.  Therefore, we support two RB offset values for MUX 3. The two values could be (-20 if kssb=0, -21 based on kssb) and X, where X is the number of RBs in the respective CORESET#0 (can be 24 or 48 RBs).  In this way, the CORESET#0 could be multiplexed along with SSB in frequency domain, wherein the CORESET#0 RBs could have the option to be positioned preceding or following the respective SSB RBs. |
| Nokia | Update to the above summary our proposed ranges, if missing. For multiplexing pattern 3 case we did not have specific/dedicated proposal in our paper but in the formulated tables {-20/-21, 24} and {-20/-21, 48} were assumed, for 24RB and 48RB CORESET sizes, respectively.  We used fixed RF channel placement (given in Appendix A of our contribution in R1-2201662) to identify the possible channel locations i.e.   * + Distance between center of the channels being integer multiple of 960 kHz   + Guard bands of different RF channels are not overlapping   + For 100MHz channel bandwidth the channel raster step is minimized   + For 400MHz, 800MHz, 1600MHz and 2GHz channel bandwidths the channel raster locations are aligned to enable smooth CA operation and minimize the gap between channels   Based on these locations we evaluated the needed SS-raster positions and RB offsets for ‘fixed SS-raster’. For ‘floating SS-raster’ valid ARFCN was assumed for channel placement, and RB offsets were identified.  For multiplexing pattern 1 and CORESET size of 24RB and 48RB, it would seem that regardless of partially different assumptions, common offsets can be found. With multiplexing pattern 3, the offsets should be hopefully common.  Further discussion and alignment seems to be needed for 96RB case. |
| Samsung | We also provided the analysis on the minimum number of frequency offset required for each possible sync raster intervals discussed in RAN4, according to same principle used for Rel-15. The particular choices on the offset values, according to the minimum number of offsets, can be multiple, and we can be flexible on that point. We suggest to go with a conservative design as long as the total number of rows in the CORESET#0 configuration table doesn’t exceed 16. |
| Intel | Our analysis on the required RB offset in R1-2201688 is actually quite similar to Ericsson’s analysis. The only difference for multiplexing pattern 1 is {0 38} RB offset vs {0 56} RB offset for 96 PRB with 480/960 kHz case. From our understanding {0 56} should equally work ok for 480 kHz case, and 56 RB offset is not really needed for 960 kHz case. Other than this the analysis is pretty much identical.  While we don’t quite understand the need for additional RB offsets (other than what we have proposed) and how they provide additional optimization (since putting the SSB in the edge of the CORESET#0 is always a preferred approach due to providing the largest contiguous bandwidth for PDSCH), if companies really think additional values are needed, then we suggest having completely identical table (with 16 entries) for 120, 480, and 960 kHz.  Alternative 1) minimal set   * For 120 kHz   + Multiplexing pattern 1 with 24 RBs: 0 RB offset   + Multiplexing pattern 1 with 48 RBs: {0, 14, 28} RB offset   + Multiplexing pattern 1 with 96 RBs: 0 RB offset   + Multiplexing pattern 3 with 24 RB: -20 or -21 (depending on k\_ssb) RB offset   + Multiplexing pattern 3 with 48 RB: -20 or -21 (depending on k\_ssb) RB offset * For 480 kHz   + Multiplexing pattern 1 with 24 RBs: 0 RB offset   + Multiplexing pattern 1 with 48 RBs: {0, 14, 28} RB offset   + Multiplexing pattern 1 with 96 RBs: {0, 38} or {0, 56} RB offset   + Multiplexing pattern 3 with 24 RB: -20 or -21 (depending on k\_ssb) RB offset   + Multiplexing pattern 3 with 48 RB: -20 or -21 (depending on k\_ssb) RB offset * For 960 kHz   + Multiplexing pattern 1 with 24 RBs: {0, 4} RB offset   + Multiplexing pattern 1 with 48 RBs: 0 RB offset   + Multiplexing pattern 1 with 96 RBs: 0 RB offset   + Multiplexing pattern 3 with 24 RB: -20 or -21 (depending on k\_ssb) RB offset   + Multiplexing pattern 3 with 48 RB: -20 or -21 (depending on k\_ssb) RB offset   Alternative 2) identical table for 120/480/960 kHz   * Multiplexing pattern 1 with 24 RBs and 2 symbol: {0, 4} RB offset * Multiplexing pattern 1 with 48 RBs and {1, 2} symbols: {0, 14, 28} RB offset * Multiplexing pattern 1 with 96 RBs and {1, 2} symbols: {0, 76} RB offset * Multiplexing pattern 3 with 24 RB with 2 symbols: {-20 or -21 (depending on k\_ssb) or 24} RB offset   Multiplexing pattern 3 with 48 RB with 2 symbols: {-20 or -21 (depending on k\_ssb) or 48} RB offset |
| LG Electronics | We indicated our preference above.  For 96-RB CORESET#0, we think one (or two, if needed) RB offset value is sufficient and don’t prefer to optimize RB offset since it is not essential for FR2-2.  In addition, we think a single table for 480/960 kHz seems reasonable considering that initial access is not supported for 960 kHz (i.e., sync raster doesn’t need to be defined for 960 kHz). |
| DOCOMO | After some rough observation, we agree with Intel (and Ericsson) in general. Having Alt-1 (or Alt-2) as a starting point, we are ok with adding some other RB offsets (e.g. the ones supported in FR2-1), as long as Mux pattern 3 and Mux pattern 1 with 96 PRB are supported. |
| Apple | Our preference is indicated above.  In addition, we also prefer to define a single Table for all SCSs unless clear benefit or flexibility is identified to justify the need. |
| Futurewei | We indicated our preferences above. |
| Huawei, HiSilicon | RAN4 has made an agreement regarding supporting floating synch-raster for licensed and fixed synch raster for unlicensed band as well as the minimum gap between adjacent SS rasters in RAN4 101b-e. To our understanding, not much further progress is yet made about the channel raster design or further details of synch raster design.  Given the current state, we think that a detailed analysis regarding admissible RB offsets in RAN1 would be mainly contemplative and a concrete analysis of admissible RB offsets would only be possible if the exact locations of SS rasters and channel rasters for both licensed and unlicesend bands are already determined in RAN4.  On the other hand, given the large available BW and the synch/channel raster design flexibility, we think that it is likely that most of proposed sets of RB offsets in RAN1 can be accommodated by RAN4 synch/channel raster design. Therefore, we think that, at this point, a reasonable course of action is that RAN1 agrees (or reaches a WA) on the RB offsets based on RAN1 requirements/preference and send an LS to RAN4 regarding the agreed RB offsets in RAN1. Then, RAN4 can design synch/channel rasters in a way that each RB offset can be accommodated in at least one channel BW. If RAN4 design cannot provide such an accommodation, they can later notify RAN1 and RAN1 can update their WA regarding the inadmissible RB offsets.  Given above explanation, we think for CORESET#0 with 48 and 96 PRB with multiplexing pattern 1 that   1. It would be beneficial for gNB to transmit portion of discovery burst (e.g. SSB, Type0-PDCCH, RMSI PDSCH) with the same beam and as compact as possible in time and frequency domain to save LBT and beam switching overheads. Considering only frequency domain resource allocation type 1 is allowed for RMSI PDSCH, aligning SSB with the two extremities of CORESET#0 in the frequency domain frees up more contiguous RBs and allows a more flexible and potentially a larger allocation for RMSI PDSCH. 2. aligning SSB with the two extremities of CORESET#0 in the frequency domain even more important in 480/960 kHz as the beam switching delay may be too large to be absorbed in CP in 480/960 kHz SCS and, therefore, it is critical to have the possibility of transmitting SSB and its associated RMSI PDCCH/PDSCH in contiguous set of time/frequency resources without a need for a switching gap as shown in the following figure.     As such, we think it is quite important to support the following RB offsets for all three numerologies:   * For CORESET#0 with 48 RBs: The same as supported values in Table 13-8 of 38.213 in addition to **RB offset values of [0] and [28] RBs for multiplexing pattern 1**. * For CORESET#0 with 96 RBs: **RB offsets of [0] and [76] RBs for multiplexing pattern 1.** |
| Ericsson | We think a common table for all SCSs could be a reasonable way forward, and it seems as though there is room to cover all configurations with 16 table entries. See below proposal.  Note that when choosing the offsets for 96 RBs, we assumed a conservative value for the spectral utilization, i.e., not greater than 90% to leave some "wiggle" room for what RAN4 might decide. Any offsets that work for this conservative value, will also work for larger spectral utilization values. With this conservative value, we found the following offsets are needed for 96 RB:   * 120 kHz (requires 400 MHz channel bandwidth):   + Offset 0 is sufficient * 480 kHz (requires at least 800 MHz channel bandwidth)   + Two offsets needed. We found that [0 56] work. Intel suggested [0 38], but we found that 38 is too small assuming SU no greater than 90%. We also found that 76 is too large. * 960 kHz (requires at least 1600 MHz channel bandwidth):   + Two offsets needed. We found that [0 56] work. Intel suggested [0 76], and this works fine, but this value does not work for 480 kHz. Hence [0 56] seems like a good choice since it is common for both 480/960 kHz.   If companies need more time to check the offsets needed for 96 RB another WF could be to agree offsets [0 X] with value of X as FFS.   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 1 | 14 | | 4 | 1 | 48 | 1 | 28 | | 5 | 1 | 48 | 2 | 0 | | 6 | 1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 1 | 56 | | 10 | 1 | 96 | 2 | 0 | | 11 | 1 | 96 | 2 | 56 | | 12 | 3 | 24 | 2 | -20 if  -21 if > 0 | | 13 | 3 | 24 | 2 | 24 | | 14 | 3 | 48 | 2 | -20 if  -21 if > 0 | | 15 | 3 | 48 | 2 | 48 | |
| Moderator | Based on inputs so far, moderator put together Proposal #4-1.  While it seems the entries proposed in 4-1 may have additional RB offsets values, but doesn’t seem to have negative impact other than added entries for specification. Having a single table for all SCS seems to provide the benefit of being able to share the same table to simply specification.  Please check if Proposal #4-1 can be acceptable by all. |
| ZTE, Sanechips | We support proposal #4-1 |
| vivo | We support proposal #4-1 |
| LG Electronics | We are supportive of the direction of Proposal #4-1.  However, we haven’t agreed yet to support 1-symbol CORESET#0 with 96 PRBs for 480/960 kHz. In that sense, we prefer to have two separate tables where one is for 120 kHz SCS and the other is for 480/960 kHz SCS. |
| Lenovo | We are fine with proposal #4-1 |
| OPPO | According to LS from RAN4 (R4-2200081), both fixed sync raster for unlicensed bands and floating sync raster for licensed bands are considered, and it may have impacts on RB offset design. We think proposal #4-1 can be considered as working assumption and can be revisited based on RAN4 conclusion.   * Proposed ~~Agreement~~ working assumption:   + The following table are used for set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120}, {480, 480}, and {960, 960} kHz for FR2-2.     - ~~Note: Values in [ ] are agreed as working assumption, and can be revisited once RAN4 finalizes the further details of the channelization.~~   + Endorse TP#4-2 for TS38.213 from R1-2202502   + Note: this working assumption can be revisited once RAN4 finalizes the further details of the channelization. |
| Samsung | We are in general ok with Proposal #4-1, but cannot accept 56 as the RB offset as a working assumption. It’s obvious that resources are wasted in RMSI PDSCH resource allocation, and it’s not clear why 76 as the RB offset has an issue. We prefer to leave it as FFS and resolve it later.   * Proposed Agreement (modified by Samsung):   + The following table are used for set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120}, {480, 480}, and {960, 960} kHz for FR2-2.     - FFS: X     - ~~Note: Values in [ ] are agreed as working assumption, and can be revisited once RAN4 finalizes the further details of the channelization.~~   + Endorse TP#4-2 for TS38.213 from R1-2202502  |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 1 | 14 | | 4 | 1 | 48 | 1 | 28 | | 5 | 1 | 48 | 2 | 0 | | 6 | 1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 1 | X | | 10 | 1 | 96 | 2 | 0 | | 11 | 1 | 96 | 2 | X | | 12 | 3 | 24 | 2 | -20 if  -21 if > 0 | | 13 | 3 | 24 | 2 | 24 | | 14 | 3 | 48 | 2 | -20 if  -21 if > 0 | | 15 | 3 | 48 | 2 | 48 | |
| Ericsson | We support Proposal #4-1. We are also okay with Samsung's revision leaving the 2nd offset for 96 RB CORESET 0 as FFS. We are also fine to take the whole proposal as a working assumption. |
| Huawei, HiSilicon2 | As pointed out by LGE “1-symbol CORESET#0 with 96 PRBs for 480/960 kHz” was not supported. So, at this point, it is better to have a Table for 120 kHz and another Table for 480/960 kHz (note that latest version of 38.213 has already three separate tables for these numerologies).  As pointed out by multiple companies, we don’t see the use case of 56 RB offset for 96 RB CORESET and we think that 76 RB is a much better choice to allow a better resource usage of RMSI PDSCH and to facilitate having RMSI-PDCCH and (SSB/RMSI-PDSCH) in back-to-back symbols which, in turn, may avoid the need to perform LBT prior to RMSI-PDSCH and reduce the number of beam switching at the UE side.  If agreeing for 76 RB is not possible, in principle we can agree with the table provided by Samsung with the following changes:   1. Two different tables are provided for 120 kHz and 480/960 kHz where 480/960 kHz does not have a row for 96 RB with 1 symbol.   Add Candidate values for X={56,76}. |
| Intel | If we are going to add (in our opinion) redundant RB offset values for potential flexibility, we think we should just have 1 single table. From testing and specification perspective having another RB offset for a given entry is pretty much the same as introducing 1 symbol 96 PRB CORESET. If the goal isn’t to minimize the entries for each SCS, then we see no reason why we create multiple tables with all multiple redundant entries. |

### <Summary of 1st Round Discussion>

Companies seems to be generally ok with Proposal 4-1 with some modification such that the values can be revisited once the RAN4 channelization completes. Moderator has updated Proposal #4-1 to #4-1A and #4-1B based on comments. Also updated the TP to remove the FFS entry for now.

RAN1 should decide between Proposal #4-1A or #4-1B.

#### Proposal# 4-1A

* Proposed ~~Agreement~~Working Assumption:
  + The following table are used for set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120}, {480, 480}, and {960, 960} kHz for FR2-2.
    - ~~Note: Values in [ ] are agreed as working assumption, and can be revisited once RAN4 finalizes the further details of the channelization.~~
    - FFS: X, candidate values {56, 76}
  + Endorse TP#4-2A for TS38.213 from R1-2202502
  + Note: this working assumption can be revisited once RAN4 finalizes the further details of the channelization.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** |
| 0 | 1 | 24 | 2 | 0 |
| 1 | 1 | 24 | 2 | 4 |
| 2 | 1 | 48 | 1 | 0 |
| 3 | 1 | 48 | 1 | 14 |
| 4 | 1 | 48 | 1 | 28 |
| 5 | 1 | 48 | 2 | 0 |
| 6 | 1 | 48 | 2 | 14 |
| 7 | 1 | 48 | 2 | 28 |
| 8 | 1 | 96 | 1 | 0 |
| 9 | 1 | 96 | 1 | X |
| 10 | 1 | 96 | 2 | 0 |
| 11 | 1 | 96 | 2 | X |
| 12 | 3 | 24 | 2 | -20 if  -21 if > 0 |
| 13 | 3 | 24 | 2 | 24 |
| 14 | 3 | 48 | 2 | -20 if  -21 if > 0 |
| 15 | 3 | 48 | 2 | 48 |

#### TP# 4-2A for TS38.213

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 13 UE procedure for monitoring Type0-PDCCH CSS sets ======================= Unchanged Text Omitted =============================  Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120}, {480, 480}, or {960, 960} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | ~~48~~24 | ~~1~~2 | 4 | | 2 | 1 | 48 | ~~2~~1 | 0 | | 3 | 1 | ~~96~~48 | 1 | 14 | | 4 | 1 | ~~96~~48 | ~~2~~1 | 28 | | 5 | ~~3~~1 | ~~24~~48 | 2 | 0 | | 6 | ~~3~~1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 1 |  | | 10 | 1 | 96 | 2 | 0 | | 11 | 1 | 96 | 2 |  | | 12 | 3 | 24 | 2 | -20 if  -21 if > 0 | | 13 | 3 | 24 | 2 | 24 | | 14 | 3 | 48 | 2 | -20 if  -21 if > 0 | | 15 | 3 | 48 | 2 | 48 |   ~~Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz for FR2-2~~   |  |  |  |  |  | | --- | --- | --- | --- | --- | | ~~Index~~ | ~~SS/PBCH block and CORESET multiplexing pattern~~ | ~~Number of RBs~~ | ~~Number of Symbols~~ | ~~Offset (RBs)~~ | | ~~0~~ | ~~1~~ | ~~24~~ | ~~2~~ |  | | ~~1~~ | ~~1~~ | ~~48~~ | ~~1~~ |  | | ~~2~~ | ~~1~~ | ~~48~~ | ~~2~~ |  | | ~~3~~ | ~~1~~ | ~~96~~ | ~~2~~ |  | | ~~4~~ | ~~3~~ | ~~24~~ | ~~2~~ |  | | ~~5~~ | ~~3~~ | ~~48~~ | ~~2~~ |  | | ~~6~~ |  |  |  |  | | ~~7~~ |  |  |  |  | | ~~8~~ |  |  |  |  | | ~~9~~ |  |  |  |  | | ~~10~~ |  |  |  |  | | ~~11~~ |  |  |  |  | | ~~12~~ |  |  |  |  | | ~~13~~ |  |  |  |  | | ~~14~~ |  |  |  |  | | ~~15~~ |  |  |  |  |   ~~Table 13-10C: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {960, 960} kHz for FR2-2~~   |  |  |  |  |  | | --- | --- | --- | --- | --- | | ~~Index~~ | ~~SS/PBCH block and CORESET multiplexing pattern~~ | ~~Number of RBs~~ | ~~Number of Symbols~~ | ~~Offset (RBs)~~ | | ~~0~~ | ~~1~~ | ~~24~~ | ~~2~~ |  | | ~~1~~ | ~~1~~ | ~~48~~ | ~~1~~ |  | | ~~2~~ | ~~1~~ | ~~48~~ | ~~2~~ |  | | ~~3~~ | ~~1~~ | ~~96~~ | ~~2~~ |  | | ~~4~~ | ~~3~~ | ~~24~~ | ~~2~~ |  | | ~~5~~ | ~~3~~ | ~~48~~ | ~~2~~ |  | | ~~6~~ |  |  |  |  | | ~~7~~ |  |  |  |  | | ~~8~~ |  |  |  |  | | ~~9~~ |  |  |  |  | | ~~10~~ |  |  |  |  | | ~~11~~ |  |  |  |  | | ~~12~~ |  |  |  |  | | ~~13~~ |  |  |  |  | | ~~14~~ |  |  |  |  | | ~~15~~ |  |  |  |  |   ======================= Unchanged Text Omitted ============================= |

#### Proposal# 4-1B

* Proposed ~~Agreement~~Working Assumption:
  + The following tables are used for set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120}, {480, 480}, and {960, 960} kHz for FR2-2.
    - ~~Note: Values in [ ] are agreed as working assumption, and can be revisited once RAN4 finalizes the further details of the channelization.~~
    - FFS: X, candidate values {56, 76}
  + Endorse TP#4-2B for TS38.213 from R1-2202502
  + Note: this working assumption can be revisited once RAN4 finalizes the further details of the channelization.

Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz for FR2-2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** |
| 0 | 1 | 24 | 2 | 0 |
| 1 | 1 | 24 | 2 | 4 |
| 2 | 1 | 48 | 1 | 0 |
| 3 | 1 | 48 | 1 | 14 |
| 4 | 1 | 48 | 1 | 28 |
| 5 | 1 | 48 | 2 | 0 |
| 6 | 1 | 48 | 2 | 14 |
| 7 | 1 | 48 | 2 | 28 |
| 8 | 1 | 96 | 1 | 0 |
| 9 | 1 | 96 | 1 | X |
| 10 | 1 | 96 | 2 | 0 |
| 11 | 1 | 96 | 2 | X |
| 12 | 3 | 24 | 2 | -20 if  -21 if > 0 |
| 13 | 3 | 24 | 2 | 24 |
| 14 | 3 | 48 | 2 | -20 if  -21 if > 0 |
| 15 | 3 | 48 | 2 | 48 |

Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} or {960, 960} kHz for FR2-2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** |
| 0 | 1 | 24 | 2 | 0 |
| 1 | 1 | 24 | 2 | 4 |
| 2 | 1 | 48 | 1 | 0 |
| 3 | 1 | 48 | 1 | 14 |
| 4 | 1 | 48 | 1 | 28 |
| 5 | 1 | 48 | 2 | 0 |
| 6 | 1 | 48 | 2 | 14 |
| 7 | 1 | 48 | 2 | 28 |
| 8 |  |  |  |  |
| 9 |  |  |  |  |
| 10 | 1 | 96 | 2 | 0 |
| 11 | 1 | 96 | 2 | X |
| 12 | 3 | 24 | 2 | -20 if  -21 if > 0 |
| 13 | 3 | 24 | 2 | 24 |
| 14 | 3 | 48 | 2 | -20 if  -21 if > 0 |
| 15 | 3 | 48 | 2 | 48 |

#### TP# 4-2B for TS38.213

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 13 UE procedure for monitoring Type0-PDCCH CSS sets ======================= Unchanged Text Omitted =============================  Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | ~~48~~24 | ~~1~~2 | 4 | | 2 | 1 | 48 | ~~2~~1 | 0 | | 3 | 1 | ~~96~~48 | 1 | 14 | | 4 | 1 | ~~96~~48 | ~~2~~1 | 28 | | 5 | ~~3~~1 | ~~24~~48 | 2 | 0 | | 6 | ~~3~~1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 1 |  | | 10 | 1 | 96 | 2 | 0 | | 11 | 1 | 96 | 2 |  | | 12 | 3 | 24 | 2 | -20 if  -21 if > 0 | | 13 | 3 | 24 | 2 | 24 | | 14 | 3 | 48 | 2 | -20 if  -21 if > 0 | | 15 | 3 | 48 | 2 | 48 |   Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} or {960, 960} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | ~~48~~24 | ~~1~~2 | 4 | | 2 | 1 | 48 | ~~2~~1 | 0 | | 3 | 1 | ~~96~~48 | 2 | 14 | | 4 | ~~3~~1 | ~~24~~48 | 2 | 28 | | 5 | ~~3~~1 | 48 | 2 | 0 | | 6 | ~~3~~1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 |  |  |  |  | | 9 |  |  |  |  | | 10 | 1 | 96 | 2 | 0 | | 11 | 1 | 96 | 2 |  | | 12 | 3 | 24 | 2 | -20 if  -21 if > 0 | | 13 | 3 | 24 | 2 | 24 | | 14 | 3 | 48 | 2 | -20 if  -21 if > 0 | | 15 | 3 | 48 | 2 | 48 |   ~~Table 13-10C: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {960, 960} kHz for FR2-2~~   |  |  |  |  |  | | --- | --- | --- | --- | --- | | ~~Index~~ | ~~SS/PBCH block and CORESET multiplexing pattern~~ | ~~Number of RBs~~ | ~~Number of Symbols~~ | ~~Offset (RBs)~~ | | ~~0~~ | ~~1~~ | ~~24~~ | ~~2~~ |  | | ~~1~~ | ~~1~~ | ~~48~~ | ~~1~~ |  | | ~~2~~ | ~~1~~ | ~~48~~ | ~~2~~ |  | | ~~3~~ | ~~1~~ | ~~96~~ | ~~2~~ |  | | ~~4~~ | ~~3~~ | ~~24~~ | ~~2~~ |  | | ~~5~~ | ~~3~~ | ~~48~~ | ~~2~~ |  | | ~~6~~ |  |  |  |  | | ~~7~~ |  |  |  |  | | ~~8~~ |  |  |  |  | | ~~9~~ |  |  |  |  | | ~~10~~ |  |  |  |  | | ~~11~~ |  |  |  |  | | ~~12~~ |  |  |  |  | | ~~13~~ |  |  |  |  | | ~~14~~ |  |  |  |  | | ~~15~~ |  |  |  |  |   ======================= Unchanged Text Omitted ============================= |

### [ACTIVE] 2nd Round Discussion

Among the two potential way forward (Proposal #4-1A or #4-1B), based on feedback so far Proposal #4-1A seems to have the highest chance for getting something finalized.

Can companies check Proposal **#4-1A** (and corresponding **TP#4-2A**) and provide comments? Moderator would like to urge companies to be in compromising spirit and try to focus on constructive inputs so that this issue can be resolved before end of meeting.

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | Fine with Proposal #4-1A and TP #4-2A |
| LG Electronics | In general, we prefer to have the minimal number of rows for 96-RB CORESET#0 which is not essential for FR2-2. In that sense, we suggest to change the following FFS bullet.   * + - FFS: whether/how to define X, if defined, candidate values {56, 76}   Between Proposal #4-1A and #4-1B, we prefer Proposal #4-1B which is aligned with the previous working assumptions. When it comes to the corresponding TP, we suggest to totally remove the rows for 96-RB CORESET#0 with X, e.g.,  Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | ~~48~~24 | ~~1~~2 | 4 | | 2 | 1 | 48 | ~~2~~1 | 0 | | 3 | 1 | ~~96~~48 | 1 | 14 | | 4 | 1 | ~~96~~48 | ~~2~~1 | 28 | | 5 | ~~3~~1 | ~~24~~48 | 2 | 0 | | 6 | ~~3~~1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 2 | 0 | | 10 | 3 | 24 | 2 | -20 if  -21 if > 0 | | 11 | 3 | 24 | 2 | 24 | | 12 | 3 | 48 | 2 | -20 if  -21 if > 0 | | 13 | 3 | 48 | 2 | 48 | | 14 | Reserved | | | | | 15 | Reserved | | | | |
| Ericsson | Support Proposal #4-1A and TP #4-2A  We think it is quite attractive to a unified solution across all SCSs and finish this topic (aside from the value of X), rather than splitting into two tables and having further discussions on fine tuning. |
| Nokia\_2 | We are OK with Proposal# 4-1A.  We are also fine with TP# 4-2A for TS38.213. Of course we could agree common offset values and leave the implementation to the Editor, but as said, OK with this approach as well. |
| ZTE, Sanechips | We prefer to use a single table for all supported SCSs in FR2-2 unless there is a strong motivation to define separate tables, so we support Proposal# 4-1A and TP# 4-2A |
| OPPO | Fine with Proposal #4-1A and TP #4-2A |
| Samsung | We support Proposal# 4-1A and TP# 4-2A, and one unified table for all SCSs is the best.  Regarding Proposal# 4-1B and TP# 4-2B, if we design the table for {120,120} and {480.480}/{960,960} separately, we suggest to use X1 and X2 in two different tables, since there seems no technical justification that the offset values have to be the same, if we design them separately.  Regarding LG’s comment to remove the row with X, we don’t support. Although the value of X is FFS, we believe there is a majority view that at least two offsets are needed for 96 RBs (we saw this from companies’ analysis), and removing such row is against this intention. |
| InterDigital | We support Proposal #4-1A and TP #4-2A in order to have the same configuration table for all supported SCS. |
| Moderator | Seems like companies to gravitating toward having a single table for simplicity and flexibility.  @LGE do you think we can live with Proposal #4-1A and TP #4-2A? I also tend to agree, the purpose of having X was not to remove them from specification but eventually fill in the values. |
| Sharp | We also support Proposal# 4-1A and TP# 4-2A for the unified design. |
| vivo | Fine with Proposal #4-1A and TP #4-2A |
| LG Electronics | We are fine to have a common table for all SCSs. However, as we commented earlier, we have a concern to have rows corresponding to X RB offset which is uncertain at this stage.   * 96 RB CORESET#0 is not essential for FR2-2 since it cannot be supported for minimum channel bandwidth. * The necessity on 2 RB offset values has not been justified yet since RAN4 didn’t finalize channel/sync raster design. * It would be a safer choice to have two reserved states.   Considering those, we suggest the following changes. Proposal# 4-1A  * Proposed ~~Agreement~~Working Assumption:   + The following table are used for set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120}, {480, 480}, and {960, 960} kHz for FR2-2.     - ~~Note: Values in [ ] are agreed as working assumption, and can be revisited once RAN4 finalizes the further details of the channelization.~~     - FFS: whether/how to define X, if defined, candidate values {56, 76}   + Endorse TP#4-2A for TS38.213 from R1-2202502   + Note: this working assumption can be revisited once RAN4 finalizes the further details of the channelization.  |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 1 | 14 | | 4 | 1 | 48 | 1 | 28 | | 5 | 1 | 48 | 2 | 0 | | 6 | 1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 1 | X | | 10 | 1 | 96 | 2 | 0 | | 11 | 1 | 96 | 2 | X | | 12 | 3 | 24 | 2 | -20 if  -21 if > 0 | | 13 | 3 | 24 | 2 | 24 | | 14 | 3 | 48 | 2 | -20 if  -21 if > 0 | | 15 | 3 | 48 | 2 | 48 |  TP# 4-2A for TS38.213  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 13 UE procedure for monitoring Type0-PDCCH CSS sets ======================= Unchanged Text Omitted =============================  Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120}, {480, 480}, or {960, 960} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | ~~48~~24 | ~~1~~2 | 4 | | 2 | 1 | 48 | ~~2~~1 | 0 | | 3 | 1 | ~~96~~48 | 1 | 14 | | 4 | 1 | ~~96~~48 | ~~2~~1 | 28 | | 5 | ~~3~~1 | ~~24~~48 | 2 | 0 | | 6 | ~~3~~1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 2 | 0 | | 10 | 3 | 24 | 2 | -20 if  -21 if > 0 | | 11 | 3 | 24 | 2 | 24 | | 12 | 3 | 48 | 2 | -20 if  -21 if > 0 | | 13 | 3 | 48 | 2 | 48 | | 14 | Reserved | | | | | 15 | Reserved | | | |   ~~Table 13-10B: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz for FR2-2~~   |  |  |  |  |  | | --- | --- | --- | --- | --- | | ~~Index~~ | ~~SS/PBCH block and CORESET multiplexing pattern~~ | ~~Number of RBs~~ | ~~Number of Symbols~~ | ~~Offset (RBs)~~ | | ~~0~~ | ~~1~~ | ~~24~~ | ~~2~~ |  | | ~~1~~ | ~~1~~ | ~~48~~ | ~~1~~ |  | | ~~2~~ | ~~1~~ | ~~48~~ | ~~2~~ |  | | ~~3~~ | ~~1~~ | ~~96~~ | ~~2~~ |  | | ~~4~~ | ~~3~~ | ~~24~~ | ~~2~~ |  | | ~~5~~ | ~~3~~ | ~~48~~ | ~~2~~ |  | | ~~6~~ |  |  |  |  | | ~~7~~ |  |  |  |  | | ~~8~~ |  |  |  |  | | ~~9~~ |  |  |  |  | | ~~10~~ |  |  |  |  | | ~~11~~ |  |  |  |  | | ~~12~~ |  |  |  |  | | ~~13~~ |  |  |  |  | | ~~14~~ |  |  |  |  | | ~~15~~ |  |  |  |  |   ~~Table 13-10C: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {960, 960} kHz for FR2-2~~   |  |  |  |  |  | | --- | --- | --- | --- | --- | | ~~Index~~ | ~~SS/PBCH block and CORESET multiplexing pattern~~ | ~~Number of RBs~~ | ~~Number of Symbols~~ | ~~Offset (RBs)~~ | | ~~0~~ | ~~1~~ | ~~24~~ | ~~2~~ |  | | ~~1~~ | ~~1~~ | ~~48~~ | ~~1~~ |  | | ~~2~~ | ~~1~~ | ~~48~~ | ~~2~~ |  | | ~~3~~ | ~~1~~ | ~~96~~ | ~~2~~ |  | | ~~4~~ | ~~3~~ | ~~24~~ | ~~2~~ |  | | ~~5~~ | ~~3~~ | ~~48~~ | ~~2~~ |  | | ~~6~~ |  |  |  |  | | ~~7~~ |  |  |  |  | | ~~8~~ |  |  |  |  | | ~~9~~ |  |  |  |  | | ~~10~~ |  |  |  |  | | ~~11~~ |  |  |  |  | | ~~12~~ |  |  |  |  | | ~~13~~ |  |  |  |  | | ~~14~~ |  |  |  |  | | ~~15~~ |  |  |  |  |   ======================= Unchanged Text Omitted ============================= | |
| Huawei, HiSilicon | We can support #4-1A and TP #4-2A for the sake of progress.  Editorial change for #4-1A: The following table ~~are~~ is used for set of resource blocks… |

## 2.5 NR Carrier RSSI measurement

* From [16] Samsung
  + For 480 and 960 kHz:
    - Support the following 4 configurations for NR carrier RSSI measurement:
    - Configuration #0: {0, 1};
    - Configuration #1: {0, 1, …, 5};
    - Configuration #2: {0, 1, …, 8};
    - Configuration #3: {0, 1, …, 12};
  + Adopt TP#5-1 for TS 38.215.

#### TP# 5-1 for TS38.215 [16]

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 5.1.3 SS reference signal received quality (SS-RSRQ)  ======================== Unchanged Text Omitted ===========================  Table 5.1.3-1: NR Carrier RSSI measurement symbols   |  |  | | --- | --- | | **OFDM signal indication *endSymbol*** | **Symbol indexes** | | | 0 | {0,1} | | 1 | For 480 kHz and 960 kHz {0,1,2,..,10,12}; otherwise {0,1,2,..,10,11} | | 2 | {0,1,2,…, 5} | | 3 | For 480 kHz and 960 kHz {0,1,2,..,8}; otherwise {0,1,2,…, 7} |   ========================= Unchanged Text Omitted ============================== |

### Summary of Discussions

Updates to NR RSSI has been discussed in the last two meetings. However, the proposal was not agreeable and RAN1 was not able to conclude previously. Given the ample time to discuss and agree to the proposal, moderator suggests unless there is new compelling evidence or information, we skip the discussion and close the issue for Rel-17.

Moderator asks the proponent companies to provide inputs to concerns raised from the previous meetings that stopped RAN1 to agree on the proposal.

### [CLOSED] 1st Round Discussion

Moderator asks the proponent companies to provide inputs to concerns raised from the previous meetings that stopped RAN1 to agree on the proposal. Companies are asked to provide further comments on the proposal.

#### TP# 5-1A for TS38.215 [16]

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 5.1.3 SS reference signal received quality (SS-RSRQ)  ======================== Unchanged Text Omitted ===========================  Table 5.1.3-1: NR Carrier RSSI measurement symbols   |  |  | | --- | --- | | **OFDM signal indication *endSymbol*** | **Symbol indexes** | | | 0 | {0,1} | | 1 | For 480 kHz and 960 kHz {0,1,2,..,10,12}; otherwise {0,1,2,..,10,11} | | 2 | {0,1,2,…, 5} | | 3 | {0,1,2,…, 7} |   ========================= Unchanged Text Omitted ============================== |

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | As commented in the last meeting, we are ok with compromising to the following TP. Whether this change is essential or optimization is indeed subject, and we believe this change is beneficial and without any technical drawback. We would encourage more companies to reconsider this issue and reach a consensus.  ===================== Unchanged Text Omitted ===========================  Table 5.1.3-1: NR Carrier RSSI measurement symbols   |  |  | | --- | --- | | **OFDM signal indication *endSymbol*** | **Symbol indexes** | | | 0 | {0,1} | | 1 | For 480 kHz and 960 kHz {0,1,2,..,10,12}; otherwise {0,1,2,..,10,11} | | 2 | {0,1,2,…, 5} | | 3 | {0,1,2,…, 7} |   ==================== Unchanged Text Omitted ============================== |
| Intel | Support TP# 5-1 to align the design principles of SSB placement pattern and RSSI measurement pattern between Rel-17 and previous NR releases. |
| DOCOMO | Given that there is no drawback, we think it would be ok to support the TP#5-1. Samsung’s compromise is also fine. |
| Huawei/HiSilicon | We don’t see the need for the proposal. As discussed in the last meeting, the proposal aim to include the SSB symbols in RSSI-measurement period. The advantage of such inclusion is that SSB symbols are guaranteed to be DL symbols and the RSSI measurement on these symbols is not contaminated by UL traffic. However, the very fact that the RSSI measurement symbols necessarily include SSB symbols already distort the measurement as the incurred interference from DL traffic on a “SSB-free” symbol is substantially different from the incurred interference from DL traffic on a SSB symbol.  In short, the TP is enhancement at best. However, if we are the only company opposing it, we can accept it. |
| Moderator | Added TP#5-1A based on Samsung’s suggestion. We can maybe quickly check if all other companies are also ok with the TP during GTW. |
| ZTE, Sanechips | We think it is just an optimization issue. But if majority companies agree to solve this issue, we can also accept TP# 5-1A. |

### <Summary of 1st Round Discussion>

Moderator suggests checking to if there are major concerns with TP#5-1A. If possible, perform a quick check during GTW.

### [ACTIVE] 2nd Round Discussion

During a quick check in GTW, Nokia still has questions/doubts on the proposed change. We can try to check further but at least following companies thought the proposal was some optimization.

* Huawei, ZTE, Nokia

Please comment if other companies share the same concern. Please comment companies (especially the three companies above) are ok to agree to TP#5-1A (or TP#5-1). If there are still concerns, moderator suggest closing the discussion for Rel-17 since this has been discussed for last three meetings.

|  |  |
| --- | --- |
| Company | Comments |
| Nokia\_2 | Firstly, apologizes for the confusing comments in the GTW. What I meant to say/ask was that going from 11 symbols (not bits) to 12 symbols for RSSI, accounting the RAN4 accuracy requirements, might not result significant difference in the RSRQ. That being said, I don’t have technical issue aligning the RSSI symbols with the selected SSB pattern as proposed by the TP. |
| ZTE, Sanechips | As we commented before, we can accept it if majority companies agree to TP# 5-1A or TP#5-1. |
| InterDigital | We are ok with TP #5-1A. |
| Moderator | Let’s wait for Huawei’s further comments, to see if they can live with TP#5-1A or not. If Huawei also is ok, I will suggest the TP for email approval (along with other stable proposals) |
|  |  |
| Huawei, HiSilicon | We can support TP# 5-1A as a compromise. |

## 2.6 PRACH

* From [19] LG Electronics,
  + Update the Table 6.3.3.2-1 in TS 38.211 as in TP#6-1

#### TP# 6-1 for TS38.211 [19]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Table 6.3.3.2-1: Supported combinations of and , and the corresponding value of .**   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | **for PRACH** | **for PUSCH** | **, allocation expressed in number of RBs for PUSCH** |  | | 839 | 1.25 | 15 | 6 | 7 | | 839 | 1.25 | 30 | 3 | 1 | | 839 | 1.25 | 60 | 2 | 133 | | 839 | 5 | 15 | 24 | 12 | | 839 | 5 | 30 | 12 | 10 | | 839 | 5 | 60 | 6 | 7 | | 139 | 15 | 15 | 12 | 2 | | 139 | 15 | 30 | 6 | 2 | | 139 | 15 | 60 | 3 | 2 | | 139 | 30 | 15 | 24 | 2 | | 139 | 30 | 30 | 12 | 2 | | 139 | 30 | 60 | 6 | 2 | | 139 | 60 | 60 | 12 | 2 | | 139 | 60 | 120 | 6 | 2 | | 139 | 120 | 60 | 24 | 2 | | 139 | 120 | 120 | 12 | 2 | | 139 | 120 | 480 | 3 | 1 | | 139 | 120 | 960 | 2 | 23 | | 139 | 480 | 120 | ~~48~~47 | 1~~2~~ | | 139 | 480 | 480 | 12 | 2 | | 139 | 480 | 960 | 6 | 2 | | 139 | 960 | 120 | 94~~96~~ | ~~2~~1 | | 139 | 960 | 480 | 24 | 2 | | 139 | 960 | 960 | 12 | 2 | | 571 | 30 | 15 | 96 | 2 | | 571 | 30 | 30 | 48 | 2 | | 571 | 30 | 60 | 24 | 2 | | 571 | 120 | 120 | 48 | 2 | | 571 | 120 | 480 | 12 | 1 | | 571 | 120 | 960 | 7 | 47 | | 571 | 480 | 120 | 191~~192~~ | 1~~2~~ | | 571 | 480 | 480 | 48 | 2 | | 571 | 480 | 960 | 24 | 2 | | 1151 | 15 | 15 | 96 | 1 | | 1151 | 15 | 30 | 48 | 1 | | 1151 | 15 | 60 | 24 | 1 | | 1151 | 120 | 120 | 97 | 6 | | 1151 | 120 | 480 | 25 | 23 | | 1151 | 120 | 960 | 13 | 45 | |

### Summary of Discussions

Updates to NR PRACH table has been discussed in the last meetings. However, the proposal was not agreeable and RAN1 was not able to conclude previously. Given that this is issue being revisited, moderator suggests unless there is new compelling evidence or information, we skip the discussion and close the issue for Rel-17.

Moderator asks the proponent companies to provide inputs to concerns raised from the previous meetings that stopped RAN1 to agree on the proposal.

### [CLOSED] 1st Round Discussion

Moderator asks the proponent companies to provide inputs to concerns raised from the previous meetings that stopped RAN1 to agree on the proposal. Companies are asked to provide further comments on the proposal.

|  |  |
| --- | --- |
| Company | Comments |
| Intel | As mentioned in previous RAN1 meeting, we don’t think the changes are needed. They seem minor optimization at best, and potentially reduces guard band which are generally useful in implementation. |
| LG Electronics | In RAN1#107-e meeting, it was pointed out by ZTE that can still work well. In this regard, we found that it is possible to reduce the number of RBs for PUSCH, , in a specific combination of PRACH sequence length and PRACH/PUSCH SCS by replacing with . By reducing the wasted number of RB, , there are the following advantages:  1)  Can increase the number of RBs available for PUSCH transmission which is FDMed with PRACH.  2) Can increase the maximum number of FDMed ROs given the number of RBs within the bandwidth part. |
| Huawei/HiSilicon | Agree with Intel |
| CATT | Agree with Intel/HW |
| ZTE, Sanechips | Agree with Intel |

### <Summary of 1st Round Discussion>

TP#6-1 does not seem agreeable. Moderator suggest closing the discussion for RAN1#108-e.

### [ACTIVE] 2nd Round Discussion

While it seems there are several companies who think the changes are not essential at this stage. Moderator can try one more time to ask companies for comments if they changed their mind and also ask LGE to provide further compelling information to persuade opposing companies.

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | We also believe this change is not needed. |
| LG Electronics | We still believe that it is beneficial to reduce the number of RBs for PUSCH by replacing with . But if the majority of views think it's not essential, we're fine with it. |
| Mediatek | We also don’t see the change is necessary |
| ZTE, Sanechips | We still think that change is not needed |
| Samsung | We agree with comment that this issue is not that essential. |
| Huawei, HiSilicon | We still don’t think it is needed to change the Table. This Table has already optimized multiple times. |

## 2.7 Editorial Aspects

* From [2] Futurewei:
  + Change the Draft 38.213 h00 text “For operation without shared spectrum channel access, in FR1 and FR2, and for operation with shared spectrum channel access in FR2-2” to “For operation without shared spectrum channel access, in FR1 and FR2, and for operation in FR2-2”
* From [7] ZTE/Sanechips
  + For PRACH slot index for 480 and 960 kHz, adopt TP#7-2 in TS 38.211.
* From [10] Panasonic
  + Adopt TP#7-3, #7-4

**TP# 7-1 for TS38.213 [10]**

|  |
| --- |
| 4.1 Cell search ============= Unchanged Text Omitted =============  - For operation without shared spectrum channel access, in FR1 and FR2, and for operation ~~with shared spectrum channel access~~ in FR2-2  - For operation with shared spectrum channel access in FR1, for and 15 kHz SCS of SS/PBCH blocks and for and 30 kHz SCS of SS/PBCH blocks  ============= Unchanged Text Omitted ===================== |

**TP# 7-2 for TS38.211 [7]**

|  |
| --- |
| **5.3.2 OFDM baseband signal generation for PRACH**  < Unchanged parts are omitted >  where  -  is given by the parameter "starting symbol" in Tables 6.3.3.2-2 to 6.3.3.2-4;  -  is the PRACH transmission occasion within the PRACH slot, numbered in increasing order from 0 to  within a RACH slot where  is given Tables 6.3.3.2-2 to 6.3.3.2-4 for and fixed to 1 for ;  -  is given by Tables 6.3.3.2-2 to 6.3.3.2-4;  -  is given by  - if kHz, then  - if kHz and either of "Number of PRACH slots within a subframe" in Tables 6.3.3.2-2 to 6.3.3.2-3 or "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then , otherwise  *{indent backwards here}*- if kHz and *{next paragraph here}*  - the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then for kHz and for kHz  *{indent forwards here}*- the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 2, then for kHz and for kHz.  < Unchanged parts are omitted > |

**TP# 7-3 for TS38.211 [10]**

|  |
| --- |
| 7.4.3.1 Time-frequency structure of an SS/PBCH block ============= Unchanged Text Omitted =============  - For operation without shared spectrum channel access, and for operation with shared spectrum channel access in FR2-2, the 4 least significant bits of  are given by the higher-layer parameter *ssb-SubcarrierOffset* and for FR1 the most significant bit of  is given by in the PBCH payload as defined in clause 7.1.1 of [4, TS 38.212].  - For operation with shared spectrum channel access in FR1, the 4 least significant bits of are given by the higher-layer parameter *ssb-SubcarrierOffset* and the most significant bit of is given by in the PBCH payload as defined in clause 7.1.1 of [4, TS 38.212]. If , ; otherwise, , and if *ssb-SubcarrierOffset* is not provided, is derived from the frequency difference between the SS/PBCH block and Point A.  ============= Unchanged Text Omitted ===================== |

**TP# 7-4 for TS38.213 [10]**

|  |
| --- |
| 13 UE procedure for monitoring Type0-PDCCH CSS sets  ============= Unchanged Text Omitted =============  For operation without shared spectrum channel access, and for operation with shared spectrum channel access in FR2-2, a UE assumes that the offset in Tables 13-1 through 13-10C is defined with respect to the SCS of the CORESET for Type0-PDCCH CSS set from the smallest RB index of the CORESET for Type0-PDCCH CSS set to the smallest RB index of the common RB overlapping with the first RB of the corresponding SS/PBCH block. The SCS of the CORESET for Type0-PDCCH CSS set is provided by *subCarrierSpacingCommon* for FR1 and FR2-1 and same as the SCS of the corresponding SS/PBCH block for FR2-2. In Tables 13-7, 13-8, and 13-10 is defined in [4, TS 38.211].  ============= Unchanged Text Omitted ===================== |

### Summary of Discussions

The suggested updates in TP#7-1, 7-2, 7-3, and 7-4 all seem reasonable editorial changes that fixed ambiguity and adds clarity to specification. Moderator asks companies to review the TP and comment if they are acceptable.

### [CLOSED] 1st Round Discussion

Moderator asks companies to check on TP#7-1, #7-2, #7-3, and #7-4 and provide comments on them.

#### TP# 7-2A for TS38.21

|  |
| --- |
| **5.3.2 OFDM baseband signal generation for PRACH**  < Unchanged parts are omitted >  where  -  is given by the parameter "starting symbol" in Tables 6.3.3.2-2 to 6.3.3.2-4;  -  is the PRACH transmission occasion within the PRACH slot, numbered in increasing order from 0 to  within a RACH slot where  is given Tables 6.3.3.2-2 to 6.3.3.2-4 for and fixed to 1 for ;  -  is given by Tables 6.3.3.2-2 to 6.3.3.2-4;  -  is given by  - if kHz, then  - if kHz and either of "Number of PRACH slots within a subframe" in Tables 6.3.3.2-2 to 6.3.3.2-3 or "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then , otherwise  *{indent backwards here}*- if kHz and ~~- the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then for kHz and for kHz~~  - the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then for kHz and for kHz  - the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 2, then for kHz and for kHz.  < Unchanged parts are omitted > |

#### TP# 7-3A for TS38.211

|  |
| --- |
| 7.4.3.1 Time-frequency structure of an SS/PBCH block ============= Unchanged Text Omitted =============  - For operation without shared spectrum channel access in all frequency ranges and for operation with shared spectrum channel access in FR2-2, the 4 least significant bits of  are given by the higher-layer parameter *ssb-SubcarrierOffset* and for FR1 the most significant bit of  is given by in the PBCH payload as defined in clause 7.1.1 of [4, TS 38.212].  - For operation with shared spectrum channel access in FR1, the 4 least significant bits of are given by the higher-layer parameter *ssb-SubcarrierOffset* and the most significant bit of is given by in the PBCH payload as defined in clause 7.1.1 of [4, TS 38.212]. If , ; otherwise, , and if *ssb-SubcarrierOffset* is not provided, is derived from the frequency difference between the SS/PBCH block and Point A.  ============= Unchanged Text Omitted ===================== |

#### TP# 7-4A for TS38.213

|  |
| --- |
| 13 UE procedure for monitoring Type0-PDCCH CSS sets  ============= Unchanged Text Omitted =============  For operation without shared spectrum channel access in all frequency ranges and for operation with shared spectrum channel access in FR2-2, a UE assumes that the offset in Tables 13-1 through 13-10C is defined with respect to the SCS of the CORESET for Type0-PDCCH CSS set from the smallest RB index of the CORESET for Type0-PDCCH CSS set to the smallest RB index of the common RB overlapping with the first RB of the corresponding SS/PBCH block. The SCS of the CORESET for Type0-PDCCH CSS set is provided by *subCarrierSpacingCommon* for FR1 and FR2-1 and same as the SCS of the corresponding SS/PBCH block for FR2-2. In Tables 13-7, 13-8, and 13-10 is defined in [4, TS 38.211].  ============= Unchanged Text Omitted ===================== |

|  |  |
| --- | --- |
| Company | Comments |
| InterDigtial | We support moderator’s assessment and find the TP#7-1, 7-2, 7-3, and 7-4 acceptable. |
| Nokia | TP#7-1: OK  TP#7-2: OK  TP#7-3/4: OK |
| Samsung | Editor has fixed the wording related to TP#7-1 in the draft CR after RAN1#107bis, so we believe this TP is not needed anymore.  OK with TP#7-2.  TP#7-3/4, we don’t think the change is essentially needed (especially when two editors are using the same wording in different spec), but we are ok if all companies want the change. |
| Qualcomm | Fine with TP# 7-1, 7-2, 7-3, and 7-4 |
| Intel | Support TP#7-1, #7-2, #7-3, and #7-4 |
| LG Electronics | For TP#7-1, we agree with Samsung that additional correction on top of R1-2200812 is not needed.  We are fine with TP#7-2.  TP#7-3 and TP#7-4 don’t seems to be essential. |
| DOCOMO | Fine with TP#7-1, #7-2, #7-3 and #7-4. |
| Apple | Fine with TP#7-2/7-3/7-4.  On TP#7-1, we share the view from Samsung that the draft CR after RAN1 107bis meeting fixed this problem already and no need of more TP. |
| Futurewei | Fine with TP#7-1, 7-2, 7-3, 7-4. We agree that TP#7-1 may no be needed and 7-3 and 7-4 are not essential. |
| Huawei, HiSilicon | **TP#7-1: Not support.**  “operation without shared spectrum channel access in FR2-2” is already covered in 38.213 in the yellow part and “operation with shared spectrum channel access in FR2-2” is already covered in red part. No need for any update.  “For operation without shared spectrum channel access, in FR1 and FR2, and for operation with shared spectrum channel access in FR2-2”  **TP#7-2:** **We think the TP needs to be modified as follows:**  - if kHz and either of "Number of PRACH slots within a subframe" in Tables 6.3.3.2-2 to 6.3.3.2-3 or "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then , otherwise  - *{indent backwards here}*if and ~~- the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then for kHz and for kHz~~  - the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then for kHz and for kHz  - the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 2, then for kHz and for kHz.  **TP#7-3: Support.**  **TP#7-4: Support** |
| Sharp | Okay with TP#7-1, TP#7-2, TP#7-3, and TP#7-4 |
| Ericsson | TP #7-1: Not needed, since correction has already been made as pointed out by Samsung  TP #7-2: Support. Indeed, the formatting needs fixing  TP #7-3/4: These don't seem needed. The comma doesn't change the meaning. |
| Moderator | Updated TP #7-2 based on Huawei’s comments in TP#7-2A.  Based on comments so far TP#7-1 can be skipped as it has been already corrected.  Companies suggested that TP#7-3 and 7-4 are not essential changes. Alternative method to address the concern from the proponent is simply to spell out the frequency range aspect. Please comment if TP#7-3A and 7-4A help, if companies don’t see a need, we can skip the TPs. |
| CATT | All these can be taken care of by the editor |
| ZTE, Sanechips | We are fine with TP# 7-2A, actually we think it does not make any essential difference between TP# 7-2 and TP# 7-2A .  We support TP# 7-3A/4A |
| LG Electronics | TP#7-2A: Support  TP#7-3A/4A: Another way could be to change to “For operation with shared spectrum channel access in FR2-2 and for operation without shared spectrum channel access” by exchanging the order of licensed and unlicensed bands… |
| Lenovo | We support TP# 7-2A and TP#7-3A/4A also fine with LG suggested re-wording. |
| OPPO | TP#7-2A: Support  TP#7-3A/4A: OK and also fine with LG’s suggestion. |
| Samsung | We are ok with TP#7-3A/4A if all companies want it, although we don’t see an issue with current specification (no way to implement wrongly). |
| Ericsson | Support with TP#7-2a.  One minor clarification (although we don't insist on it), should there be an "or" at the end of the first subullet? |

### <Summary of 1st Round Discussion>

Updated TP#7-1A, #7-3A, #7-4A based on comments received. Moderator suggests companies to further check the TPs and provide further comments if you have concerns on them.

#### TP# 7-2B for TS38.21

|  |
| --- |
| **5.3.2 OFDM baseband signal generation for PRACH**  < Unchanged parts are omitted >  where  -  is given by the parameter "starting symbol" in Tables 6.3.3.2-2 to 6.3.3.2-4;  -  is the PRACH transmission occasion within the PRACH slot, numbered in increasing order from 0 to  within a RACH slot where  is given Tables 6.3.3.2-2 to 6.3.3.2-4 for and fixed to 1 for ;  -  is given by Tables 6.3.3.2-2 to 6.3.3.2-4;  -  is given by  - if kHz, then  - if kHz and either of "Number of PRACH slots within a subframe" in Tables 6.3.3.2-2 to 6.3.3.2-3 or "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then , otherwise  *{indent backwards here}*- if kHz and ~~- the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then for kHz and for kHz~~  - the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then for kHz and for kHz, or  - the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 2, then for kHz and for kHz.  < Unchanged parts are omitted > |

#### TP# 7-3B for TS38.211

|  |
| --- |
| 7.4.3.1 Time-frequency structure of an SS/PBCH block ============= Unchanged Text Omitted =============  - For operation with shared spectrum channel access in FR2-2 and f~~F~~or operation without shared spectrum channel access ~~and for operation with shared spectrum channel access in FR2-2~~, the 4 least significant bits of  are given by the higher-layer parameter *ssb-SubcarrierOffset* and for FR1 the most significant bit of  is given by in the PBCH payload as defined in clause 7.1.1 of [4, TS 38.212].  - For operation with shared spectrum channel access in FR1, the 4 least significant bits of are given by the higher-layer parameter *ssb-SubcarrierOffset* and the most significant bit of is given by in the PBCH payload as defined in clause 7.1.1 of [4, TS 38.212]. If , ; otherwise, , and if *ssb-SubcarrierOffset* is not provided, is derived from the frequency difference between the SS/PBCH block and Point A.  ============= Unchanged Text Omitted ===================== |

#### TP# 7-4B for TS38.213

|  |
| --- |
| 13 UE procedure for monitoring Type0-PDCCH CSS sets  ============= Unchanged Text Omitted =============  For operation with shared spectrum channel access in FR2-2 and f~~F~~or operation without shared spectrum channel access ~~and for operation with shared spectrum channel access in FR2-2~~, a UE assumes that the offset in Tables 13-1 through 13-10C is defined with respect to the SCS of the CORESET for Type0-PDCCH CSS set from the smallest RB index of the CORESET for Type0-PDCCH CSS set to the smallest RB index of the common RB overlapping with the first RB of the corresponding SS/PBCH block. The SCS of the CORESET for Type0-PDCCH CSS set is provided by *subCarrierSpacingCommon* for FR1 and FR2-1 and same as the SCS of the corresponding SS/PBCH block for FR2-2. In Tables 13-7, 13-8, and 13-10 is defined in [4, TS 38.211].  ============= Unchanged Text Omitted ===================== |

### [ACTIVE] 2nd Round Discussion

Please check TP#7-2B, 7-3B, and 7-4B and comment only if you have concerns on the TP.

For TP #7-3B and 7-4B the only change is the flip of the order of the description so that there is no confusion that without shared spectrum is not limited to FR2-2.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | Thanks Moderator for reflecting our comments. We support TP#7-2B, 7-3B, and 7-4B. |
| Ericsson | Support TP#7-2B  While we don't think TP#7-3B/4B are needed, if the majority wants them, we are flexible. |
| Nokia\_2 | We are OK with TP# 7-2B and can also accept TP #7-3B and 7-4B. |
| ZTE, Sanechips | We support TP#7-2B, 7-3B, and 7-4B. |
| OPPO | We support TP#7-2B, 7-3B, and 7-4B. |
| Samsung | Same view as Ericsson. |
| InterDigital | We are ok with TP #7-2B, 7-3B, and 7-4B. |
| Huawei, HiSilicon | We Support TP #7-2B, 7-3B, and 7-4B. |

## 2.8 Other Aspects

* From [5] OPPO:
  + Support indication of short control signalling transmission related parameters.
  + RAN4’s conclusions on fixed channelization for unlicensed band should be taken into account and revisit the following questions:
    - Whether RB set should be reconsidered to match with channelization
    - Whether CORESET should be configured within each channelization
    - Whether PUCCH and PRACH should be transmitted within channelization
    - Whether LBT bandwidth should be aligned with channelization (related to agenda item 8.2.6)
* From [9] Spreadtrum
  + Supporting initial cell selection with 480kHz SSB should be an optional UE capability separately from supporting other processing with 480/960kHz SCS.
  + The candidate SSB positions for 120kHz SCS follows the current spec.
  + The SSB-based TRS/CSI-RS validation can be supported.

### Summary of Discussions

Similar to last meeting, moderator suggest that short control signaling and LBT aspects to be discussed in channel access agenda. Also any discussion whether specific features should be optional or mandatory should be discussed in the UE feature discussion (unless it is proposal to introduce a new capability).

Companies to provide additional comments for other missing issues not covered by the moderator summary.

### [ACTIVE] 1st Round Discussion

Companies to provide additional comments for other missing issues not covered by the moderator summary.

|  |  |
| --- | --- |
| Company | Comments |
| OPPO | According to the LS from RAN4 (R4-2200081), fixed sync raster with potential fixed channelization similar as NR-U for unlicensed bands is considered, accordingly, concepts defined in NR-U may be reused, e.g.,   * RB set should be reconsidered to match with channelization * CORESET should be configured within each channelization * PUCCH and PRACH should be transmitted within channelization * LBT bandwidth should be aligned with channelization (related to agenda item 8.2.6) |
| Moderator | Continue discussion.  @OPPO: can you clarify what exactly you do wish to agree to? |
| OPPO | Since the RAN1 discussions up to now has not considered that in unlicensed band there would be channelizations like we have in NRU. Therefore, we have not discussed whether the CORESET should be restricted in a channelization or can be configured cross channelization. Similarly, in FR2-2 we did not introduce RB set due to that we believed there won’t be any kind of channelization for FR2-2. However, from RAN4 LS, on the other hand, it shows that RAN4 has decided that there is channelization for unlicensed band like NRU. Moreover, RAN4 asked RAN1 to take this decision into account for RAN1 work. For this reason, it would be reasonable to re-discuss whether the RB set should be introduced to align with the channelization. Also whether the PRACH, PUCCH, CORESET0 during the initial access can be configured across channelization. |

# List of Stable Proposals for Email Approval

#### Conclusion #3-1A

* Support default DBTW length of 5ms if discoveryBurstWindowLength is not provided in FR2-2.
* No change to specification is needed

# List of Agreements/Conclusions from RAN1 #108-e

Outcome from Tuesday Feb. 22 GTW session

**Working Assumption**

* Use 1 bit for Q in MIB
  + SubcarrierSpacingCommon field will be used to convey value of {32, 64} for operation with~~out~~ shared spectrum channel access
  + Note that this is revising the working assumption made in RAN1#107-e on “use 2 bits for Q, {SubcarrierSpacingCommon, spare bit in MIB}”

# Reference

1. R1-2200952, “Remaining issue of initial access signals and channels for 52-71GHz spectrum,” Huawei, HiSilicon
2. R1-2200987, “On the remaining issues in initial access for Beyond 52.6GHz,” FUTUREWEI
3. R1-2201032, “Remaining issues for initial access operation in 52.6-71GHz,” InterDigital, Inc.
4. R1-2201085, “Remaining issues on initial access aspects for NR operation from 52.6GHz to 71GHz,” vivo
5. R1-2201265, “Discussion on remaining issue for initial access aspects,” OPPO
6. R1-2201351, “Remaining issues on Initial access aspects for up to 71GHz operation,” CATT
7. R1-2201388, “Remaining issues on the initial access aspects for 52.6 to 71GHz,” ZTE, Sanechips
8. R1-2201470, “Remaining issues on initial access aspects for NR in FR2-2,” NTT DOCOMO, INC.
9. R1-2201541, “Discussion on initial access aspects for NR for 60GHz,” Spreadtrum Communications
10. R1-2201596, “Maintenance on initial access aspects for NR from 52.6 GHz to 71 GHz,” Panasonic Corporation
11. R1-2201662, “Initial access aspects,” Nokia, Nokia Shanghai Bell
12. R1-2201688, “Discussion on initial access aspects for extending NR up to 71 GHz,” Intel Corporation
13. R1-2201734, “Initial Access Aspects,” Ericsson
14. R1-2201764, “On remaining issues for initial access,” Apple
15. R1-2201901, “Remaining issues on initial access aspects supporting NR from 52.6 to 71 GHz,” NEC
16. R1-2202004, “Maintenance on initial access aspects for NR from 52.6 GHz to 71 GHz,” Samsung
17. R1-2202129, “Initial access aspects for NR in 52.6 to 71GHz band,” Qualcomm Incorporated
18. R1-2202189, “Initial access aspects,” Sharp
19. R1-2202335, “Initial access aspects to support NR above 52.6 GHz,” LG Electronics

# List of RAN1 Agreements on initial access

## RAN1 #104-e

**R1-2102073** [Draft] LS on beam switching gap for 60 GHz band Intel Corporation

Final LS endorsed in R1-2102202

Agreement:

Send an LS to RAN4 to get input on gap required for gNBs and UEs for beam switching and for UL/DL and DL/UL switching.

Agreement:

Whether or not to support 240 kHz, 480kHz and 960kHz SCS for SSB and the conditions under which SSB for 240 kHz, 480 kHz and 960 kHz may be supported will be decided no later than RAN1#104bis-e.

Agreement:

For an unlicensed band that requires LBT, further study whether/how to support discovery burst (DB) and discovery burst transmission window (DBTW) at least for 120 kHz SSB SCS

* If DB supported
  + FFS: What signals/channels are included in DB other than SS/PBCH block
* If DBTW is supported
  + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs
    - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.
  + PBCH payload size is no greater than that for FR2
  + Duration of DBTW is no greater than 5 ms
  + Number of PBCH DMRS sequences is the same as for FR2
* The following points are additionally FFS:
  + How to indicate candidate SSB indices and QCL relation without exceeding limit on PBCH payload size
  + Details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands
  + Whether or not to support DBTW for SSB SCS(s) other than 120 kHz if other SSB SCS(s) are supported

Agreement:

For CORESET#0 and Type0-PDCCH search space configured in MIB:

* Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {120, 120} kHz
  + Support at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 for {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS = {120, 120} kHz.
    - FFS: Supporting additional values
  + FFS: Supported values for SSB to CORESET#0 offset RBs
* If 480kHz SSB SCS that configures CORESET#0 and Type0-PDCCH CSS in MIB is agreed to be supported,
  + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {480, 480} kHz
* If 960 kHz SSB SCS that configures CORESET#0 and Type0-PDCCH CSS in MIB is agreed to be supported,
  + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {960, 960} kHz
* If 240 kHz SSB SCS is agreed to be supported,
  + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {240, 120} kHz
* FFS: any other combinations between one of SSB SCS (120, 240, 480, 960) and one of CORESET#0 SCS (120, 480, 960)
  + FFS: initial timing resolution based on low SCS (120 kHz) and its impact on the performance of higher SCS (480/960 kHz)

Agreement:

For 480 kHz and 960 kHz SSB SCS (if agreed)

* Study further on reserving symbol gap between SSB positions with different SSB index (and possibly between SSB position and other signal/channels)
  + FFS: whether symbol gap is needed for only 960 kHz or both 480 and 960 kHz.
* Study further on reserving gap for UL/DL switching within the pattern accounting possibility for reserving UL transmission occasions in the SSB pattern
* Study should account for inputs from RAN4

Agreement:

* For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2.
* For non-initial access use cases,
  + if 480kHz and/or 960 kHz SSB SCS is agreed to be supported, support 480 and/or 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.
    - FFS: support of sequence length L = 571, 1151
* FFS: Support of 480 and/or 960 kHz PRACH SCS for initial access use cases, if 480 and/or 960 kHz SSB SCS is agreed to be supported for initial access

Agreement:

If 480 and/or 960 kHz PRACH SCS is supported, RAN1 should study whether or not the current RA-RNTI calculation and PRACH identification in RAR correctly provides unique identification of PRACH.

## RAN1 #104-bis-e

Agreement:

For the case where SSB location and SCS are explicitly provided to the UE (non-initial access) and SSB does not configure Type-0 PDCCH, support 480 kHz and 960 kHz numerologies for the SSB

* Note: Strive to minimize specification impact due to the new SCS for SSB

Agreement:

* For operation with shared spectrum channel access of NR 52.6 – 71 GHz, support discovery burst (DB) and define the DB same as in Rel-16 37.213 Section 4.0
* FFS: Support discovery burst transmission window (DBTW) at least for SSB with 120 kHz SCS with the following requirements
  + PBCH payload size is no greater than that for FR2
  + Duration of DBTW is no greater than 5 ms
  + Number of PBCH DMRS sequences is the same as for FR2
  + FFS: applicability of DBTW design for 120kHz to SSB with 480kHz and 960kHz SCS
  + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs
    - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.
    - FFS: details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands
    - FFS: details of how to inform UEs of the configuration of DBTW

Agreement:

For SSB with 120kHz SCS for NR 52.6 GHz to 71 GHz,

* 120 kHz SCS: the first symbols of the candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n, where index 0 corresponds to the first symbol of the first slot in a half-frame.
* For carrier frequencies within 52.6 GHz to 71GHz, support at least 𝑛 = 0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18.
  + Other values of *n* (if any) are FFS, and support of additional n values are subject to support of DBTW for 120kHz SSB

Agreement:

* PRACH configuration for 480/960 kHz SCS (if agreed)
  + The minimum PRACH configuration period is 10 ms (as in FR2)
  + For RO configuration for PRACH with 480/960kHz SCS,
    - FFS: details of how to configure the 480/960 kHz PRACH ROs using [60 or 120 kHz] reference slot considering at least:
      * location of 480/960 kHz PRACH slot per reference slot
      * location of duration containing 480/960khz PRACH slot pattern within 10ms
      * potential impact to RA-RNTI calculation

## RAN1 #105-e

Agreement:

For 480kHz/960kHz SSB, select one of the following alternatives:

* ALT 1) First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
  + value of X and Y are identical for 480kHz and 960kHz
    - FFS: exact value of X and Y
* ALT 2) First symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
* Values of n for 480kHz and 960kHz for ALT 1 and 2
  + FFS: whether number of values for ‘n’ depend on LBT operation (i.e. LBT vs no-LBT)
  + FFS: exact values of ‘n’ for each SCS
  + Values of ‘n’ for one mode of operation shall be strictly a subset of values for another mode of operation, if two mode of operation exist for number of candidate SSBs
  + FFS: whether values of ‘n’ shall not be all consecutive integer values (i.e. non-candidate SSB slots are positioned every few candidate SSB slots)

Proposal:

In addition to 120kHz, support **480** kHz SSB for initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with following constraints.

* Limited sync raster entry numbers
  + It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than 665 (Note: the total number of synchronization raster entries in FR2 for band n259 + n261 is 602). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.
* only 480kHz CORESTE#0/Type0-PDCCH SCS supported for 480 kHz SSB SCS.
* SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical
* Prioritize support SSB-CORESET0 multiplexing pattern 1. Other patterns discussed on a best effort basis.
* Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible

Formal objection sustained by: Huawei, MediaTek (would like to discuss at next meeting)

Proposal:

In addition to 120kHz, support **both** **480 and 960** kHz SSB for initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with following constraints.

* Limited sync raster entry numbers
  + It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than 665 (Note: the total number of synchronization raster entries in FR2 for band n259 + n261 is 602). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.
* only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS i.e., (480,480) and (960,960).
* SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical
* Prioritize support SSB-CORESET0 multiplexing pattern 1. Other patterns discussed on a best effort basis.
* Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible

Formal objection sustained by: Huawei, MediaTek (object to 960 kHz)

Proposal:

To support ANR and PCI confusion detection for 480/960kHz SCS based SSB, support CORESET#0/Type0-PDCCH configuration in MIB of 480 and 960kHz SSB

* FFS: additional method(s) to enable support to obtain neighbor cell PCI and SIB1 contents related to CGI reporting
* Only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS, i.e., (480,480) and (960,960).
* Prioritize support SSB-CORESET0 multiplexing pattern 1. Other patterns discussed on a best effort basis.
* Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible
* Note: From UE perspective, ANR detection for 480/960kHz SCS based SSB is not supported if the UE does not support 480/960 SCS for SSB.
* Note: for ANR, when reading the MIB, the cell containing the SSB is known to the UE, as defined in 38.133 specification.

Formal objection sustained by: Huawei

Agreement:

For the case agreed in RAN1 #104bis-e where 480/960 kHz SSB location and SCS are explicitly provided to the UE (non-initial access)

* Support configuring CORESET#0/Type0-PDCCH for the purpose of ANR/PCI confusion detection by down selecting from the following two alternatives
  + Alt 1) Using dedicated signaling
  + Alt 2) Using configuration in MIB
    - Note: for ANR, when reading the MIB, the cell containing the SSB is known to the UE, as defined in 38.133 specification.

Agreement:

For 480kHz and 960kHz PRACH,

* Down-select among option 1 and 2
  + Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
    - FFS: supported values of the starting PRACH slot index within reference slot and whether or not the ROs for a given PRACH configuration can span more than one PRACH slot if gaps between consecutive ROs are supported for LBT and/or beam switching purposes
  + Option 2) Each 120kHz RO corresponds to 4 and 8 candidate RO positions for 480kHz and 960kHz PRACH, respectively. Information about the number and locations of 480/960kHz candidate RO(s) are configured or pre-selected within each 120kHz RO. The reference 120kHz RO is determined by the current PRACH configuration method in Rel-15/16 specification.
* Following alternatives are considered on PRACH density
  + ALT 1) At least the same density (i.e. number of PRACH slots per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: support for higher PRACH slot density (number of PRACH slots per reference slot)
  + ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: support for higher RO density
  + An “example” illustration of PRACH slots for 480/960kHz is shown below:



* FFS: whether and how to account for LBT in RO configuration (if needed)
* FFS: whether and how to account for beam switching gap in RO configuration (if needed)

Agreement:

FFS: Support DBTW at least for 120kHz

* FFS whether DBTW will be applicable for 480/960 kHz SSB SCS
  + If DBTW is supported for 480/960kHz SSB:
    - For the case agreed in RAN1 #104bis-e where 480/960 kHz SSB location and SCS are explicitly provided to the UE (non-initial access), indication of DBTW configuration (e.g. enable/disable of DBTW,  , and DBTW length) are supported by dedicated signaling.
* For 120kHz SSB, support mechanism to distinguish at least the following scenarios:
  + Case 1) (Unlicensed with LBT off) + DBTW disabled
  + Case 2) (Unlicensed with LBT on) + DBTW enabled
  + Case 3) (Unlicensed with LBT on) + DBTW disabled
  + Case 4) (Licensed) + DBTW disabled
  + FFS: Whether/how LBT on/off is indicated in MIB
    - If not indicated in MIB, then FFS whether/how the UE determines different sizes of DCI 1\_0 with CRC scrambled by SI-RNTI
  + FFS: whether any case(s) can be combined for DBTW signaling design and how to handle implications to DCI 1\_0 size ambiguity if is not distinguished in signaling
  + FFS: whether all above cases need an explicit indication
  + FFS: Whether a single indication can be used for combination of more than one cases
* For 120 kHz SSB, enable/disable of DBTW is indicated by one or more of the following methods:
  + Option 1) signaling in MIB
    - Option 1-1) disabling DBTW is jointly coded with
    - Option 1-2) indicated by other bit fields in MIB
    - FFS: among options 1-1 and 1-2
  + Option 2) distinct GSCN used by the SSB
  + Option 3) By comparing the value of  in MIB and DBTW length after UE reads SIB1 or by comparing the value of  in MIB and default DBTW length of 5 ms before UE reads SIB1.
  + FFS: whether to support option 1, 2, 3, or any combination of the options.
  + Note: enable/disable signaling of DBTW by MIB or GSCN does not preclude other signaling methods

Agreement:

If DBTW is supported,

* Working assumption: MIB signaling to support
  + Alt A) indication of at least for 120kHz SSB
    - In this case, the total number of values of to not exceed 4
  + Alt B) Explicit indication of SSB index and/or SSB candidate location
    - FFS on the details of signaling
  + FFS betweenAlt A, or B, or supporting both
* Supported DBTW lengths
  + Alt 1) 0.5, 1, 2, 3, 4, 5 msec
    - Note: same as Rel-16 FR1 NR-U
  + Alt 2) maximum 5 msec
    - FFS other values
  + FFS between Alt 1 and 2
* Number of candidate positions when DBTW is enabled
  + For 120kHz SSB
    - FFS between 64 or 80
  + If DBTW is additionally supported for 480/960kHz SSB
    - FFS between 64 or 128

## RAN1 #106-e

Conclusion:

RAN1 will continue discussions to develop solutions for supporting DBTW

Agreement:

* For 480 and 960kHz PRACH:
  + The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.



Agreement:

* For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, X} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.



* Alt 1: X = 8
* Alt 2: X = 9

Agreement:

For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.

Working assumption:

For 120kHz SSB, the number of candidates SSBs in a half frame is 64.

Agreement:

For DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec

* Note: this should be the same as Rel-16 NR-U DBTW lengths.

Agreement:

For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,

* Support the following set of parameters.

|  |  |  |
| --- | --- | --- |
| SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols |
| 1 | 24 | 2 |
| 1 | 48 | 1 |
| 1 | 48 | 2 |

* + Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design.
* FFS: addition other set of parameters

Agreement:

Do not support PRACH length L=571, 1151 for 960kHz PRACH and at least L =1151 for 480kHz PRACH.

Agreement:

For 480 and 960kHz PRACH:

* At least the same RO density in time domain (i.e. number of specified RO per reference slot according the PRACH configuration index) as for 120kHz PRACH in FR2 is supported
  + FFS: Support gap between consecutive ROs in time domain and the details to derive the gap

Agreement:

For 480 and 960kHz PRACH,

* When a PRACH slot can contain all time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,
  + and when number of PRACH slots in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + and when the number of PRACH slots in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* FFS: values, when a PRACH slot cannot contain all time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching.
* FFS: whether to allow for additional values if the maximum that can be configured for the number of FD RO’s is less than 8 (due to BW limitation)

## RAN1 #106-bis-e

Working assumption:

Support DBTW for 120 kHz.

* FFS: Support for 480 kHz and 960 kHz

Conclusion:

Do not support gap between consecutive ROs for 480kHz and 960kHz

Agreement:

Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).

* Existing DCI size alignment in TS38.212 applies to DCI 1\_0 and 0\_0 in CSS.

Agreement:

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB or PBCH payload.
  + FFS: Whether or not to indicate licensed regime by different synchronization raster entries.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB or PBCH payload.

Agreement:

No other values of n other than agreed previously is supported for 120kHz SCS, where parameter ‘n’ is the set of values to determine the first symbols of the candidate SSB blocks for 120kHz SCS in agreement from RAN1 #104-bis-e.

Working assumption:

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations
* Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design

Agreement:

Additionally, support PRACH length L=571 for 480kHz

Agreement:

Support 120 kHz and 480 kHz subcarrier spacing for initial UL BWP for PCell.

Working assumption:

For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW

* If only 1 bit is needed: subCarrierSpacingCommon
* If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 (pending CORESET0 or search space design would allows for this bit), else, use the spare-bit (not the Msg Extension bit)
  + The design of CORESET0 and search space shall be done without any consideration to this proposal
  + If 2 bits are needed for both 120kHz and 480/960kHz cases, then use the same bit field combination (i.e. use pdcch-ConfigSIB1 bit for 120/480/960 kHz or spare-bit for 120/480.960 kHz)
  + Note: If pdcch-ConfigSIB1 bit is used, the use of controlResourceSetZero (searchSpaceZero) for 120 kHz and   searchSpaceZero (controlResourceSetZero) for 480/960 kHz is not precluded
* FFS: if 3 bits are required
* Note: the working assumption can be confirmed after RAN1 agrees on the number of needed SSB-CORESET0 offsets based on RAN4 channelization design

Agreement:

For 120kHz SCS, for  values:

* If 2 bits are available in MIB for , at least support {16, 32, 64}
* If 1 bit is available in MIB for , support {32, 64}
  + FFS: methods to indicate more  values without increasing used number of bits, e.g., {16, 32, 64}
* Note: value  < 64 indicates DBTW enabled/supported and operation with shared spectrum.
* Note: For operation without shared spectrum channel access, a UE expects to be configured with  = 64. Use of =64 in shared spectrum is not precluded.
* FFS: 1 bit or 2 bits used for 

Agreement:

Supported value of n for 480/960kHz SSB slot pattern:

* ALT A) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
  + same pattern will apply to 480kHz and 960kHz (i.e same N and M for 480 and 960 kHz)
  + N = 2, M = 8
  + FFS: starting position of n
* ALT B) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
  + scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz)
  + N = 2, M = 8
  + FFS: starting position of n
* ALT C) slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.
  + Note: ALT 4 means that only slots 32-39 for 480 kHz SSB pattern are reserved for UL and 960 kHz SSB pattern is contiguous.

Agreement:

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:

* FFS: The value of X (> 0)
* FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
* FFS: whether or not to use same or different X value for 480 and 960 kHz
* FFS: whether Y = , or Y=, or whether to remove entries with Y

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Index** |  | **Number of search space sets per slot** |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | X | 1 | 1 | 0 |
| 3 | X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 7 | X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 9 | 5 + X | 1 | 1 | 0 |
| 10 | 5 + X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 11 | 5 + X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

## RAN1 #107-e

**Agreement**

* Support DBTW with 480 and 960 kHz SCS.
* For licensed and unlicensed operation, support 64 candidate SSB positions in a half frame
* Working assumption: Use 2 bits for Q:
  + SubcarrierSpacingCommon
  + spare bit in MIB
* Send LS to RAN2 for confirming the use of the spare bit in MIB
  + The use of 2 bits for Q can be revisited if RAN2 tells RAN1 that the spare bit cannot be used

R1-2112614 [Draft] LS on initial access for 60 GHz Intel Corporation

Final LS endorsed in R1-2112805.

**Agreement**

Confirm the following working assumptions:

* (From #106-bis-e) Support DBTW for 120 kHz.
* (From #106-e) For 120kHz SSB, the number of candidates SSBs in a half frame is 64.

**Agreement**

For SCS that support DBTW, UE derives the QCL relation between candidate SSBs by the value of , where is the candidate SSB index.

**Conclusion**

* The bit-width of ssb-PositionsInBurst in SIB1 and ServingCellConfigCommon is kept the same as in Rel-15 (i.e., 16-bits in SIB1 and 64-bits in ServingCellConfigCommon).

**Agreement**

If multiplexing pattern 3 for 480 and 960 kHz is supported, the TDRA allocation table C is updated as follows:

* Row index 6 (previously reserved) is set to
  + Dmrs-TypeA-Position: 2,3
  + PDSCH mapping type: Type B
  + K0 : 0
  + S = 11
  + L = 2

**Agreement**

Finalizing PRACH slot index for 480 and 960 kHz (removal of bracket of previous agreement)

* when number of PRACH slots in a reference slot is 1,
  + for 480kHz and for 960kHz PRACH
* when the number of PRACH slots in a reference slot is 2,
  + for 480kHz and for 960kHz PRACH

**Agreement**

Update the Table 8.1-2 in TS38.213 to indicate the Ngap (gap between valid RO and SS/PBCH) for 480 kHz and 960 kHz SCS as follows:

* for 480 kHz
* for 960 kHz;

**Agreement**

For single cell operation or for operation with carrier aggregation in a same frequency band, a UE does not transmit PRACH and PUSCH/PUCCH/SRS in a same slot or when a gap between the first or last symbol of a PRACH transmission in a first slot is separated by less than 𝑁 symbols from the last or first symbol, respectively, of a PUSCH/PUCCH/SRS transmission in a second slot where 𝑁=16 for 𝜇=5, 𝑁=32 for 𝜇=6, and 𝜇 is the SCS configuration for the active UL BWP. For a PUSCH transmission with repetition Type B, this applies to each actual repetition for PUSCH transmission [6, TS 38.214].

**Conclusion:**

as part of gap between last symbol of PDCCH order reception and first symbol of the PRACH transmission for FR2-2 uses the same value as FR2-1 (i.e. single value for FR2).

**Agreement**

* For 480 kHz, slot index, n, that contain SSB are:
  + n = {0,1,2,3,4,5,6,7, 8,9,10,11,12,13,14,15, 16,17,18,19,20,21,22,23, 24,25,26,27,28,29,30,31}
* For 960 kHz, slot index, n, that contain SSB are:
  + n = {0,1,2,3,4,5,6,7, 8,9,10,11,12,13,14,15, 16,17,18,19,20,21,22,23, 24,25,26,27,28,29,30,31}

**Agreement**

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz,

* use Table 13-12 in TS38.213 for multiplexing pattern 1,
* use Table 13-15 in TS38.213 for multiplexing pattern 3.

**Agreement**

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, parameter X from previous RAN1 agreement is set to:

* X = 1.25 for 480 kHz
* X = 0.625 for 960 kHz

**Conclusion:**

For FR2-2, support the same mechanism as in Rel-16 for extended RAR window for both 4-step and 2-step RACH.

**Agreement**

For a Type-2 random access procedure, a UE transmits a PUSCH, when applicable, after transmitting a PRACH. The UE encodes a transport block provided for the PUSCH transmission using redundancy version number 0. The PUSCH transmission is after the PRACH transmission by at least symbols where for and for , and is the SCS configuration for the active UL BWP.

**Agreement**

For 480 and 960 kHz, supported DBTW lengths are:

* {1.25, 1, 0.75, 0.5, 0.25, 0.125, X} ms, where X = 0.0625 if Q=8 is supported and X is removed if Q=8 is not supported.

**Agreement**

SSB-PositionQCL-Relation IE to indicate QCL relationship between SSB positions for FR2-2 are same set of values supported for in MIB.

**Agreement**

For operation with shared spectrum access, for SS/PBCH block and CORESET#0 multiplexing pattern 3, a UE monitors PDCCH in the Type0-PDCCH CSS set over slots that include Type0-PDCCH monitoring occasions associated with SS/PBCH blocks that are quasi co-located with the SS/PBCH block that provides a CORESET for Type0-PDCCH CSS set.

**Agreement**

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, parameter Y from previous RAN1 agreement is Y = .

**Agreement**

* For 480kHz and 960kHz PRACH, reuse the RA-RNTI and MSGB-RNTI formula as FR2 and express the slot indexes t\_id based on 120kHz SCS:
  + RA-RNTI =1+s\_id+14×t\_id+14×80×f\_id +14×80×8×ul\_carrier\_id
  + MSGB-RNTI = 1 + s\_id + 14 × t\_id + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id + 14 × 80 × 8 × 2
    - where the subcarrier spacing to determine t\_id is based on the value of µ specified in clause 5.3.2 in TS 38.211 [8] for µ = {0, 1, 2, 3}
    - for µ = {5, 6}, t\_id is the index of the 120 kHz slot in a system frame that contains the PRACH occasion (0 ≤ t\_id < 80).
  + Note: As per previous RAN1 agreement, there is only one 480 or 960 kHz PRACH slot in a 120kHz slot, such that RA-RNTI and MSGB-RNTI does not result in ID collision.
* Send LS to RAN2 on the updates on RA-RNTI and MSGB-RNTI.

R1-2112734 [Draft] LS on RA-RNTI and MSGB-RNTI for 480 and 960 kHz Intel Corporation

Final LS endorsed in R1-2112832 (with removal of “first” in text referring to the captured agreement)

**Agreement**

* Same values using the same set of signaling bits are supported for 120, 480, and 960 kHz.
* Supported values of : {16, 32, 64}
  + Note:
    - For operation with shared spectrum channel access, any supported value of can be indicated and value < 64 indicates DBTW enabled
    - UE is expected to be configured with =64 in licensed operations
    - For operation with and without shared spectrum channel access, =64 indicates that the SS/PBCH block index and the candidate SS/PBCH block index have a one-to-one mapping relationship.

**Working assumption**

For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,

* After supporting entries for multiplexing pattern 1 for the agreed pairs of (, ) ={(24, 2), (48, 1), (48,2)} (with required RB offsets), if additional entries are left, support multiplex pattern 3 with 24 PRB and 2 symbol duration, and multiplexing pattern 3 with 48 PRB and 2 symbol duration.

**Working assumption**

For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,

* After supporting entries for multiplexing pattern 1 for the agreed pairs of (, ) ={(24, 2), (48, 1), (48,2)} (with required RB offsets) and multiplex pattern 3 with 24 and 48 PRB and 2 symbol duration (with required RB offsets), if additional entries are left, support multiplexing pattern 1 with 96 PRB and 2 symbol duration
  + Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design.

**Agreement**

* If is indicated, the same interpretation of ssb-PositionsInBurst in SIB1 or ServingCellConfigCommon as in Rel-16 is supported, i.e.:
  + A bit set to 1 at position indicates SS/PBCH block index k-1
  + The UE assumes that a bit at position k > is set to 0
    - For ssb-PositionsInBurst in SIB1, the UE assumes that a bit at *groupPresence* corresponding to a SS/PBCH block index ≥ is set to 0
  + Note: for ssb-PositionsInBurst in SIB1, position k corresponds to the SS/PBCH block index indicated by a bit in inOneGroup and a bit in groupPresence
* In operation with shared spectrum in 60 GHz, for ssb-PositionsInBurst in ServingCellConfigCommonSIB,
  + for MSB k, k≥1, of inOneGroup and MSB m, m≥1, of groupPresense of ssb-PositionsInBurst:
    - if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to ‘SSB index’ equal to k-1+(m-1)×8 may be transmitted;
    - if MSB k of inOneGroup or MSB m of groupPresense is set to 0, the UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to ‘SSB index’ equal to k-1+(m-1)×8 is not transmitted;
* In operation with shared spectrum in 60 GHz, for ssb-PositionsInBurst in ServingCellConfigCommon,
  + ssb-PositionsInBurst bits correspond to supported ‘SSB indices’,
    - and UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to indicated bit(s) may be transmitted;
    - and UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to not indicated bit(s) are not transmitted
* Note to spec editor: The above three bullets maintain the same behavior as Rel-16 NR-U

**Agreement**

Update the Table 6.3.3.2-1 in TS 38.211 as follows:

* Table 6.3.3.2-1: Supported combinations of and , and the corresponding value of .

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | for PRACH | for PUSCH | , allocation expressed in number of RBs for PUSCH |  |
| ... | ... | ... | ... | ... |
| 139 | 120 | 120 | 12 | 2 |
| 139 | 120 | 480 | 3 | 1 |
| 139 | 120 | 960 | 2 | 23 |
| 139 | 480 | 120 | 48 | 2 |
| 139 | 480 | 480 | 12 | 2 |
| 139 | 480 | 960 | 6 | 2 |
| 139 | 960 | 120 | 96 | 2 |
| 139 | 960 | 480 | 24 | 2 |
| 139 | 960 | 960 | 12 | 2 |
| 571 | 120 | 120 | 48 | 2 |
| 571 | 120 | 480 | 12 | 1 |
| 571 | 120 | 960 | 7 | 47 |
| 571 | 480 | 120 | 192 | 2 |
| 571 | 480 | 480 | 48 | 2 |
| 571 | 480 | 960 | 24 | 2 |
| 1151 | 120 | 120 | 97 | 6 |
| 1151 | 120 | 480 | 25 | 23 |
| 1151 | 120 | 960 | 13 | 45 |

## RAN1 #107-bis-e

**Conclusion:**

RRC parameters list to capture changes identified below:

* Add the following note to the comment section of discoveryBurstWindowLength-r17 row in RRC parameter list
  + “Note: This parameter is to be included in both SIB1 and the common serving cell configuration parameters”.
* Support adding “SSB-PositionQCL-Relation-r17” to RRC parameter list as both UE-specific and cell-specific parameter.
* Inform RAN2 (by adding notes to RRC parameter list) that the either the value range of the information element SSB-PositionQCL-Relation-r16 needs to be extended, or a new Rel-17 IE need to be defined to allow configuration of Q = 16, 32, or 64 in SIB2, SIB3, SIB4, MeasObjectNR, and ServingCellConfigCommon for RRM measurements when operating with shared spectrum channel access in FR2-2.

The TP below for TS38.213v17.0.0 is endorsed as a working assumption

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| =========== Unchanged Text Omitted ===========  Table 13-15A: PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 3 and {SS/PBCH block, PDCCH} SCS {480, 480} kHz or {960, 960} kHz   |  |  |  | | --- | --- | --- | | Index | PDCCH monitoring occasions (SFN and slot number) | First symbol index  ( = 0, 1, …, 31) | | 0 |  | 2, 9 in  , |   ============ Unchanged Text Omitted ============ |

The TP below for TS38.211v17.0.0 is endorsed

|  |
| --- |
| \*\*\* Unchanged text omitted \*\*\*  5.3.2 OFDM baseband signal generation for PRACH  The time-continuous signal  on antenna port for PRACH is defined by  \*\*\* Unchanged text omitted \*\*\* |

The TP below for TS38.214v17.0.0 is endorsed

|  |
| --- |
| \*\*\* Unchanged text omitted \*\*\*  7       UE procedures for transmitting and receiving on a carrier with intra-cell guard bands  For operation with shared spectrum channel access in FR1, when the UE is configured with any of *IntraCellGuardBandsPerSCS* for UL carrier and for DL carrier with SCS configuration , the UE is provided with intra-cell guard bands on a carrier with , each defined by start CRB and size in number of CRBs, and, provided by higher layer parameters *startCRB* and *nrofCRBs*, respectively, where. The subscript *x* is set to DL and UL for the downlink and uplink, respectively. Where there is no risk of confusion, the subscript *x* can be dropped. The intra-cell guard bands separateRB sets, each defined by start and end CRB,and, respectively. The UE does not expect that *nrofCRBs* is configured with non-zero value smaller than the applicable intra-cell guard bands as specified in [8, TS 38.101-1] corresponding to and carrier size. The UE determines the start and end CRB indices for as  \*\*\* Unchanged text omitted \*\*\* |

**R1-2200689** Summary #1 of email discussion on initial access aspect of NR extension up to 71 GHz Moderator (Intel Corporation)

TP# 8-1a for TS38.213 in section 3 of R1-2200689 is endorsed.

**Conclusion**

RRC parameters list to capture changes identified below

* New parameter, ra-ResponseWindow-r17, under sub-feature group SSB and RACH
  + Value range {sl240, sl320, sl640, sl960, sl1280, sl1920, sl2560}
  + Based on previous conclusion:
    - For FR2-2, support the same mechanism as in Rel-16 for extended RAR window for both 4-step and 2-step RACH.
* New parameter, msgB-ResponseWindow-r17, under sub-feature group SSB and RACH
  + Value range { sl240, sl640, sl960, sl1280, sl1920, sl2560}
  + Based on previous conclusion:
    - For FR2-2, support the same mechanism as in Rel-16 for extended RAR window for both 4-step and 2-step RACH.
* Existing parameter, msgA-PRACH-RootSequenceIndex-r16, under sub-feature group SSB and RACH
  + Description:
    - May not need to change the IE, but need to add in the note on the limitation to be used with SCS. Field description requires updating to capture that L = 1151 is not supported for SCS 480 and 960 kHz and L = 571 is not supported for 960 kHz.
  + Value range:
    - CHOICE { l571 INTEGER {0..569}, l1151 INTEGER {0..1149}}
  + Cell-specific