**3GPP TSG RAN WG1 Meeting #106-bis-e R1-2110405**

**e-Meeting, October 11 – 19, 2021**

**Source: Moderator (Intel Corporation)**

**Title: Issue Summary for initial access aspects of NR extension up to 71 GHz**

**Agenda item: 8.2.1**

**Document for: Discussion**

# Introduction

In this contribution, we discuss aspects related to initial access for extending NR up to 71 GHz based on submitted contributions to RAN1 #106-bis-e. The main issues discussed in the following section for initial access are detailed design for synchronization signal block (SSB), CORESET#0, PRACH related issues, and discovery reference signal (DRS) related operations.

During the last RAN Plenary, the WID has been updated to reflect the approved numerologies for initial access. The following is copy of the WID objectives relevant for initial access.

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| * Physical layer aspects including [RAN1]:   + Support of up to 64 SSB beams for licensed and unlicensed operation in this frequency range.   + Supports 120kHz SCS for SSB and 120kHz SCS for initial access related signals/channels in an initial BWP.     - Study and specify, if needed, additional SCS (480kHz, 960kHz) for SSB for cases other than initial access.     - Note: coverage enhancement for SSB is not pursued.   + In addition to 120kHz, support 480 kHz SSB for initial access with support of CORESET#0/Type0-PDCCH configuration in the MIB with following constraints:     - Limited sync raster entry numbers       * It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than 665 (Note: the total number of synchronization raster entries in FR2 for band n259 + n257 is 599). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.     - only 480kHz CORESET#0/Type0-PDCCH SCS supported for 480 kHz SSB SCS.     - Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis.     - 960 kHz numerology for the SSB is not supported by the UE for initial access in Rel-17.     - Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible     - Note: 480 kHz is an optional SSB numerology for initial access for the UE. A UE supporting a band in 52.6-71 GHz must at least support 120 kHz SCS (for initial access and after initial access)     - Note: Dependency or lack thereof for a UE supporting 480kHz and/or 960kHz numerology for data and control to also support 480kHz SSB numerology for initial access is to be tackled as part of UE capability discussion.   + Support ANR and PCI confusion detection for 120, 480 and 960kHz SCS based SSB, support CORESET#0/Type0-PDCCH configuration in MIB of 120, 480 and 960kHz SSB     - FFS: additional method(s) to enable support to obtain neighbour cell SIB1 contents related to CGI reporting     - Only 1 CORESET#0/Type0-PDCCH SCS supported for each SSB SCS, i.e., (120, 120), (480, 480) and (960, 960).     - Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis.     - Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible     - Note: From UE perspective, ANR detection for 480/960kHz SCS based SSB is not supported if the UE does not support 480/960 SCS for SSB.     - Note: for ANR, when reading the MIB, the cell containing the SSB is known to the UE, as defined in 38.133 specification.   + Specify support for PRACH sequence lengths (i.e. L=139, L=571 and L=1151) and study, if needed, specify support for RO configuration for non-consecutive RACH occasions (RO) in time domain for operation in shared spectrum |

# Summary of issues

## 2.1 SSB Aspects

### 2.1.1 DRS Related Aspects (and other MIB design other than CORESET#0/Type0-PDCCH)

* From [1] Huawei/HiSilicon:
  + For SSB with 120 kHz SCS, confirm the working assumption on 64 candidate SSBs within a half frame.
  + For SSB with 480 kHz and 960 kHz SCS, 64 candidate SSBs is sufficient for operation without shared spectrum while 128 candidate SSBs should be supported for operation with shared spectrum.
  + For operation with shared spectrum and for 480 kHz and 960 kHz SSBs, indicate the 7th bit of the candidate SSB index by borrowing the 4th LSB of SFN in the PBCH payload. Indicate the 4th LSB of SFN with spare bit in MIB payload.
  + Support discovery burst transmission window (DBTW) for all three numerologies in shared spectrum in 52.6GHz to 71GHz. At least should be indicated in MIB for all three numerologies.
  + Configure DBTW length in SIB1 for operation with shared spectrum in 52.6GHz to 71GHz with the following values:
    - 480 kHz SCS: {72, 32, 24, 16, 8, 4} slots = {2.25, 1, 0.75, 0.5, 0.25, 0.125} ms
    - 960 kHz SCS: {64, 32, 24, 16, 8, 4} slots = {1, 0.5, 0.375, 0.25, 0.125, 0.0625} ms
  + No indication for licensed or unlicensed operation is required in MIB.
  + Use of LBT should be indicated in SIB1 to help UE determine the existence of “ChannelAccess-CPext” field in DCI format 1-0/0-0. Common DCI size should be assumed for DCI format 1-0/0-0 in CSS no matter LBT is ON or OFF.
  + In operation with shared spectrum in 60 GHz, for MSB k, k≥1, of inOneGroup and MSB m, m≥1, of groupPresense of ssb-PositionsInBurst:
    - if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with candidate SSB index(es) corresponding to SSB index equal to k-1+(m-1)×8 may be transmitted;
    - if MSB k of inOneGroup or MSB m of groupPresense are set to 0, the UE assumes that the SSB(s) are not transmitted.
  + Regardless of the value of the MSB k of inOneGroup and MSB m of groupPresense in ssb-PositionsInBurst configured in SIB1, if > , UE assumes that candidate SSB index(es) corresponding to SSB index equal to are not transmitted.
  + the MIB content and PBCH payload in Table [1]-6 and Table [1]-7should be supported for 120 kHz, 480 kHz and 960 kHz SSB.
    - Table [1]-6 MIB and PBCH payload bit allocation for 120kHz SCS SSB

|  |  |  |  |
| --- | --- | --- | --- |
| bit | | FR2-1 | FR2-2 |
|  |  | 120kHz | 120kHz |
| MIB | 0 | 10 - 5 MSB of SFN | 10 - 5 MSB of SFN |
| 1 |
| 2 |
| 3 |
| 4 |
| 5 |
| 6 | subCarrierSpacingCommon | 1 bit for (sec 2.2) |
| 7 | ssb-SubcarrierOffset | ssb-SubcarrierOffset |
| 8 |
| 9 |
| 10 |
| 11 | dmrs-TypeA-Position | dmrs-TypeA-Position |
| 12 | pdcch-ConfigSIB1  /controlResourceSetZero | controlResourceSetZero  (Sec 3.1 Table 1) |
| 13 |
| 14 |
| 15 |
| 16 | pdcch-ConfigSIB1  /searchSpaceZero | searchSpaceZero  (Sec 3.3 Table 4) |
| 17 |
| 18 |
| 19 | 1 bit for (sec 2.2) |
| 20 | cellBarred | cellBarred |
| 21 | intraFreqReselection | intraFreqReselection |
| 22 | spare | Spare bit |
| PBCH payload | 23 | 4th LSB of SFN | 4th LSB of SFN |
| 24 | 3th LSB of SFN | 3th LSB of SFN |
| 25 | 2th LSB of SFN | 3th LSB of SFN |
| 26 | 1th LSB of SFN | 3th LSB of SFN |
| 27 | half frame indication | half frame indication |
| 28 | 6th bit of candi. SSB index | 6th bit of candi. SSB index |
| 29 | 5th bit of candi. SSB index | 5th bit of candi. SSB index |
| 30 | 4th bit of candi. SSB index | 4th bit of candi. SSB index |

* + Table [1]-7 MIB and PBCH payload bit allocation 480kHz and 960kHz SCS SSB

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| bit | | FR2-1 | FR2-2 | |
|  |  | 120kHz | 480kHz and 960kHz | |
| DBTW OFF | DBTW ON |
| MIB | 0 | 10 - 5 MSB of SFN | 10 - 5 MSB of SFN | |
| 1 |
| 2 |
| 3 |
| 4 |
| 5 |
| 6 | subCarrierSpacingCommon | 1 bit for (sec 2.2) | |
| 7 | ssb-SubcarrierOffset | ssb-SubcarrierOffset | |
| 8 |
| 9 |
| 10 |
| 11 | dmrs-TypeA-Position | dmrs-TypeA-Position | |
| 12 | pdcch-ConfigSIB1  /controlResourceSetZero | controlResourceSetZero  (sec 3.2 Table 2) | |
| 13 |
| 14 |
| 15 | searchSpaceZero  (Sec 3.3 Table 5) | |
| 16 | pdcch-ConfigSIB1  /searchSpaceZero |
| 17 |
| 18 |
| 19 | 1 bit for (sec 2.2) | |
| 20 | cellBarred | cellBarred | |
| 21 | intraFreqReselection | intraFreqReselection | |
| 22 | spare | Spare bit | 4th LSB of SFN |
| PBCH payload | 23 | 4th LSB of SFN | 4th LSB of SFN | 7th bit of candi. SSB index (sec 2.1) |
| 24 | 3th LSB of SFN | 3th LSB of SFN | |
| 25 | 2th LSB of SFN | 3th LSB of SFN | |
| 26 | 1th LSB of SFN | 3th LSB of SFN | |
| 27 | half frame indication | half frame indication | |
| 28 | 6th bit of candi. SSB index | 6th bit of candi. SSB index | |
| 29 | 5th bit of candi. SSB index | 5th bit of candi. SSB index | |
| 30 | 4th bit of candi. SSB index | 4th bit of candi. SSB index | |

* From [2] Futurewei:
  + For FR2-2 120 kHz SCS support SS/PBCH DBTW.
  + For 480/960 kHz SS/PBCH DBTW should not be supported.
  + If DBTW is supported use where is the candidate SS/PBCH block index to establish a QCL relation between different SS/PBCH indexes.
  + For 120kHz SS/PBCH SCS indicate that DBTW is enabled in SIB1 and indicate LBT disabled either in MIB or in SIB1.
  + For 480/960 kHz SS/PBCH SCS use the field subCarrierSpacingCommon to indicate LBT disabled.
  + Consider whether the ssb-PositionsInBurst definition needs to be updated to support higher SCS SSB.
* From [3] Spreadtrum:
  + Confirm the working assumption that DBTW is supported at least for 120kHz SCS.
  + DBTW is supported for 480/960kHz SCS.
  + Confirm the working assumption that the number of candidate SSBs in a half frame is 64 for 120kHz SCS.
  + The number of candidate SSBs in a half frame is more than 64 and not great than 128 for 480/960kHz SCS.
  + The maximum DBTW length for 480/960kHz SCS can be 2ms and 1ms respectively.
  + The gap slots (slots without SSB) for 480/960kHz SCS can be different from that of 120kHz SCS.
* From [4] ZTE, Sanechips:
  + The following design of candidate SSBs with SCS 480/960 kHz in a half frame can be considered: First symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
    - If DBTW is not supported or DBTW is disabled
      * For 480kHz SCS, the 64 candidate SSBs are located in 32 slots, with 2 slots spacing between every 8 consecutive slots to avoid prolonged occupation, i.e. n=0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37
      * For 960kHz SCS, the 64 candidate SSBs are located in 32 slots, with 4 slots spacing between every 16 consecutive slots to avoid prolonged occupation, i.e. n=0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35
    - If DBTW is supported and it is enabled
      * Additional 64 candidate SSB can be defined after the above original 64 candidate SSBs in the half frame
  + Discovery burst transmission window (DBTW) should be supported for all approved SSB SCS in FR2-2, including 120 kHz, 480 kHz and 960 kHz.
  + In order to reduce the impact of standardization caused by indicating candidate SSB indices, the maximum number of candidate SSBs defined in the half-frame can be kept unchanged (maintain 64) or limited to 128 for 480/960 kHz SSB SCS.
  + Four candidate values {8,16,32,64} for are preferred from the perspective of reducing bit overhead.
  + For Rel-17 above 52.6GHz, it is recommended that the UE derives the QCL relation between candidate SSBs by the value of , where is the candidate SSB index.
  + Enable/disable of DBTW can be implicitly indicated by comparing the value of  in MIB and DBTW length, and explicit signaling is not needed for this purpose.
* From [5] vivo:
  + Support DBTW in un-licensed band/LBT case from 52.6 GHz to 71 GHz for SSB with all supported SCSs.
  + Do not support explicit indication of DBTW on/off in MIB.
  + Support to use DBTW lengths {0.5, 1, 2, 3, 4, 5} msec for SCS 120 kHz, and FFS small values for SCS 480 kHz and 960 kHz.
  + Do not support LBT on/off indication in MIB.
  + The following fields could be considered to indicate the value of Q in PBCH:
    - subCarrierSpacingCommon
    - LSB of ssb-SubcarrierOffset
    - Coreset#0 and Type#0 PDCCH indication
  + When DBTW is enabled with indicated value of Q, how to interpret the meaning of ssbPositionsInBurst should be studied.
* From [8] NEC:
  + DBTW should be supported for SSB transmission with 120 kHz and 480/960 kHz SCS.
  + The long term sensing could be considered as an approach to enabling/disabling DBTW.
  + DBTW indication could be indicated per beam for SSB transmission.
  + Unlicensed/licensed operation indication should not be indicated in MIB.
  + LBT on/off indication should not be indicated in MIB.
  + The value of Q should be no lower than 16 at least.
  + The candidate SSB indication in NR-U should be reused with enhancement to indicate DBTW enabling/disabling and Q value jointly in MIB.
  + If DBTW is additionally supported for 480/960kHz SCS SSB transmission, 128 SSB candidates should be supported.
* From [9] CATT:
  + DBTW for 480/960 kHz SSB SCS can be supported with up to 128 candidate SSB index.
  + To indicate 7th bit of the candidate SSB index for 480/960 kHz SSB SCS, following schemes can be further considered and down-selected:
    - Borrowing the subCarrierSpacingCommon in MIB
    - Borrowing the 4th LSB of SFN, and move 4th LSB of SFN to subCarrierSpacingCommon in MIB
    - Borrowing half frame bit  , with all candidate SSBs are assumed to be put in first half frame when DBTW is enabling.
  + For NR operation in 60 GHz unlicensed spectrum, the discovery burst transmission window (DBTW) shall be supported for 120 KHz SSB at least when gNB configures more than 56 SSB transmissions.
  + sub-set of SSBs can be transmitted as NO-LBT and the other sub-set SSBs are transmitted as DBTW if the exempt Short Control Signaling rules can be applied by local region rule.
  + For number of ，four states {16, 32, 64, reserved/DBTW disabled} is recommend.
  + On DBTW length for SCS 480/960 KHz (if supported), scale factor is applied comparing to value of SCS 120 KHz,
  + For 120 kHz SSB, signaling in MIB can indicate enable/disable of DBTW.
  + If LBT ON/OFF state is indicated in MIB/PBCH, joint coding can be used for indication of LBT ON/OFF, DBTW enabling/disabling and one bit information for candidate SSB index.
  + If LBT ON/OFF state is not indicated in MIB/PBCH, it can be indicated in DCI 1\_0 scrambled by SI-RNTI.
* From [11] Ericsson:
  + If a DBTW is supported (not our preference), it should only be supported for 120 kHz SSB SCS and not for 480/960 kHz SSB SCS.
  + Confirm the working assumption that no additional (compared to the already supported 64) candidate SS/PBCH block positions are introduced.
  + Conclude that a DBTW is not supported.
  + If a DBTW is supported (not our preference) select one of the following options:
    - Option 1: Q and DBTW on/off indicated in MIB using the subCarrierSpacingCommon field
      * Q = [64, 32] where Q=64 indicates DBTW off
      * DCI 1\_0 size is the same for LBT on/off (unlicensed/licensed)
    - Option 2: Q and DBTW on/off indicated in SIB1
      * The subCarrierSpacingCommon field is ignored
      * Default assumption for Q depends on the agreed value range of Q and can be left to UE implementation
      * Q = [48, 32, 16, 8]. Absence of the parameter in SIB1 indicates DBTW off.
      * DCI 1\_0 size is the same for LBT on/off (unlicensed/licensed)
    - Option 3: Q indicated in SIB1 and DBTW on/off indicated in MIB using the subCarrierSpacingCommon field
      * Default assumption for Q (if DBTW on) depends on the agreed value range of Q and can be left to UE implementation
      * Q = [48, 32, 16, 8]. The parameter is only configured in SIB1 if DBTW is on
      * DCI 1\_0 size is the same for LBT on/off (unlicensed/licensed)
* From [12] Nokia, NSB:
  + The design for DBTW, if supported, is common to different sub-carrier spacings.
  + Confirm the working assumption on number of SSB candidate locations in a half frame for 120kHz:
  + For 480kHz and 960kHz, the number of SSB candidate locations in a half frame is 64.
  + If DBTW is supported,  is supported. FFS for need for other values.
  + Provide LBT on/off and DBTW indication in SIB1. (Note: licenced/unlicenced operation is assumed to be already part of SIB1 via frequency band information.)
  + Do not provide separate, additional indication for DBTW on/off in MIB. (Note it would be possible to provide the indication implicitly e.g. part of .)
* From [13] Samsung:
  + Support discovery burst transmission window for all SCSs on the 60 GHz unlicensed spectrum.
    - The indication of Q can be in MIB for a best effort, and if not possible, in SIB1;
    - The indication of DBTW disabling can be joint coded with the indication of Q, if Q is indicated in MIB; and the indication can use 1 bit in MIB, if Q is not indicated in MIB;
    - For 480 kHz and 960 kHz SCS, support 128 candidate SS/PBCH block locations within a half frame, and use one PHY bit in PBCH payload to indicate the extra candidate SS/PBCH block index (e.g. 7th LSB);
    - For initial access, different synchronization raster entries are applied for licensed and unlicensed operations; for non-initial access, support an explicit indication of licensed or licensed operation when configuring a cell.
* From [15] Intel:
  + For DRS based on SSBs with SCS 120 kHz:
    - and reuse Case D slot pattern for placement of SSB candidates
    - is indicated in MIB
      * At least the subCarrierSpacingCommon bit from MIB is reinterpreted to indicate
      * Consider 1 bit from pdcch-ConfigSIB1 in MIB to indicate from the extended set, e.g.,
        + Alternatively, the spare bit from PBCH payload could be used to indicate in addition to the subCarrierSpacingCommon bit from MIB
    - DBTW on/off is identified based on comparison of the DBTW length with the time duration occupied by transmission of SSBs
    - DBTW length is signalled in SIB1
    - Licensed vs. unlicensed operation is not signalled in MIB
      * Align sizes of DCI 1\_0 scrambled with SI-RNTI between licensed and unlicensed modes of operation
  + For DRS based on SSBs with SCS 480 kHz/960 kHz:
    - and SSB candidate slots are arranged according to Proposal 2
    - One bit from MIB is used for indexing additional SSB candidates
      * The subCarrierSpacingCommon bit from MIB is reinterpreted for this purpose
    - is indicated in MIB
      * One bit from pdcch-ConfigSIB1 in MIB is repurposed to indicate at least
    - The spare bit from PBCH payload could be used to indicate in addition to 1 bit from pdcch-ConfigSIB1 in MIB
    - DBTW length is fixed and not signalled
    - DBTW on/off is explicitly signalled in SIB1
    - Licensed vs. unlicensed operation is not signalled in MIB
      * Align sizes of DCI 1\_0 scrambled with SI-RNTI between licensed and unlicensed modes of operation
* From [16] NTT Docomo:
  + DBTW should be supported irrespective of SCS.
    - In a certain region, e.g., Japan, sensing needs to be performed for initiating any transmission by any device in 60 GHz.
  + Support to confirm the working assumption that the number of candidate SSBs with 120 kHz SCS in a half frame is 64
  + Support 64 candidate SSBs with both 480 and 960 kHz SCS
  + For DBTW to be supported in Rel-17 NR 52.6 – 71 GHz, similar to Rel-16 NR-U, support to indicate QCL parameter in MIB
    - Support to use subCarrierSpacingCommon for QCL parameter indication in MIB
  + For DBTW to be supported in Rel-17 NR 52.6 – 71 GHz, following information can be implicitly indicated via subCarrierSpacingCommon
    - Enabling/disabling of DBTW
    - Licensed/unlicensed band
    - LBT on/off
* From [17] Pansonic:
  + DBTW is supported regardless of SCS.
  + The number of candidate SSB positions is 64.
  + For values, total of 4 states are supported (e.g., {8, 16, 32, 64}).
  + For the indication of Q, SIB1 is used except the signaling method to use MIB are clarified.
  + If Q is indicated in MIB, DBTW enabled/disabled is indicated in MIB (implicitly Q=64). If Q is indicated in SIB1, DBTW enabled/disabled is indicated in SIB1.
  + DBTW lengths for 480/960 kHz SCS are scaled from 120 kHz SCS.
* From [18] Sony:
  + Discovery Burst Transmission Window should be supported for all SCSs.
  + Enabling/disabling DBTW and should be signalled in MIB
    - Indication of disabling DBTW should be jointly coded with
      * Parameter to signal indicates {8, 16, 32, or 64}
      * = 64 implies disabling DBTW
  + For indication of QCL relation and disabling DBTW in MIB, subCarrierSpacingCommon and reserved state of pdcchConfig-SIB1 should be used.
* From [19] ETRI:
  + Propose to support DBTW for all SSB SCSs and the same DBTW lengths with Rel-16 NR-U.
* From [20] Lenovo, Motorola Mobility:
  + For NR operation in unlicensed bands between 52.6 GHz and 71 GHz, potential enhancements related to periodic transmission of DRS such as SSB/PBCH/CORESET#0 are needed including:
    - performing directional LBT prior to the transmission of SSB according to the ssb-PositionsInBurst
    - directional LBT on multiple beams at the same time at the beginning of the DRS window
    - Cat 2 LBT (depending on the gap) before actual transmission
* From [21] Interdigital:
  + Support Discovery Burst (DB) and Discovery Burst Transmission Window (DBTW) in unlicensed spectrum operations that require LBT to enhance the initial access operation in beyond 52.6GHz spectrum.
  + Consider indicating enable/disable of DBTW in initial access operations based on a range of the sync raster offset.
  + Consider the enhancements to indicate the mode of operation regarding the enable/disable of the DBTW, on/off of the LBT, and the license regime based on the combination of Sync. raster offset and MIB indication.
  + Support enhancements on the reference tables in indication of Q parameter for up to 64 SSB beams in initial access operations for unlicensed spectrum in beyond 52.6GHz, e.g., subsamples of the Q parameter.
  + Support candidate SSB positions more than 64 for 120kHz SSB.
* From [22] LG Electronics:
  + For FR2-2, UE always assumes DBTW is enabled for 120 kHz SSB reception.
  + Total of 4 states (e.g., {8, 16, 32, 64}) of values are supported by using 2 bits of the followings.
    - subCarrierSpacingCommon
    - LSB(s) of ssb-SubcarrierOffset
    - dmrs-TypeA-Position
  + No MIB indication to identify operation with or without shared spectrum channel access, but SIB indication or synchronization raster differentiation to identify operation with or without shared spectrum channel access.
  + Do not indicate LBT on/off in PBCH. DCI format 1\_0 size should be aligned regardless of LBT on or off unless synchronization rasters are used to identify operation with or without shared spectrum channel access.
  + Discuss how to signal actually transmitted SSBs via ssb-PositionsInBurst when can be indicated to be less than 64 in MIB.
* From [23] Sharp:
  + Adopt DBTW for SSB with 120 or 480 or 960 kHz SCS in FR2-2 operation.
  + One MIB payload bit is used for indication of candidate SSB index for . Another MIB payload bit indicates Q related information. DBTW enabled/disabled is not explicitly indicated via MIB. These two bits are repurposed from the bit for subCarrierSpacingCommon indication and the LSB for ssb-SubcarrierOffset indication.
* From [24] Apple:
  + If DBTW is introduced, for above 52.6GHz frequency band, consider the following:
    - Re-purposing the 1-bit 'subCarrierSpacingCommon'
    - If more than one bit is needed, re-purposing 1-bit MSB of controlResourceSetZero in MIB or providing one more bit information by selecting one sequence from two candidates to scramble CRC bits of PBCH payload.
  + LBT on/off can be implicitly indicated based on the indication of DBTW enable/disable.
  + Licensed/unlicensed band can be signaled in SIB1.
  + The same DCI size is used for DCI format 1\_0 monitored in a common search space in both licensed and unlicensed band with existing padding operation.
* From [25] Convida Wireless:
  + If impact of LBT failure is not addressed, increasing the number of SSB candidate positions to above 64 to increase transmission opportunities to cope with LBT failure could be considered.
  + Increased number of candidate SSB positions for unlicensed/shared spectrum channel access with LBT could be considered for SCSs of 480KHz and 960KHz for 52.6 GHz-71 GHz.
* From [26] Qualcomm:
  + do not support discovery burst transmission window (DBTW) for SSB for SCS 480 and 960 kHz
  + for an unlicensed band that requires LBT, if DBTW for SSB is adopted for 120 kHz SSB:
    - MIB signaling to support indication of for 120 kHz SSB
    - Minimize the number of bits needed to signal (1 or 2 bits) and thus the values (2 or 4 values)
    - Enabling/disabling DBTW can be implicit in the value
    - Consider getting the bits needed from one or more of the following: controlResourceSetZero, subCarrierSpacingCommon
    - Confirm the working assumption that the number of candidate positions when DBTW is enabled = 64 for 120 kHz SSB
    - Consider having a subset of the SSBs (< 64) transmitted under the short control signal assumption while another subset can be best effort or have multiple positions per beam (have a within the subset)
  + consider increasing the size of the DCI 1\_0 for NR licensed, by adding a field, to align with the size of the corresponding DCIs for the unlicensed operation.
* From [27] WILUS:
  + We propose to support discovery burst transmission window (DBTW) for at least 120kHz SCS which makes it possible to define candidate SSB positions within the DBTW. In addition to 120kHz SCS, DBTW should be applicable for 480/960 kHz SSB SCS on supporting NR above 52.6GHz.
  + Before confirming the working assumption that the number of candidates SSBs in a half frame is 64 for 120kHz SSB, it would be necessary to consider a method for compensating for the insufficient opportunity of the SSB transmission due to LBT failures in order to perform the operation in the unlicensed band of above 52.6GHz.
  + It should be further considered that the additional candidate SS/PBCH block locations within a DBTW can be set to the closest slot locations after LBT failure at candidate SS/PBCH blocks locations as defined in FR2.

#### Summary of Discussions

The following are previous agreements on DRS aspects.

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| **RAN1 #105e**  **Agreement:**  For an unlicensed band that requires LBT, further study whether/how to support discovery burst (DB) and discovery burst transmission window (DBTW) at least for 120 kHz SSB SCS   * If DB supported   + FFS: What signals/channels are included in DB other than SS/PBCH block * If DBTW is supported   + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs     - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.   + PBCH payload size is no greater than that for FR2   + Duration of DBTW is no greater than 5 ms   + Number of PBCH DMRS sequences is the same as for FR2 * The following points are additionally FFS:   + How to indicate candidate SSB indices and QCL relation without exceeding limit on PBCH payload size   + Details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands * Whether or not to support DBTW for SSB SCS(s) other than 120 kHz if other SSB SCS(s) are supported   **Agreement:**   * For operation with shared spectrum channel access of NR 52.6 – 71 GHz, support discovery burst (DB) and define the DB same as in Rel-16 37.213 Section 4.0 * FFS: Support discovery burst transmission window (DBTW) at least for SSB with 120 kHz SCS with the following requirements   + PBCH payload size is no greater than that for FR2   + Duration of DBTW is no greater than 5 ms   + Number of PBCH DMRS sequences is the same as for FR2   + FFS: applicability of DBTW design for 120kHz to SSB with 480kHz and 960kHz SCS   + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs     - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.     - FFS: details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands     - FFS: details of how to inform UEs of the configuration of DBTW   **Agreement:**  FFS: Support DBTW at least for 120kHz   * FFS whether DBTW will be applicable for 480/960 kHz SSB SCS   + If DBTW is supported for 480/960kHz SSB:     - For the case agreed in RAN1 #104bis-e where 480/960 kHz SSB location and SCS are explicitly provided to the UE (non-initial access), indication of DBTW configuration (e.g. enable/disable of DBTW,  , and DBTW length) are supported by dedicated signaling.  * For 120kHz SSB, support mechanism to distinguish at least the following scenarios:   + Case 1) (Unlicensed with LBT off) + DBTW disabled   + Case 2) (Unlicensed with LBT on) + DBTW enabled   + Case 3) (Unlicensed with LBT on) + DBTW disabled   + Case 4) (Licensed) + DBTW disabled   + FFS: Whether/how LBT on/off is indicated in MIB     - If not indicated in MIB, then FFS whether/how the UE determines different sizes of DCI 1\_0 with CRC scrambled by SI-RNTI   + FFS: whether any case(s) can be combined for DBTW signaling design and how to handle implications to DCI 1\_0 size ambiguity if is not distinguished in signaling   + FFS: whether all above cases need an explicit indication   + FFS: Whether a single indication can be used for combination of more than one cases * For 120 kHz SSB, enable/disable of DBTW is indicated by one or more of the following methods:   + Option 1) signaling in MIB     - Option 1-1) disabling DBTW is jointly coded with  * + - Option 1-2) indicated by other bit fields in MIB     - FFS: among options 1-1 and 1-2   + Option 2) distinct GSCN used by the SSB   + Option 3) By comparing the value of  in MIB and DBTW length after UE reads SIB1 or by comparing the value of  in MIB and default DBTW length of 5 ms before UE reads SIB1.  * + FFS: whether to support option 1, 2, 3, or any combination of the options.   + Note: enable/disable signaling of DBTW by MIB or GSCN does not preclude other signaling methods   **Agreement:**  If DBTW is supported,   * Working assumption: MIB signaling to support   + Alt A) indication of at least for 120kHz SSB  * + - In this case, the total number of values of to not exceed 4  * + Alt B) Explicit indication of SSB index and/or SSB candidate location     - FFS on the details of signaling   + FFS betweenAlt A, or B, or supporting both * Supported DBTW lengths   + Alt 1) 0.5, 1, 2, 3, 4, 5 msec     - Note: same as Rel-16 FR1 NR-U   + Alt 2) maximum 5 msec     - FFS other values   + FFS between Alt 1 and 2 * Number of candidate positions when DBTW is enabled   + For 120kHz SSB     - FFS between 64 or 80   + If DBTW is additionally supported for 480/960kHz SSB     - FFS between 64 or 128   **RAN1 #106e**  Conclusion:  RAN1 will continue discussions to develop solutions for supporting DBTW  **Agreement:**  For DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec   * Note: this should be the same as Rel-16 NR-U DBTW lengths.   Working assumption:  For 120kHz SSB, the number of candidates SSBs in a half frame is 64. |

The following is a summary of company position of various aspects of DRS.

* Supporting DBTW
  + Support: Huawei/HiSilicon, Futurewei (120kHz only), ZTE/Sanechips, vivo, NEC, Intel, Docomo, Panasonic, Sony, ETRI, Interdigital, Sharp, WILUS, LGE
  + Do not support: Ericsson (if supported only for 120kHz only), Qualcomm (not support for 480/960kHz)
* Indication of DBTW (for initial access)
  + in MIB (either explicit or implicit with Q=64):
    - implicit: ZTE/Sanechip, NEC, Samsung (if Q is indicated in MIB), Docomo, Panasonic, Sony, Sharp, Apple, Qualcomm (for 120kHz), Huawei/HiSilicon (for 120 kHz), Nokia/NSB (if number of candidate locations is restricted for 480/960kHz scs to 64)
    - no explicit signaling in MIB: vivo
    - explicit: CATT, Samsung (if Q is not indicated in MIB), Huawei/HiSilicon (for 480/960 kHz)
  + in SIB1:
    - Futurewei, Nokia/NSB
  + raster:
    - Interdigital, Samsung
  + UE always assumes DBTW is enabled for 120 kHz SSB reception, w/o indication of DBTW
    - LGE
* Supporting means of conveying candidate SSB location & SSB beams
  + Supported values:
    - 120kHz {16,32,64} : Huawei/HiSilicon
    - 480/960kHz {16,32,64} : Huawei/HiSilicon
    - {8,16,32,64}: ZTE/Sanechips, Intel (if 2 bit for Q), Panasonic, Sony, LGE
    - Min 16: NEC
    - {16, 32, 64, reserved/DBTW disabled}: CATT
    - {32, 64} 64 serves DBTW disable: Ericsson (if DBTW supported, if Q indicated in MIB, as one option)
    - {8,16,32,48} : Ericsson (if DBTW supported, if Q indicated in SIB1, as one option)
    - {32, 64}: Nokia/NSB
    - {16,64}: Intel (if 1 bit for Q)
  + Potential bits for required signaling (e.g. additional SSB index, Q) for supporting DBTW in MIB
    - subCarrierSpacingCommon: Huawei/HiSilicon, vivo, Ericsson (if DBTW supported, as one option), Intel, Docomo, Sony, LGE, Apple, Qualcomm (for 120kHz), Futurewei (for 120 kHz only)
    - controlResourceSetZero: vivo, Intel (for 480/960kHz), Sony, Apple, Qualcomm (for 120kHz), Huawei/HiSilicon (for 480/960 kHz)
    - searchSpaceZero: Huawei/HiSilicon (for 120 kHz only), vivo
    - some bits of k\_SSB: vivo, LGE
    - dmrs-typeA-position: LGE
    - spare bit (not the Msg Extension bit): Intel
    - LSB of *ssb-SubcarrierOffset* Futurewei (120 kHz only)
  + Placement of candidate SSB index in PHY portion of PBCH (not in MIB) (requires moving 1 bit of SFN from PHY portion of PBCH to MIB.
    - Support: Huawei/HiSilicon, Samsung
    - FFS: CATT
  + indication in SIB1
    - Ericsson (if DBTW supported, as one option)
* Supported DBTW lengths for 480/960 kHz (if supported)
  + For 480kHz:
    - {2.25, 1, 0.75, 0.5, 0.25, 0.125} ms : Huawei/HiSilicon
    - Max 2 ms: Spreadtrum
    - Scaled version of 120kHz case: CATT, Panasonic
    - Fixed to single value: Intel
    - Same as for 120kHz i.e. {0.5, 1, 2, 3, 4, 5} ms: Nokia
  + For 960kHz:
    - {1, 0.5, 0.375, 0.25, 0.125, 0.0625} ms : Huawei/HiSilicon
    - Max 1ms: Spreadtrum
    - Scaled version of 120kHz case: CATT, Panasonic
    - Fixed to single value: Intel
    - Same as for 120kHz i.e. {0.5, 1, 2, 3, 4, 5} ms: Nokia
* Number of SSB candidates for DBTW
  + For 120kHz:
    - confirm WA
      * Huawei/HiSilicon, Spreadtrum, Ericsson, Nokia/NSB, Intel, Docomo, Qualcomm, ETRI, LGE, Sharp
    - Wait for confirming WA after decision for 480/960kHz is made:
      * CATT
    - Support additional values of n
      * NEC
  + For 480/960kHz:
    - 64: Huawei/HiSilicon (licensed), ZTE (if DBTW not supported/disabled), Docomo, Panasonic, LGE (if supported), Nokia (if supported)
    - 64 < 128 ≤ 128: Spreadtrum
    - < 64: Interdigital,
    - 128: Huawei/HiSilicon (unlicensed), ZTE (if DBTW supported/enabled), NEC, CATT, Samsung, Intel, Convida, Sharp
* *ssb-PositionsInBurst* in SIB1
  + if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with candidate SSB index(es) corresponding to SSB index equal to k-1+(m-1)×8 may be transmitted; if MSB k of inOneGroup or MSB m of groupPresense are set to 0, the UE assumes that the SSB(s) are not transmitted.
    - Huawei/HiSilicon
  + FFS: Futurewei, vivo, LGE
* Indication of licensed and unlicensed operation in MIB:
  + Support: [Docomo]
  + Not support: Huawei/HiSilicon, NEC, Intel, LGE, Apple, Sharp
* Indication of LBT
  + MIB: Futurewei (480/960kHz), [Docomo], Apple (implicit with DBTW)
  + SIB1: Nokia/NSB, Intel, [LGE], Sharp
  + If indicated, joint encoding with DBTW enable/disable: CATT
  + If not indicated, provide indication in DCI 1\_0 scrambled by SI-RNTI: CATT
* DCI sizes between licensed and unlicensed
  + Same size for CSS DCI 1\_0/0\_0: Huawei/HiSilicon, Ericsson, Intel, LGE (unless licensed and unlicensed operation modes are differentiated by sync raster), Apple, Qualcomm, Sharp

#### <Moderator’s Suggestion for Discussions>

Discuss further on the following proposals and issues. The proposals listed are not unanimously supported by all companies. However, more numbers of companies seem to support the proposal. Therefore, moderator suggests using the proposal as basis for further discussions (even if they may not be agreeable).

**Issue #1) Whether or not to support DBTW and number of SSB candidates**

##### Proposal 1.1-1 – resolved in GTW

* Support DBTW for 120kHz, 480kHz, and 960kHz cases

##### Proposal 1.1-2

* If DBTW is supported for 480 and 960 kHz, support 128 candidate SSB positions

**Issue #2) Potential bits for required signaling for supporting DBTW in MIB**

Discuss and identify which bits are available for required signaling for supporting DBTW in MIB

* subCarrierSpacingCommon
  + Seems to be unanimous support from all companies
* controlResourceSetZero
* searchSpaceZero
* some bits of k\_SSB
* dmrs-typeA-position
* spare bit (not the Msg Extension bit)

**Issue #3) Indication of DBTW &**

##### Proposal 1.1-4

* If DBTW is supported, for values:
  + If 2 bits are available in MIB for , at least support {16, 32, 64}
  + If 1 bit is available in MIB for , support {32, 64}

**Issue #4) DCI size**

##### Proposal 1.1-5

* Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).
* Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)
  + Bits will be padded, if needed, to the format with smaller DCI size between the channel access modes to match the DCI size between them.
  + Existing DCI size alignment in TS38.213 applies to DCI 1\_0 and 0\_0 in CSS.
  + FFS: DCI in USS

**Issue #5) DBTW lengths**

##### Proposal 1.1-6

* If DBTW is supported, the following DBTW length are supported for 480 and 960 kHz:
  + {2.25, 1, 0.75, 0.5, 0.25, 0.125} msec for 480 kHz.
  + {1, 0.5, 0.375, 0.25, 0.125, 0.0625} msec for 960 kHz

**Issue #6) Indication of licensed/unlicensed and LBT/no LBT in MIB**

##### Proposal 1.1-7

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB content payload.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB content payload.
  + If explicit indication of DBTW disabled is supported, use of no-LBT may be inferred from DBTW disabled indication.

**Issue #7) ssb-PositionsInBurst in SIB1**

##### Proposal 1.1-3

* If DBTW is supported, support implicit indication DBTW may be disabled with = 64 configuration.

##### Proposal 1.1-8

* For ssb-PositionsInBurst in SIB1,
  + if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with candidate SSB index(es) corresponding to SSB index equal to k-1+(m-1)×8 may be transmitted;
  + if MSB k of inOneGroup or MSB m of groupPresense are set to 0, the UE assumes that the SSB(s) are not transmitted.

#### Outcome of 10/12 Tuesday GTW Session

**Working Assumption**

* Support DBTW for 120kHz
  + FFS: support for 480kHz and 960kHz

#### 1st Round of Discussions

Please provide further comments on the above issues #1 ~ #7 and proposals listed. Also, if there are any other issues that require discussion, please comment them here.

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| Company | Comments |
| NTT DOCOMO | As for issue #1,   * On whether to support DBTW, while we support to confirm this and support DBTW for 480/960kHz as well, it would be ok to revisit this issue after clarifying the exact functionality of DBTW in 52.6-71GHz a bit more. * On # of candidate SSB positions, our best preference is to keep it as 64 as in FR2-1 for both 480/960kHz SCS, and to confirm WA for 120kHz SCS, since we would like to avoid a significant impact in physical layer specification to support 128 candidate SSB positions, which we think exceeds the benefit of 128 candidates. Furthermore, 128 candidate SSB positions are not possible for 120kHz SCS due to 5ms limitation. We prefer to have a unified design among 120, 480 and 960kHz SCS. On the other hand, if we need to consider 128 candidate SSB positions to support DMTW for larger SCSs, we would like to consider some other options to achieve the indication of SSB index more than 64 with minimized specification efforts, for example:   + Borrow the half frame bit in PBCH payload     - In this case, SSB burst has to be transmitted only in the first half frame or only in the last half frame   + Borrow LSB of SFN in MIB     - In this case, the frame where SSB burst is transmitted has to be limited in a certain frame   The alternatives above need to limit the exact occasions of SSB burst transmissions, while may require smaller amount of specification effort than the ones proposed already.  As for issue #2, we prefer to reuse subCarrierSpacingCommon for Q value indication in MIB.  As for issue #3, this highly depends on issue#1. We should defer the discussion.  As for issue #4, we support the Proposal 1.1-5.  As for issue #5, we do not think it is essential. Thus we propose to deprioritize the discussion.  As for issue #6, we support the Proposal 1.1-7.  As for issue #7, we think it should be discussed after determining # of candidate SSB positions. |
| OPPO | Proposal 1.1-2: support.  Proposal 1.1-3: we can accept this proposal only when 1 bit for is assumed, otherwise we think DBTW and should be configured independently, e.g., DBTW may be disabled with = 32 configuration if support {16, 32, 64}.  Proposal 1.1-4: support.  Proposal 1.1-5: not support. We think LBT on/off can be indicated in SIB, so there is no need to align the DCI sizes of LBT on/off for DCI 0\_0. We propose the following modification: *Proposal 1.1-5*  * *Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).* * *~~Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)~~*   + *Bits will be padded, if needed, to the format with smaller DCI size between the channel access modes to match the DCI size between them.*   + *Existing DCI size alignment in TS38.213 applies to DCI 1\_0 and 0\_0 in CSS.*   + *FFS: DCI in USS*   Proposal 1.1-6: support.  Proposal 1.1-7: support.  Proposal 1.1-8: support. |
| Qualcomm | Issue #1 (Proposal 1.1-2): we do not support this proposal. If 480/960 kHz are agreed for DBTW, we prefer to have a common design (in terms of signaling) with SCS 120 kHz, i.e. use 64 candidate SSB, since we do not see a need to differentiate 480/960 kHz.  Issue #2:   * subCarrierSpacingCommon: yes, this is already freed since SCS of SSB = SCS of CORESET0 * controlResourceSetZero: This depends on the outcome of the CORESET0 design. We can restrict it to be only 3-bits (8 possible values) to spare one bit for Q. In the current specs, only 3 bits are used for 120 kHz SCS SSB for the valid combinations for this WI. However, this may not become available if more combinations are supported (e.g., 96 RBs).   Issue #3:   * Proposal 1.1-3: We are fine with this proposal * Proposal 1.1-4: We are fine with this proposal   Issue #4 (Proposal 1.1-5): We are fine with this proposal  Issue #5 (Proposal 1.1-6): May be good to defer this until the SSB pattern and the number of SSB candidate positions are agreed  Issue #6 (Proposal 1.1-7): We are fine with this proposal  Issue #7 (Proposal 1.1-8): We prefer to defer this until other SSB/DBTW details are agreed |
| Lenovo, Motorola Mobility | Issue #1 We do not support having 128 SSB candidates for 480/960 kHz. We agree with DOCOMO that we should avoid a significant impact in physical layer specification to support 128 candidate SSB positions and prefer a common signalling design for 120 kHz, 480 kHz, and 960 kHz.  Issue #2 subCarrierSpacingCommon bits can be used for signalling  Issue #3 We are fine with the proposal  Issue #4 support the proposal  Issue #5 This depends on the number of SSB candidates and their positions, so we can deprioritize it until that has been agreed.  Issue #6 support the proposal |
| Samsung | Proposal 1.1-2: We support the proposal. Increasing the number of candidate SSB locations to allow more transmission opportunities is the most essential feature for DBTW, and that’s not possible for 120 kHz simply due to the limited number of slots in a half frame, but such restriction is not applicable for 480 and 960 kHz. We also want to note that for Rel-16 NR-U, the number of candidate SSB locations for 15 kHz and 30 kHz are different, and SCS-specific design was supported at that time, so we didn’t see any technical issue to support more than 64 candidate SSB locations for 480 and 960 kHz only.  Proposal 1.1-3: Whether this proposal works or not depend on whether we support more than 64 candidate locations. Also, we don’t prefer an implicit method for indicating DBTW is off, since for licensed band UE, the UE needs to assume to support the feature of DBTW, and then determines Q=64 to imply DBTW is off, then why not explicitly configure the DBTW is off?  Proposal 1.1-4: We believe this is related to Proposal 1.1-3, and should be resolved together after knowing the number of candidate SSB locations.  Proposal 1.1-5: We are ok with the proposal.  Proposal 1.1-6: This is also related to the number of candidate SSB locations.  Proposal 1.1-7: We don’t have strong concern on this proposal, but it would be good to be combined with the decision on DBTW on/off indication. If a UE cannot decide whether DBTW is on/off from MIB, we cannot accept this proposal.  Proposal 1.1-8: This should be part of the RRC parameter discussion, and we believe there are obvious typos in the proposal to be resolved for clarity. |
| Interdigital | **Proposal 1.1-1**: Support DBTW for 120kHz, 480kHz, and 960kHz cases  **Proposal 1.1-2**: For the number of candidate SSB indexes, in shared spectrum if the number of candidate SSB positions is equal to maximum number of beams, i.e. 64, then the DBTW cannot function as it is supposed to. The whole support for DBTW is to enable SSB retransmissions in candidate SSB positions due to LBT failure. So, we support the candidate SSB positions to be more than 64, that is:   * For 120kHz, support at least 80 candidate SSB positions * For 480 and 960 kHz, support 128 candidate SSB positions  **Proposal 1.1-3**: We do not support implicit indication of DBTW enable/disable as it might cause ambiguity given that UE might not know the license regime.**Proposal 1.1-4**: We support the proposed values.**Proposal 1.1-5:** We support the proposal.**Proposal 1.1-6**: We support the proposal. **Proposal 1.1-7**: We do not support the proposal. We propose to indicate the license regime based on sync raster offset. |
| LG Electronics | Proposal 1.1-2: We do not support this proposal. As indicated in GTW session, we prefer a common design of DBTW for all SCSs. Thus, 64 candidate SSB positions are supported for all SCSs in FR2-2.  Issue #2: In addition to subCarrierSpacingCommon, we can consider some bits of k\_SSB (but RAN4 should be involved to confirm whether those can be re-purposed) or dmrs-typeA-position.  Proposal 1.1-3: We do not support this proposal. Particularly for 120 kHz, considering WA to support 64 candidate SSB positions, UE behavior with Q=64 assuming DBTW is disabled is exactly same as UE behavior with Q=64 assuming DBTW is enabled. Therefore, it is not necessary to let UE know whether DBTW is enabled or disabled. Instead, UE can always assume that DBTW is enabled at least for 120 kHz SSB reception.  Proposal 1.1-4: Support  Proposal 1.1-5: We think if channel access mode can be informed to UE prior to SIB reception (e.g., by using sync raster), assuming different DCI size based on channel access mode is possible. In that sense, we suggest the modification as follows (in addition, editorial in the spec reference): Proposal 1.1-5 If channel access mode (i.e., LBT on/off) is not informed to UE before SIB reception,   * Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off). * Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)   + Bits will be padded, if needed, to the format with smaller DCI size between the channel access modes to match the DCI size between them.   + Existing DCI size alignment in TS38.212 applies to DCI 1\_0 and 0\_0 in CSS.   + FFS: DCI in USS   Proposal 1.1-6: We can accept this proposal but can be deferred similar to other companies’ views.  Proposal 1.1-7: We prefer not to explicitly/implicitly indicate licensed/unlicensed operation and LBT on/off MIB. In this sense, we suggest the following: Proposal 1.1-7  * Indication of licensed and unlicensed operation is not indicated in MIB content payload. * Indication of use of LBT or no-LBT is not indicated in MIB content payload.   Proposal 1.1-8: It seems premature to try to converge a specific scheme for ssb-PositionsInBurst indication in SIB1. Maybe it could be a starting point to keep the size of ssb-PositionsInBurst field same as in legacy SIB1 signaling. |
| Ericsson | Issue #1  For 120 kHz, the details of the full solution must be known before the working assumption can be confirmed, e.g., how DBTW and Q are signaled.  **We do not support Proposal 1.1-2**. If 480 and 960 kHz are to be supported, then it must be a common solution for all 3 subcarrier spacings based on 64 candidate positions. We do not wish to re-open the discussion on how to signal more than 64 candidate SSB positions – the issues are no different than for 120 kHz, and the potential solutions discussed in prior meetings are all unattractive and involve changes to implementation of the MIB/PBCH processing. One solution required low level changes to the PBCH scrambling procedures. Another solution violated the Rel-15 principle that the MIB should be constant over 80 ms.  Issue #2  **In our view, the discussion should be limited to subCarrierSpacingCommon and the spare bit**. We don't agree to repurposing of controlResourceSetZero since it is not yet known if more than 8 entries in the CORESET0 configuration table are needed, i.e., there is a RAN4 dependence on channelization design. searchSpaceZero is not feasible since there are fewer than 8 reserved value, so no bit is available. We don't agree to repurposing of k\_SSB as there is a RAN4 dependence on channelization design. Furthermore, unlike Rel-16, it is unlikely that the design would result in only even or odd values of k\_SSB being needed, so no bit is available.  Issue #3  **Proposal 1.1-3 and 1.1-4 need to be merged together and discussed as a package**. We can agree to the meged proposal, **conditioned on using one or both of the ssbSubCarrierSpacingCommon and spare bits**. This is the most efficient way forward considering the RAN4 dependence discussed in Issue #2.  Issue #4  We support Proposal 1.1.5, except that we think that **the 2nd bullet may not be needed**.  In our understanding, in the Rel-16 definition of DCI 0\_0 in 38.212, padding bits are added to equalize the size of DCI 0\_0 for licensed/unlicensed. For unlicensed, 2 fewer padding bits are added.  Issue #5  **We do not support Proposal 1.1-6 (yet)**. The values of n for the SSB time domain pattern (Section 2.1.2) need to be agreed first.  Issue #6  We support the 1st two bullets of Proposal 1.1-7, but **we do not support the 3rd bullet**. Just because the DBTW is disabled, it doesn't mean that LBT is not used for other signals/channels, e.g, if the short control signaling provision is used for SSB.  Issue #7  This is a 2nd level issue, and should be deferred until DBTW design is stable. |
| ETRI | For Issue #1, we prefer common design for DBTW regardless of SCS, however also open to increase the number of candidate SSB positions if the specification impact is limited.  For Issue #2, ‘subCarrierSpacingCommon’ can be considered as the first priority, and then other bit(s) can be considered depending on the output of other issues (e.g., CORESET#0 design, sync raster, and so on)  For Issue #3, we support both Proposal 1.1-3 and Proposal 1.1-4.  For Issue #4, we support Proposal 1.1-5.  For Issue #5, we prefer to defer this issue until the details on SSB and DBTW are agreed.  For Issue #6, we support Proposal 1.1-7.  For Issue #7, we prefer to defer this issue until the details on SSB and DBTW are agreed. |
| Sharp | Issue #1  We support Proposal 1.1-2. It is reasonable to support DBTW also for 480kHz and 960kHz cases, if the principle is to have consistent design/function among SCSs. Consequently, 128 candidate SSB positions should be supported to enable effective DBTW and Q functions.  Issue #2  It becomes clear that 1 bit of *subCarrierSpacingCommon* could be repurposed. Whether 1 bit from *controlResourceSetZero* depends on the final design of CORESET#0.  Since some of the following issues depend on the outcome of Issue #1 and Issue #2, it seems better to firstly resolve Issue #1 and Issue #2.  Issue #3  We share the same view to discuss this issue after determinations on the number of candidate SSB positions and available MIB bits.  Issue #4  We are fine with Proposal 1.1-5.  Issue #5  Discuss this issue after determinations on the number of candidate SSB positions.  Issue #6  We support Proposal 1.1-7.  Issue #7  Discuss this issue after determinations on the number of candidate SSB positions. |
| Intel | Issue#1)  **Proposal 1.1-2:** Support.  We think it’s important to support DBTW for 480 kHz/960 kHz and the number of SSB candidates as 128 for these SCS values as part of DBTW operation.  Differently from SCS 120 kHz, the operation with SCS 480 kHz/960 kHz will rely heavily on highly directional beamforming to compensate the coverage shrinkage happened with the increase of SCS. Eventually, this will require a larger number of beams including those ones carrying SSBs. Therefore, a typical operation scenario for SCS 480 kHz/960 kHz is to utilize about 64 beams for SS burst transmission which is the current maximum. However, limiting the number of SSB candidates to 64 effectively means operation without DBTW in the typical usage scenario of SCS 480 kHz/960 kHz (which is with the large number of beams). At the same time, regulations of some countries require LBT operation for unlicensed spectrum from 52.6 GHz up to 71 GHz and do not define anything similar to short control signalling exemption. One example is Japan (please see or tdoc and the reference therein for details).  From those ones don’t supporting DBTW for SCS 480 kHz/960 kHz or other ones supporting only up to 64 SSB candidates, we would like to understand how to address the situation when LBT operation is mandatory and there are no short control signalling exemption rules defined.  Issue #2)  Among the bits/fields in MIB we believe the following can be repurposed in 60 GHz.  subCarrierSpacingCommon, spare bit  also if RAN4 supports fixed channel raster definitions, we believe it will be possible to take 1 bit from controlResourceSetZero, and 1bit from LSB of k\_ssb, while supporting mux pattern 1 and 3 with 24, 48 and 96 PRBs.  Issue #3)  **Proposal 1.1-3:** Fine with the proposal assuming it is for SCS 120 kHz. In the proposal’s text the clarification is needed that this is for SCS 120 kHz.  **Proposal 1.1-4:** Fine with the proposal assuming it is for SCS 120 kHz. In the proposal’s text the clarification is needed that this is for SCS 120 kHz.  Issue #4)  **Proposal 1.1-5:** Support.  Issue#5)  **Proposal 1.1-6:** Do not support.  Our preference is a single value for DBTW length (may be different for 480 kHz and for 960 kHz) that need not to be signalled. This potentially allows to reduce the amount of signalling.  Issue #6)  **Proposal 1.1-7:** Support.  Issue#7)  **Proposal 1.1-8:** Fine with the proposal assuming it is for SCS 120 kHz. In the proposal’s text the clarification is needed that this is for SCS 120 kHz. |
| vivo | 1.1-2: Support. And the potential bits can be selected from the following indication:   * subCarrierSpacingCommon * controlResourceSetZero * searchSpaceZero   1.1-3: There is no need to discuss this specific proposal. If the number of candidate SSBs is still 64 for 480K and 960K SCS, UE follows the defined behavior with Q. When Q=64, the behavior is the same as that DBTW is off and there is no need to agree this proposal again. If the number of candidate SSBs is 128 for 480K and 960K SCH, I don’t think Q=64 could imply DBTW is off. In our view, there is no need to know whether DBTW on/off in MIB. In this case, the only benefit is less PDCCH monitoring when receiving SIB.  1.1-4: Support.  1.1-5: It is better to discuss the DCI size issue after the decision of whether support the LBT on/off indication before SIB reception.  1.1-6: The design of DBTW length is highly depend on the SSB candidate number and the SSB resource pattern design. Thus it is better to postpone this discussion.  1.1-7: Support.  1.1-8: Fine to discuss this when DBTW details are agreed. |
| Huawei, HiSilicon | **Proposal 1.1-1:** Support   * We believe that DBTW is required for 480/960 kHz as short control signaling exemption cannot be used in all regions.   **Proposal 1.1-2:** Support   * 128 candidate SSB position facilitates enabling DBTW when 64 SSB indexes are used. 64 SSB for higher numerologies seems to be a more practical use case than smaller values.   **Issue #2)**   * Support using 2 bits for indicating (which may include explicit DBTW ON/OFF indication for 480/960 kHz). 2 bits are obtained from:   + *subCarrierSpacingCommon* (1 bit) for 120/480/960 kHz.   + *searchSpaceZero* (1 bit) for 120 kHz and *controlResourceSetZero* (1 bit) for 480/960 kHz   + Note 1:     - We suggest one searchSpaceZero Table for 120 kHz and one searchSpaceZero Table for 480/960 kHz. As discussed in R1-2108767, not all entries of searchspaceZero Table 13-12 for FR2-1 are required to be supported for 120 kHz in FR2-2 as, unlike FR2-1 that supports {CORESET#0, SSB}= {120, 240} kHz, FR2-2 only supports the same numerology for SSB and CORESET#0. This renders O values 2.5 and 7.5 useless for 120 kHz searchspaceZero Table for FR2-2. Therefore, 1 bit from searchSpaceZero Table for 120 kHz in FR2-2 can be saved.     - Also, based on WID which prioritizes Mux Pattern 1 for new numerologies, we do not see the need to support Mux Pattern 3 for 480/960 kHz. This facilitates saving 1 bit from controlResourceSetZero for 480/960 kHz.   + Note 2: Based on the input from some other companies, we recognize that there may be other reasonable ways to save a bit from searchSpaceZero and/or controlResourceSetZero. We are open to discuss these alternatives as well. * Support using 1 spare bit of MIB to indicate the 4th LSB of SFN when 128 candidate SSB is used in 480/960 kHz. Instead, use the 4th LSB of SFN in PBCH payload to indicate the 7th candidate SSB index.   + Note: Note that this does not violate the 80 ms MIB periodicity in Rel15/16.   **Proposal 1.1-3:** Suggest modification  We can support the proposal if this is limited to 120 kHz. Note that “implicit indication DBTW may be disabled with = 64” seems to be at odds with Proposal 1.1-2 which propose to support 128 candidate SSBs for 480/960 kHz. To our understanding, agreeing to Proposal 1.1-3 “as is” implies that max 64 candidate SSBs for 480/960 kHz are agreed. We suggest the following change  Proposal 1.1-3 (update)  For 120 kHz, if DBTW is supported, support implicit indication DBTW may be disabled with = 64 configuration  **Proposal 1.1-4:** Support  **Proposal 1.1-5:** Suggest modification  The first sub-bullet is at odds with the second sub-bullet. In Rel-15/16, the DCI 0\_0 in CSS is padded or truncated to match the size of DCI 1\_0 in CSS as mentioned in the following lines from 38.212:   |  | | --- | | Step 0:  - Determine DCI format 0\_0 monitored in a common search space according to clause 7.3.1.1.1 where  is the size of the initial UL bandwidth part.  - Determine DCI format 1\_0 monitored in a common search space according to clause 7.3.1.2.1 where  is given by  - the size of CORESET 0 if CORESET 0 is configured for the cell; and  - the size of initial DL bandwidth part if CORESET 0 is not configured for the cell.  - If DCI format 0\_0 is monitored in common search space and if the number of information bits in the DCI format 0\_0 prior to padding is less than the payload size of the DCI format 1\_0 monitored in common search space for scheduling the same serving cell, a number of zero padding bits are generated for the DCI format 0\_0 until the payload size equals that of the DCI format 1\_0.  - If DCI format 0\_0 is monitored in common search space and if the number of information bits in the DCI format 0\_0 prior to truncation is larger than the payload size of the DCI format 1\_0 monitored in common search space for scheduling the same serving cell, the bitwidth of the frequency domain resource assignment field in the DCI format 0\_0 is reduced by truncating the first few most significant bits such that the size of DCI format 0\_0 equals the size of the DCI format 1\_0. |   Therefore, we suggest the following modification: Proposal 1.1-5 (modified)  * Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off). * Same DCI size for DCI 0\_0 in CSS regardless of channel access mode (i.e., LBT on/off)   + ~~Bits will be padded, if needed, to the format with smaller DCI size between the channel access modes to match the DCI size between them.~~   + Existing DCI size alignment in ~~TS38.213~~ TS 38.212 applies to DCI 1\_0 and 0\_0 in CSS.   + FFS: DCI in USS   **Proposal 1.1-6:** Support **Proposal 1.1-7:** Suggest modification  * First, we assume that “MIB content payload” means “MIB or PBCH payload”. However, we prefer to clarify this in the proposal. * Second, we think that DBTW may be disabled but still LBT is used. Therefore, in general, an indication (implicit or explicit) of DBTW disabled cannot be used to infer no-LBT. However, this does not result in any problem during initial access. As it has been clarified already, the only reason that UE may need to know LBT on/off before reading SIB1 is to determine the size of DCI 1\_0 scrambled with SI-RNTI to avoid two blind decoding on DCI size. However, if we unify the size of DCI 1\_0 scrambled by SI-RNTI for the cases of LBT/No-LBT (as suggested in Proposal 1.1-5) UE does not need to know LBT/No-LBT Mode before reading SIB1. LBT/No-LBT mode can then be indicated in SIB1.  **Proposal 1.1-7 (modified)**  * Indication of licensed and unlicensed operation is not explicitly indicated in MIB ~~content~~ or PBCH payload. * Indication of use of LBT or no-LBT is not explicitly indicated in MIB ~~content~~ or PBCH payload.   + ~~If explicit indication of DBTW disabled is supported, use of no-LBT may be inferred from DBTW disabled indication.~~   **Proposal 1.1-8:** Support  Note that Proposal 1.1-8 on its own is the normal UE behavior in Rel-15/16. We think what is more important to agree is the following subsequent Proposal which clarifies UE behavior when Q is configured in operation with shared spectrum. We understand that the support of Q and DBTW are still under discussion, but, given the WA on the support of DBTW for 120 kHz, we think that the following proposal can also be agreed as a WA for 120 kHz.  **Proposal:**  Regardless of the value of the MSB k of inOneGroup and MSB m of groupPresense in ssb-PositionsInBurst configured in SIB1, if > , UE assumes that candidate SSB index(es) corresponding to SSB index equal to are not transmitted. |

#### <Summary of 1st Round of Discussions>

[TBD]

### 2.1.2 SSB Resource Pattern

* From [1] Huawei/HiSilicon:
  + Support following patterns for SSB with 480 kHz and 960 kHz SCS:
    - For operations without shared spectrum:
      * {2,9}+14n, (n=0,1,2,…,31) for both 480 kHz and 960 kHz SCS.
    - For operations with shared spectrum:
      * {2,9}+14n, (n=0,1,2,…,31,40,…,71) for 480 kHz SCS;
      * {2,9}+14n, (n=0,1,2,…,63) for 960 kHz SCS.
* From [2] Futurewei:
  + For SS/PBCH transmission at 480kHz and respectively 960kHz use “n” values that correspond to SS/PBCH transmission gaps of 8 slots and respectively 16 slots to allow low latency traffic transmissions.
* From [4] ZTE, Sanechips:
  + The following design of candidate SSBs with SCS 480/960 kHz in a half frame can be considered: First symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
    - If DBTW is not supported or DBTW is disabled
      * For 480kHz SCS, the 64 candidate SSBs are located in 32 slots, with 2 slots spacing between every 8 consecutive slots to avoid prolonged occupation, i.e. n=0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37
      * For 960kHz SCS, the 64 candidate SSBs are located in 32 slots, with 4 slots spacing between every 16 consecutive slots to avoid prolonged occupation, i.e. n=0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35
    - If DBTW is supported and it is enabled
      * Additional 64 candidate SSB can be defined after the above original 64 candidate SSBs in the half frame
* From [5] vivo:
  + Non-LBT scenario: the value of ‘n’ for SCS 480 kHz and 960 kHz can be set as:
    - n=0,1,4,5,8,9,12,13,16,17,20,21,24,25,28,29,40,41,44,45,48,49,52,53,56,57,60,61,64,65,68,69.
  + LBT scenario: the value of ‘n’ for SCS 480 kHz and 960 kHz can be set as:
    - n=0,1,4,5,8,9,12,13,16,17,20,21,24,25,28,29,40,41,44,45,48,49,52,53,56,57,60,61,64,65,68,69, 80,81,84,85,88,89,92,93,96,97,100,101, 104,105, 108, 109,120,121,124, 125, 128, 129,132,133,136,137,140,141,144,145,148,149
* From [8] NEC:
  + Additional n values of 4, 9, 14 and 19 should be supported to indicate 80 candidate SSBs in DBTW at least for 120 kHz SCS SSB pattern.
  + The indication of additional candidate SSBs based on additional values should be investigated.
* From [9] CATT:
  + Confirming the working assumption of candidate SSB index number of 120 kHz SCS can be postponed to after the decision on maximum number of can SSB index supported for 480/960 kHz.
* From [11] Ericsson:
  + For SS/PBCH block with 120 kHz SCS, no new values of n are supported. Hence the Case D pattern from Rel-15 is supported.
  + For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame, and n = 0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37.
* From [12] Nokia, NSB:
  + Support in for 480kHz and 960kHz SSB pattern design with slots without SSB candidate locations at every 0.25ms.
  + Define SSB slot pattern for 480kHz and 960kHz sub-carrier spacing so that 8 consecutive slots are contain SSB candidate locations, followed by 4 slots are left unoccupied (by SSBs), until all SSBs locations are accounted. Determine the slot indexes n for candidate locations as follows:
    - The slot indexes n={0,1,2,3,4,5,6,7,
    - 12,13,14,15,16,17,18,19,
    - 24,25,26,27,28,29,30,31,
    - 36,37,38,39,40,41,42,43}
* From [13] Samsung:
  + For 480 kHz and 960 kHz, the first symbols of candidate SS/PBCH block have indexes , wherein:
    - for 480 kHz SCS and operation without shared spectrum channel access;
    - for 480 kHz SCS and operation with shared spectrum channel access;
    - for 960 kHz SCS and operation without shared spectrum channel access;
    - for 960 kHz SCS and operation with shared spectrum channel access.
* From [15] Intel:
  + For SSB SCS 120 kHz, reuse Case D pattern for SSB candidate slot positions within a half-frame.
  + Consider SSB pattern in a slot with 3 SSB containing slots, each slot with 2 SSB position, followed by 1 non-SSB carrying slot for 480 kHz and 6 SSB carrying slots followed by 2 non-SSB carrying slots for 960kHz.
    - For 480kHz and 960kHz SCS based SSB, first symbols of the candidate SSB have indexes {2,9} + 14×n, where index 0 corresponds to the first symbol of the first slot in a half-frame.
    - For 480kHz, n = {0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 32,33,34, 36,37,38, 40,41}, {42, 44,45,46, 48,49,50, 52,53,54, 56,57,58, 60,61,62, 64,65,66, 68,69,70, 72,73,74, 76,77,78, 80, 81, 82, 84}.
      * The second set of n values could be used to enable larger number of candidate SSBs, i.e.,
    - For 960kHz, n = {0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40,41}, {42,43,44,45, 48,49,50,51,52,53, 56,57,58,59,60,61, 64,65,66,67,68,69, 72,73,74,75,76,77, 80,81,82,83}.
      * The second set of n values could be used to enable larger number of candidate SSBs, i.e.,
* From [16] NTT Docomo:
  + For SSB slots “n” with 480/960 kHz SCS, the following alternatives can be considered where we prefer Alt 3 the best::
    - Alt 1: Reuse “n” values defined for Case D in Rel-15/16
    - Alt 2: Define “n” values as a set of consecutive slots
    - Alt 3: Define “n” values with more number of non-SSB slots between two set of consecutive SSB slots within a SSB burst
* From [17] Panasonic:
  + For SSB slot position, Case D SSB patten is reused (i.e., n = 0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37).
* From [19] ETRI:
  + Confirm the working assumption on the number of candidates SSBs for 120kHz as an agreement.
* From [20] Lenovo, Motorola Mobility:
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, for higher subcarrier spacings (numerologies) such as 960kHz for SSB, to allow the beam switching between contiguous SSBs and between SSB and CORESET, a gap (for example a symbol gap or post-fix) should be supported for beam switching at least for 960kHz
* From [21] Interdigital:
  + Support using gap slots in Case D SSB pattern in SCS 120kHz for the candidate SSB positions, wherein multiple subsets of candidate SSB indexes per gap slot are considered.
* From [22] LG Electronics:
  + For 480/960 kHz SSB, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame (as per agreement made in RAN1#106-e), and values of ‘n’ are consecutive integers (i.e., n = 0, 1, 2, …, 31).
* From [23] Sharp:
  + Non-contiguous values of n with 3 or 4 gap slots between SSB slots should be considered.
* From [26] Qualcomm:
  + for 480 kHz/960 kHz SSB pattern, consider the following options:
    - For 480 kHz SCS, select one of:
      * SSB slots (n) = {1, 2, 3, 4} + 6\*m, where m = 0, 1, …, 7, or
      * SSB slots (n) = {n1, n2}
        + {n1} = {1, 2, 3, 4} + 6\*m, where m = 0, 1, 2, 3
        + {n2} = {33, 34, 35, 36} + 6\*m, where m = 0, 1, 2, 3
    - For 960 kHz SCS:
      * SSB slots (n) = {2, 3, 4, 5, 6, 7, 8, 9} + 12\*m, where m = 0, 1, …, 7
    - Keep the 20 ms initial access SSB pattern period

Chart

Description automatically generated

#### Summary of Discussions

In previous RAN1 meetings the following agreement was made.

|  |
| --- |
| **Agreement:**  For SSB with 120kHz SCS for NR 52.6 GHz to 71 GHz,   * 120 kHz SCS: the first symbols of the candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n, where index 0 corresponds to the first symbol of the first slot in a half-frame. * For carrier frequencies within 52.6 GHz to 71GHz, support at least 𝑛 = 0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18.   + Other values of *n* (if any) are FFS, and support of additional n values are subject to support of DBTW for 120kHz SSB   **Agreement:**   * For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, X} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.      * Alt 1: X = 8 * Alt 2: X = 9   **Agreement:**  For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame. |

* SSB pattern for 120kHz
  + Use SSB case D from Rel-15 NR
    - Ericsson, Interdigital
* SSB slot pattern for 480 kHz:
  + Continuous slots, {2,9}+14n, (n=0,1,2,…,31)
    - Huawei/HiSilicon (for licensed), Samsung (for licensed), LGE
  + 8 slot gap every 32 slots, (n=0,1,2,…,31,40,…,71)
    - Huawei/HiSilicon (for unlicensed), Samsung (for unlicensed)
  + Gap every 8 slots
    - Futurewei
  + 2 slots gap every 8 slots, n=0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37
    - ZTE, Sanechips, Ericsson, Panasonic
  + n=0,1,4,5,8,9,12,13,16,17,20,21,24,25,28,29,40,41,44,45,48,49,52,53,56,57,60,61,64,65,68,69
    - vivo
  + 4 slot gap every 8 slots, n={0,1,2,3,4,5,6,7,12,13,14,15,16,17,18,19,24,25,26,27,28,29,30,31, 36,37,38,39,40,41,42,43}
    - Nokia/NSB
  + 1 slot gap every 3 slots, n = {0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 32,33,34, 36,37,38, 40,41}, {42, 44,45,46, 48,49,50, 52,53,54, 56,57,58, 60,61,62, 64,65,66, 68,69,70, 72,73,74, 76,77,78, 80, 81, 82, 84}
    - Intel
  + N slot gap every M slots
    - Docomo
  + 3 or 4 slot gap every M slots
    - Sharp
  + 4 slot gap every 8 slots, n={2, 3, 4, 5, 6, 7, 8, 9} + 12\*m
    - Qualcomm
* SSB slot pattern for 960 kHz:
  + Continuous slots, {2,9}+14n, (n=0,1,2,…,31)
    - Huawei/HiSilicon (for licensed), Samsung (for licensed), LGE
  + Continuous slots, (n=0,1,2,…,63)
    - Huawei/HiSilicon (for unlicensed), Samsung (for unlicensed)
  + Gap every 16 slots
    - Futurewei
  + 4 slot gap every 8 slots, n={0,1,2,3,4,5,6,7,12,13,14,15,16,17,18,19,24,25,26,27,28,29,30,31, 36,37,38,39,40,41,42,43}
    - Nokia/NSB
  + 8 slot gap every 16, n=0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35
    - ZTE, Sanechips
  + 2 slot gap every 6 slots, {0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40,41}, {42,43,44,45, 48,49,50,51,52,53, 56,57,58,59,60,61, 64,65,66,67,68,69, 72,73,74,75,76,77, 80,81,82,83}
    - Intel
  + N slot gap every M slots
    - Docomo
  + 2 slots gap every 8 slots, n=0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37
    - Panasonic, Ericsson
  + 4 slot gap every 8 slots, n={2, 3, 4, 5, 6, 7, 8, 9} + 12\*m
    - Qualcomm

#### <Moderator’s Suggestion for Discussions>

Discuss further on the following proposals, including further aspects that should be discussed together with Proposal 1.2-1 and 1.2-2.

##### Proposal 1.2-1

* Use SSB pattern case D from Rel-15 NR for 120 kHz SSB pattern

Moderator Note: Agreement from RAN1#104-bis implies we already agreed to use case D pattern for 120kHz. As Samsung pointed out not sure if this proposal needs to be agreed again.

##### Proposal 1.2-2

* Supported value of n for 480/960kHz SSB slot pattern:
  + ALT 1) contiguous, n = 0, 1, …, Lmax
  + ALT 2) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
    - FFS: whether same pattern will apply to 480kHz and 960kHz (i.e same N and M for 480 and 960 kHz), or scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz)
    - FFS: whether n will start from 0 or N
  + Moderator’s note: If Alt 2 is selected, RAN1 should work further during RAN1 #106bis-e to settle the final slot pattern (i.e. determine values of N and M and FFS aspects)

#### 1st Round of Discussions

Please provide further comments on the above issues (Proposal 1.2-1 and 1.2-2). Especially, which alternative (ALT 1 or 2) should be selected for Proposal 1.2-2. Also, if there are any other issues that require discussion, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| NTT DOCOMO | We agree that Proposal 1.2-1 is something agreed already.  For Proposal 1.2-2, while we are relatively open to discuss, our best preference is ALT 2. We think the benefit given by contiguous “n” would not be significant. |
| OPPO | Proposal 1.2-1: support  Proposal 1.2-2: support |
| Qualcomm | Proposal 1.2-1: ok  Proposal 1.2-2: To allow for gaps for UL/DL switching and URLLC, we support Alt 2 as one option.  However, we prefer the 2nd FFS to be “FFS: starting position of n ~~whether n will start from 0 or N~~”. The reason for this is to allow for the option to be able to align the starting position of the SSB of 480/960 with that of 120 kHz.  Also, although not very strong, but may be good to add Alt 3 at this point to allow for different patterns between 480 and 960 kHz. This is because 480 kHz have longer sweep time and there may be a need to insert a longer gap (e.g. N’ > N) somewhere in the middle. This may not be needed for 960 kHz because of shorter sweep time:  *ALT 3) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB, additional N’ slot gaps may be inserted in the middle of the pattern. N’ may be the same or different for 480kHz and 960kHz.* |
| Lenovo, Motorola Mobility | Proposal 1.2-1: support  Proposal 1.2-2: We prefer Alt 1 but are open to discuss Alt 2. |
| Samsung | Proposal 1.2-1: We believe it is already supported by combining previous agreements.  Proposal 1.2-2: We would like to explain our principle for determining the value of n: in Rel-15, for FR2, slots are reserved after every 1 ms for the purpose of potential URLLC traffic, and we follow exactly the same principle to determine the values of n for 480 kHz and 960 kHz (i.e., align the slots containing SSB with 120 kHz). So in principle, it’s aligned with Alt 2, but it may finally look like Alt 1 if M is sufficiently large (e.g. M=32). For those proposing smaller value of M, we are wondering for FR2-2, why a tighter requirement on the URLLC traffic is considered comparing to FR2-1, and 480/960 kHz SCS has a tighter requirement than 120 kHz SCS?  Moreover, there seems a typo in Alt 1, and the upper bound should be “bar{L}\_max/2-1”. |
| Interdigital | **Proposal 1.2-1**: Support the proposal.  **Proposal 1.2-2**: Support the proposal. |
| LG Electronics | Proposal 1.2-1: We don’t need to discuss about the already agreed feature again.  Proposal 1.2-2: We totally share the view with Samsung. We prefer ALT 1 since the time duration for 64 SS/PBCH blocks for 480/960 kHz is short enough (i.e., less than or equal to 1 msec) and the gap for UL control channel is not required. Also we agree with Samsung’s modification to “bar{L}\_max/2-1”. |
| Ericsson | Proposal 1.2-1: Support. Actually, the RAN1#104bis-e agreement has an FFS, so we think this agreement is still useful. It resolves the FSS to say that no other values of n are supported.  Proposal 1.2-2: We support Alt-2 since we agree that slot gaps can be used for scheduling high priority UL. We are open to discuss what value of M and N is supported; however, we prefer a common design for both 480/960 kHz. |
| ETRI | We support both Proposal 1.2-1 and Proposal 1.2-2. |
| Sharp | Proposal 1.2-1: Okay.  Proposal 1.2-2: we are fine to the solution that aligning design with Rel-15 FR2 (e.g., reserve UL slots every 1 ms). |
| Intel | Proposal 1.2-1: Support.  Proposal 1.2-2: Support.  Our preference is Alt.2  One of the aspects that need to be considered is the multiplexing of SSB and PRACH. Currently the RO slots are 3 or 7 for 480kHz and 7 and 15 for 960kHz.  If SSB are occupying 3 or 7 for 480kHz and 7 and 15 for 960kHz, then we can potentially have collision between SSB and RO. While specification puts priority for SSB and considers any collision invalid ROs, this would mean significant number of ROs are invalided for many PRACH configurations.  Therefore, we think it is important to make sure RO and SSB do not overlap as much as possible and if possible, completely avoided by design. This means we should support at least some gaps for SSB contained slots.  SSB slot pattern of 3 SSB slots followed by 1 non-SSB slot for 480kHz and 6 SSB slots followed by 2 non-SSB slots for 960kHz seems to work well with RO slot placements. Therefore, we suggest going further and try to agree to the exact pattern this meeting.  Please note this is quite different for FR1 and existing FR2 design, as some gaps at the end of the slots were possible to use by PRACH in some PRACH configurations. For 480/960kHz due the short symbol duration and slot duration, we do not expect DL and UL signals to be meaningfully multiplexed in the same slot. Therefore, slots where UL can be sent should be made available in the specifications. |
| vivo | Proposal 1.2-1: Support  Proposal 1.2-2: Prefer Alt. 3 proposed by Qualcomm and can accept Alt. 2.  If looking at 120KHz SSB design, there are two kinds of gaps: one is short gap between contiguous SSB slots which could allow transmission of short UL control information; the other is long gap (i.e. 2 slot gap every 8 SSB slots) which could allow transmission of URLLC traffic. In another word, for short gap, it occurs every 0.125ms to allow short UL control information and occurs every 1ms to allow URLLC data transmission. For 480K and 960KHz design, at least the same goal as above should be achieved. If Alt. 1 is adopted, considering UL DL switching time, short UL control information can only be sent after 1ms, which becomes even worse than 120KHz. So Alt. 1 is not acceptable to us.  To allow short control information, N=1 or 2 may be enough considering 7us UL-DL switching time. However, to allow URLLC traffic transmission, larger N’ may be needed. So Alt. 3 proposed by Qualcomm is preferred by us. Besides, to allow larger N’ in the middle could easily align the SSB position for 120KHz. One example is provided below (N=2, M=2, N’=8): |
| Huawei, HiSilicon | **Proposal 1.2-1**: support  **Proposal 1.2-2:** Suggest modification. Note that:   * If is agreed for 480/960, then the candidate SSBs for 480 kHz with DBTW ON span the duration that is approximately 4 times longer than the SSB burst for 960 kHz with DBTW OFF. So, we don’t think that exactly the same SSB pattern design should necessarily be used for both cases. * As Rx-Tx and Tx-Rx transition may be up to 7.015 usec (approximately 7 symbols in 960 kHz), a considerable portion of UL slots may be wasted in the transition time. Therefore, to reduce the percentage of transition time overhead, it is more sensible to reserve less number of set of consecutive slots for UL but, within each set, use more slots. * To this end, we prefer to use the same design principle as in 120 kHz Cased D for 480/960 kHz SSB: Reserve the slots for UL in 480/960 kHz that correspond to the reserved UL slots for Case D in 120 kHz:     As only 480 kHz SSB burst with DBTW ON spans more than equivalent of 8 slots in 120 kHz and the first slots in 120 kHz Case D that are reserved for UL are slots 9 and 10, we suggest to reserve the corresponding slots in 480 kHz with DBTW ON (slots 32 to 39) for UL as well. In all other cases, reserving UL slots are not necessary. We would like to add this option as an alternative to Proposal 1.2-2.  Also**,** in the first bullet should be changed to to be accurate ( is the maximum number of candidate SSBs and there are two SSBs per slot. Note that if DBTW is not agreed). We suggest the following: Proposal 1.2-2 (modified)  * Supported value of n for 480/960kHz SSB slot pattern:   + ALT 1) contiguous, n = 0, 1, …, ~~L~~~~max~~   + ALT 2) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB     - FFS: whether same pattern will apply to 480kHz and 960kHz (i.e same N and M for 480 and 960 kHz), or scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz)     - FFS: whether n will start from 0 or N   + ALT 3) slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.     - Note: ALT 3 means that only slots 32-39 for 480 kHz SSB pattern are reserved for UL and 960 kHz SSB pattern is contiguous. |

#### <Summary of 1st Round of Discussions>

[TBD]

### 2.1.3 CORESET#0 Configuration

* From [1] Huawei/HiSilicon:
  + For CORESET for Type0-PDCCH in 52.6GHz to 71GHz spectrum, support the following:
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {120, 120} kHz, support multiplexing pattern 1 and multiplexing pattern 3 as per Agreement in RAN1 104-e.
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {480, 480} kHz, support multiplexing pattern 1 only.
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {960, 960} kHz, support multiplexing pattern 1 only.
  + For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {120, 120} kHz, in addition to the supported values of (, ) from Rel-15, support = 96 with ={1,2} for multiplexing pattern 1.
  + Support the following CORESET#0 RB offsets values for {SSB, CORESET#0} SCS={120, 120} kHz:
    - For CORESET#0 with 24 RBs and 48 RBs: the same as supported values in Table 13-8 of 38.213.
    - For CORESET#0 with 48 RBs: additional RB offsets values of 0 and 28 RBs can be considered for multiplexing pattern 1.
    - For CORESET#0 with 96 RBs: RB offsets values of 0 and 76 RBs can be considered for multiplexing pattern 1.
    - Note: All above RB offsets are nominal and may need to be modified after finalizing synch raster and channel raster design in FR2-2.
  + Support the following CORESET#0 RB offsets values for {SSB, CORESET#0} SCS={480, 480} kHz and {960, 960} kHz:
    - For CORESET#0 with 24 RBs: the same as supported values in Table 13-8 of 38.213.
    - For CORESET#0 with 48 RBs: In addition to the offset of 14 RBs already supported in Rel-16, additional values of 0 and28 RBs can be considered for multiplexing pattern 1.
  + The parameters for PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 1 listed in Table [1]-4 and Table [1]-5 should be supported. For 480kHz and 960 kHz SCS, the scaling factor X in Table 5 is when DBTW is OFF and when DBTW is ON.
    - Note: DBTW OFF is indicated in MIB using a value of

Table 4 Parameters for PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 1 and FR2-2 when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index |  | Number of search space sets per slot |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 5 | 1 | 1 | 0 |
| 2 | 0 | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 3 | 5 | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 4 | 0 | 2 | 1/2 | {0, if is even}, {, if is odd} |
| 5 | 5 | 2 | 1/2 | {0, if is even}, {, if is odd} |
| 6 | 0 | 1 | 2 | 0 |
| 7 | 5 | 1 | 2 | 0 |

Table 5 Parameters for PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 1 and FR2-2 when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz or {960, 960} kHz

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index |  | Number of search space sets per slot |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 2 | 5X | 1 | 1 | 0 |
| 3 | 5X | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 6 | 5+5X | 1 | 1 | 0 |
| 7 | 5+5X | 2 | 1/2 | {0, if is even}, {7, if is odd} |
| 8 | 0 | 1 | 2 | 0 |
| 9 | 5 | 1 | 2 | 0 |
| 10-15 | Reserved | | | |

* + To find the offset between an off-synch raster SSB and the corresponding CORESET#0 in 60GHz unlicensed spectrum, RAN1 should uniquely determine the hypothetical on-synch raster SSB that serves as the reference for the offset to the off-synch raster SSB in case more than one synch rasters are included in a channel bandwidth.
* From [2] Futurewei:
  + Rel 17 FR2-2 the SS/PBCH and CORESET#0 for Type0-PDCCH should have only the same SCS.
  + Use O from the set {0, 5, 2.5, 5+2.5} for 120 kHz, {0, 5, 2.5/X, 5+2.5/X} for 480 kHz, and {0, 5, 2.5/(2\*X), 5 + 2.5/(2\*X)} for 960 kHz, with X values TBD.
* From [4] ZTE, Sanechips:
  + In addition to multiplexing pattern 1, multiplexing pattern 3 for three approved SCS combinations of SSB and Type0-PDCCH can also be considered in FR2-2.
    - (SSB, Type0-PDCCH): SCS (120 kHz, 120 kHz)
    - (SSB, Type0-PDCCH): SCS (480 kHz, 480 kHz)
    - (SSB, Type0-PDCCH): SCS (960 kHz, 960 kHz)
  + For {SSB, CORESET# for Type0-PDCCH} SCS = {120, 120} kHz, even though RAN4 has agreed the minimum CBW is increased to 100 MHz, at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 should still be supported.
* From [5] vivo:
  + Support Multiplexing pattern 1 and 3 for SCS 120 kHz, and support Multiplexing pattern 3 for SCS 480 kHz and 960 kHz when operation in FR2-2.
  + Support 96 RB for SCS 120kHz and 480 kHz. Do not support 96 RB for SCS 960kHz.
  + If the sync raster/ channel raster is designed with FR 2-1, the existing RB offset design can be reused for SCS 480 kHz and 960 kHz. Otherwise, the RB offset should be re-designed.
  + For {SSB, PDCCH} SCS {120, 120} kHz, {480, 480} kHz and {960, 960} kHz, the tables for PDCCH monitoring occasions for type0-PDCCH CSS set configuration defined for FR2-1 in Rel-15 can be reused with little adjustment.
* From [9] CATT:
  + The subCarrierSpacingCommon field in MIB can be saved and repurposed.
  + Multiplexing pattern 2 or 3 can be used for further multiplexing SSB/CORSET#0 with periodic CSI-RS/paging PDCCH&PDSCH in frequency.
  + For SSB and CORESET#0/Type0-PDCCH with 120 KHz SCS, support the following combinations of SSB/CORESET multiplexing pattern, number of RB and symbols for CORESET.
    - {mux pattern 1, 48 PRB CORESET, 1 symbol CORESET}
    - {mux pattern 1, 48 PRB CORESET, 2 symbol CORESET}
    - {mux pattern 3, 48 PRB CORESET, 2 symbol CORESET}
  + The configuration of {0, if *i* is even}, {, if *i* is odd} can be supported, considering for SCS=120 KHz use case, the gNB could use implementation to avoid beam switching gap issue if it choose to.
  + The default TDRA table for pattern 1 in TS 38.214 can be enhanced, e,g at least {S=6 ,L=7}, {S=2，L=11} is supported.
* From [10] Xiaomi:
  + Detail parameters modification for controlResourceSetZero configuration should be based on channel and sync raster design in RAN4.
* From [11] Ericsson:
  + RAN1 should strive to design a common CORESET0 configuration table for use for all 3 supported SCS combinations (120,120), (480,480), and (960, 960).
  + If RAN4 defines a floating channelization with a sync raster granularity in line with the design, add offset values 2 and 26 for the option of 48 RB CORESET0 and make Table 13-8 in 38.213 applicable also for operation with 480 and 960 kHz SCS.
  + Reuse existing Table 13-12 in 38.213 for operation with 480 and 960 kHz SCS. For subcarrier spacings 480 and 960 kHz, select Alternative 1 to define offset values.
* From [12] Nokia, NSB:
  + For CORESET#0 with 120kHz sub-carrier spacing, consider supporting also ={96} for multiplexing pattern 1.
  + For SSB and CORESET#0 with 480kHz sub-carrier spacing with SSB and CORESET#0 multiplexing pattern 3, following configuration options could be considered:
    - ={2}
    - ={24, 48}.
  + Support the following ’O’ values for both 480 and 960 kHz sub-carrier options: {0, 1.5, 5, 6.5} ms.
  + Support values {1,2} for the number of search space sets per slot, and values {1, 1/2} for the shift M. Additionally, given room in table also M={2} could be supported.
  + Support first symbol index configuration options 0 and {0, if  is even}, {7, if  is odd}
  + Support Type0-PDCCH CSS configuration presented in Table [12]-7 for multiplexing pattern 1.

|  |  |  |  |
| --- | --- | --- | --- |
| **O** | **Number of search space sets per slot** |  | **First symbol index** |
| 0 | 1 | 1 | 0 |
| 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 1.5 | 1 | 1 | 0 |
| 1.5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 5 | 1 | 1 | 0 |
| 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6.5 | 1 | 1 | 0 |
| 6.5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 0 | 1 | 2 | 0 |
| 5 | 1 | 2 | 0 |

* + Consider also SSB and CORESET#0 multiplexing pattern 3 for 120kHz SSB.
  + Pending on the UE minimum BW capability, consider also SSB and CORESET#0 multiplexing pattern 3 for 480kHz SSB.
* From [13] Samsung:
  + For CORESET#0 configuration with 120 kHz SCS,
    - additional CORESET#0 RB offsets are needed;
    - support 96 RB as the number of RBs for CORESET#0.
  + For CORESET#0 configuration with 480 kHz and 960 kHz SCS,
    - support multiplexing pattern 3;
    - support 96 RB as the number of RBs for CORESET#0;
    - further study the RB offset based on RAN4 design of channel and synchronization rasters.
  + Type0-PDCCH configuration, support all configurations from Rel-15 table except for the changes to O values:
    - For 120 kHz, ;
    - For 480 kHz, ;
    - For 960 kHz, .
  + For 480 kHz and 960 kHz SCS, a UE only monitors one slot for Type0-PDCCH:
    - Alt 1: the one slot is slot for all cases;
    - Alt 2: the one slot is slot for and , and configured from slot and for
* From [14] Mediatek:
  + Support adjusting the time-domain offset between SSB and CORESET #0 for 480/960 kHZ SCS.
* From [15] Intel:
  + Support 96 PRB CORESET for {SS/PBCH, PDCCH} equal to {120,120}, {480,480} and {960,960} kHz with = {1, 2}.
  + Support the following CORESET#0 RB offset values for {120, 120} kHz, {480, 480}, {960, 960} kHz for multiplexing patterns 1 and 3:
    - For CORESET#0 with 24 RBs: [0] for multiplexing pattern 1 and –20 if kssb =0 (-21 if kssb > 0) for multiplexing pattern 3.
    - For CORESET#0 with 48 RBs: [0], for multiplexing pattern 1 and –20 if kssb =0 (-21 if kssb > 0) for multiplexing pattern 3.
      * FFS: inclusion of RB offset of [1]
    - For CORESET#0 with 96 RBs: [0] for multiplexing pattern 1 and –20 if kssb =0 (-21 if kssb > 0) for multiplexing pattern 3.
    - Modify Table 13.8 in TS 38.213 to support the proposed RB offset when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz
    - Support addition of a new table in 38.213 for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {480, 480} kHz or {960, 960} kHz.
  + For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,
    - Support O = {0, 2.75, 5, 7.75} for 480kHz (in case Lmax = 128)
    - Support O = {0, 1.5, 5, 6.5} for 960kHz {in case Lmax = 128)
  + The equation for determining the slot number for PDCCH monitoring is modified to account for the non-contiguous numbering of the SSB slot pattern for {SSB, Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz.
    - Support the following modified equation:
    - For 480 kHz: where and
    - For 960 kHz: where and
* From [16] NTT Docomo:
  + If time allows, support the following for 480/960 kHz SCS, considering the support of two sets of SSB-CORESET#0 multiplexing within a slot:
    - More number of RBs for CORESET#0 PDCCH
    - Enhance Default PDSCH TDRA Table A
  + If time allows, support smaller ‘O’ value especially for 960 kHz SCS
* From [17] Pansonic:
  + 96 PRB CORESET for 120 kHz SCS is supported.
* From [21] Interdigital:
  + Introduce the enhancements on SS/PBCH block transmission patterns to deliberately include the CORESET#0 and SIB1 in fixed time locations along with the corresponding SS/PBCH block to ensure the channel occupancy as much as possible, in the initial access operations with 120kHz SCS for unlicensed spectrum in beyond 52.6GHz.
* From [22] LG Electronics:
  + Reuse Table 13-12 in TS 38.213 specification for type0-PDCCH CSS set configuration with 120/480/960 kHz, except for O values for 480/960 kHz.
* From [23] Sharp:
  + For Type0-PDCCH CSS set configuration rows where the first symbol index is given by {0, if i is even}, {, if i is odd}, the configuration rows should be modified such that gap symbols between different beams can be supported.
  + ‘O’ is from the set {0, 5, X5, 5+ X5} for 480 kHz, and {0, 5, X6, 5 + X6} for 960 kHz, where X5 and X6 stand for durations that count for consecutive transmission of SSB burst of 480kHz SCS and 960kHz SCS, respectively.
* From [24] Apple:
  + In addition to 24 and 48 PRBs, 96 PRBs can be considered for CORESET#0 BW with 120kHz SCS.
  + For Type0-PDCCH Mos determination, the offset values are defined as for 480kHz and 960kHz SCS respectively, where .
* From [26] Qualcomm:
  + for FR2-2, CORESET0 SCS = SSB SCS for all SCSs
  + consider minimizing the overhead of beam switching gaps by supporting multiplexing pattern 3
  + for ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, the following set of parameters are supported for SS/PBCH block and CORESET multiplexing pattern 1:

|  |  |  |
| --- | --- | --- |
| Number of search space sets per slot | M | First symbol index |
| 1 | 1 | 0 |
| 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | 1/2 | {0, if  is even}, {+ 1, if  is odd} |
| 1 | 2 | 0 |

* + - Note: the number of entries corresponding the same {number of SS per slot, M, first symbol index} tuple (listed above) will depend on supported ‘O’ for each tuple
    - For 960 kHz, re-interpret the offsets of O = {0, 2.5, 5, 7.5} from Table 13-12 as O = {0, 1.25, 5, 6.25}

#### Summary of Discussions

In RAN1 #104e and #105e the following agreement was made.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Agreement:**  For CORESET#0 and Type0-PDCCH search space configured in MIB:   * Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {120, 120} kHz   + Support at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 for {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS = {120, 120} kHz.     - FFS: Supporting additional values   + FFS: Supported values for SSB to CORESET#0 offset RBs * If 480kHz SSB SCS that configures CORESET#0 and Type0-PDCCH CSS in MIB is agreed to be supported,   + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {480, 480} kHz * If 960 kHz SSB SCS that configures CORESET#0 and Type0-PDCCH CSS in MIB is agreed to be supported,   + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {960, 960} kHz * If 240 kHz SSB SCS is agreed to be supported,   + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {240, 120} kHz * FFS: any other combinations between one of SSB SCS (120, 240, 480, 960) and one of CORESET#0 SCS (120, 480, 960)   + FFS: initial timing resolution based on low SCS (120 kHz) and its impact on the performance of higher SCS (480/960 kHz)   **Agreement:**  For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,   * Support the following set of parameters.  |  |  |  | | --- | --- | --- | | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | | 1 | 24 | 2 | | 1 | 48 | 1 | | 1 | 48 | 2 |  * + Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design. * FFS: addition other set of parameters |

The following are a summary of company views on CORESET#0 configuration aspects.

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz
  + controlResourceSetZero
    - Addition of 96 PRB CORESET#0 with {1,2} symbols
      * Support: Huawei/HiSilicon, vivo, Nokia/NSB, Samsung, Intel, Panasonic, Apple
      * Do not support: LGE
    - Addition of mux pattern 3
      * Support: Huawei/HiSilicon (according to RAN1#104-e agreement), ZTE/Sanechips, vivo, [CATT], Nokia/NSB, Intel, LGE
      * Do not support:
    - RB offset values for Mux 1
      * 24 RB
        + 0, 4 : Huawei/HiSilicon
        + 0: Intel
      * 48 RB
        + 0, 28: Huawei/HiSilicon
        + 2, 14, 26: Ericsson
        + 0, 1: Intel
      * 96 RB
        + 0, 76: Huawei/HiSilicon
        + 0: Intel
  + searchSpaceZero
    - Use Table 13-12 (originally intended for {120,120} kHz)
      * Samsung, Intel, LGE
    - Use Table 13-12 (originally intended for {120,120} kHz) except O values (2.5 and 7.5)
      * Huawei/HiSilicon
* For {SSB, CORESET#0/Type0-PDCCH} = {480, 480} and {960, 960} kHz
  + controlResourceSetZero
    - Addition of 96 PRB CORESET#0
      * Support: vivo (for 480kHz), Intel
      * Do not support: vivo (for 960kHz), LGE
    - Addition of mux pattern 3
      * Support: ZTE/Sanechips, [CATT], Nokia/NSB (for 480kHz), Samsung, Intel, Qualcomm, LGE
      * Do not support: Huawei/HiSilicon
    - RB offset values for Mux 1
      * 24 RB
        + 0, 4 : Huawei/HiSilicon, Ericsson (for 960kHz)
        + 0: Intel
      * 48 RB
        + 0, 14, 28: Huawei/HiSilicon
        + 2, 14, 26: Ericsson
        + 0: Intel
      * 96 RB
        + 0: Intel
    - RB offset values for Mux 3
      * -20/-21 depend on k\_ssb
      * N, where N is number of RBs for CORESET
  + searchSpaceZero
    - Use Table 13-12 (originally intended for {120,120} kHz) except O values
      * Nokia/NSB, Intel, LGE
    - Based on Table 13-12 (originally intended for {120,120} kHz) except O values and remove the rows with First symbol index {N\_symb^CORESET, if i is odd}
      * Huawei/HiSilicon
    - O values
      * {0, 5/X, 5, 5 + 5/X} with X = 2^(µ-3) for DBTW OFF, X = 2^(µ-4) for DBTW ON
        + Huawei/HiSilicon
      * {0, 5, 2.5/X, 5+2.5/X} for 480 kHz and {0, 5, 2.5/(2X), 5+2.5/(2X)} for 960 kHz
        + Futurewei
      * {0, 1.5, 5, 6.5}
        + Nokia/NSB
      * {0, 1.25, 5, 6.25} for 480 kHz and {0, 0.625, 5, 5.625} for 960 kHz
        + Samsung, Apple
      * {0, 2.75, 5, 7.75} for 480 kHz and {0, 1.5, 6, 6.5 } for 960 kHz
        + Intel
      * {0, 5, X, 5 +X} for 480kHz and {0, 5, Y, 5+Y} for 960kHz, X and Y are slot duration number that correspond to SSB burst
        + Sharp
      * {0, 2.5, 5, 7.5} for 480 kHz and {0, 1.25, 5, 6.25} for 960 kHz
        + Qualcomm
* Other proposals
  + Common CORESET and SS table for all SCS
    - Ericsson
  + For 480 kHz and 960 kHz, whether to monitor Type0-PDCCH in n0 only or in {n0, n0+1}
    - Samsung
  + Update PDCCH monitoring equation to account to non-contiguous numbering of SSB slots pattern for 480/960kHz
    - Intel
  + Enhancement of default PDSCH TDRA Table A
    - NTT Docomo, CATT

#### <Moderator’s Suggestion for Discussions>

Discussion and decisions are needed for the following issues:

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz
  + Whether or not to include 96 PRB CORESET
    - 9 company support, no objections so far
  + Whether or not to support mux pattern 3 – RAN1 seemed to have agreed to this in RAN1 #104-e
  + searchspaceZero - Use Table 13-12 as is or with modifications (e.g. O values, removal of entries, etc)
  + RB offset values for 24, 48, [96] PRB CORESET: FFS
* For {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and = {960, 960} kHz
  + Whether or not to include 96 PRB CORESET
  + Whether or not to support mux pattern 3
    - 7 companies support, 2 companies do not support
  + searchspaceZero - Use Table 13-12 with modification of O values
    - whether or not to use different O value depending on whether DBTW is ON/OFF
    - {0, 5, X, 5 +X} for 480kHz and {0, 5, Y, 5+Y} for 960kHz, values of X and Y FFS
  + RB offset values for 24, 48, [96] PRB CORESET: FFS
* Other proposals that require discussions
  + Common CORESET and SS table for all SCS
  + For 480 kHz and 960 kHz, whether to monitor Type0-PDCCH in n0 only or in {n0, n0+1}
  + Update PDCCH monitoring equation to account to non-contiguous numbering of SSB slots pattern for 480/960kHz
  + Enhancement of default PDSCH TDRA Table A
    - Discuss in Section 2.1.5

Moderator would like to encourage companies to initiate some discussion on RB offset values for CORESET. RAN1 has 1 more meeting left (in November) before completion of release 17 for RAN1. RAN4 does not have a meeting until November, and if RAN4 does not complete the raster design by November, then RAN1 may not be able complete the specification. Therefore, moderator suggests companies to investigate into RB offset values needed based on currently available raster proposals in RAN4. RAN1 can potentially make tentative proposals for few potential raster scenarios (being considered in RAN4). This way RAN1 at least has some idea on how many entries will be used for CORESET#0 and is able to pick out a final set as soon as RAN4 concludes on the raster design.

**Issue #1)**

##### Proposal 1.3-1

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations

**Issue #2)**

##### Proposal 1.3-2

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz,
  + use Table 13-12 in TS38.213 for multiplexing pattern 1,
  + use Table 13-15 in TS38.213 for multiplexing pattern 3.

Moderator note: As pointed out by few companies, RAN1 agreement from #104 implies multiplexing pattern 3 is agreed to be supported.

**Issue #3)**

##### Proposal 1.3-3

* For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:
  + FFS: The value of X (≥ 0)
  + FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
  + FFS: whether or not to use same or different X value for 480 and 960 kHz

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index |  | Number of search space sets per slot |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | ~~2.5~~ X | 1 | 1 | 0 |
| 3 | ~~2.5~~ X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 7 | ~~2.5~~ X | 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 9 | ~~7.5~~ 5 + X | 1 | 1 | 0 |
| 10 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 11 | ~~7.5~~ 5 + X | 2 | 1/2 | {0, if  is even}, {, if  is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

##### Proposal 1.3-4

* If supported, for ‘searchSpaceZero’ configuration for {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 3:

|  |  |  |
| --- | --- | --- |
| Index | PDCCH monitoring occasions (SFN and slot number) | **First symbol index**  **(*k* = 0, 1, … 31)** |
| 0 |  | 2, 9 in |
| 1 ~ 15 | Reserved | |

**Issue #4)**

Discuss further on the following issue:

* For 480 kHz and 960 kHz, whether to monitor Type0-PDCCH in n0 only or in {n0, n0+1}

**Issue #5)**

Discuss further on the following issue:

* Update PDCCH monitoring equation to account to non-contiguous numbering of SSB slots pattern for 480/960kHz

**Issue #6) RB offset values**

Moderator would like to encourage companies provide companies views on the required RB offsets, even if they are speculative (based on specific assumptions in raster design in RAN4). If possible, please share details of how required RB offset were computed (similar to how [11] from Ericsson provided information on the assumptions).

#### 1st Round of Discussions

Please provide further comments on the above issues #1 ~ #6. Also, if there are any other issues that require discussion, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| NTT DOCOMO | For issue #1, we support the proposal 1.3-1, while we can also live with deferring this decision.  For issue #2, we support the proposal 1.3-2.  For issue #3, we support the proposal 1.3-3 and 1.3-4.  For issue #4, it depends on the design of multi-slot PDCCH monitoring capability.  For issue #5, we do not understand the motivation of such updates. Could someone clarify? |
| OPPO | Proposal 1.3-1: support  Proposal 1.3-2: support  Proposal 1.3-3: not support. We prefer to change O from {0, 2.5, 5, 7.5} to {0, X, Y, Z} and FFS the values of X, Y, Z at current stage.  Proposal 1.3-4: support  Regarding issue #4, two PDCCH monitoring occasions as legacy should be supported. For the monitoring span, UE capability (e.g., slot-group based) could be considered. |
| Qualcomm | Issue #1 (Proposal 1.3-1): no strong view  Issue #2 (Proposal 1.3-2): we are fine with this proposal  Issue #3   * Proposal 1.3-3:   + We are fine with the ‘O’ portion of the proposal   + For the “First symbol index” we think that back-to-back SS0 is not possible if beam switching gaps are needed. Hence, we prefer {0, if  is even}, {+ 1, if  is odd} * Proposal 1.3-4: we are fine with this proposal   Issue #4: This can be discussed in agenda 8.2.2 |
| Lenovo, Motorola Mobility | Issue #1 (Proposal 1.3-1): support  Issue #2 (Proposal 1.3-2): support  Issue #3 (Proposal 1.3-3 and Proposal 1.3-4): We are fine with both proposals  Issue #4 we agree with Qualcomm that it can be discussed in 8.2.2. |
| Samsung | Proposal 1.3-1: We support the proposal.  Proposal 1.3-2: We support the proposal. Just one typo in the main bullet, and one clarification on moderator’s note.   * For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} SCS = {120, 120} kHz,   + use Table 13-12 in TS38.213 for multiplexing pattern 1,   + use Table 13-15 in TS38.213 for multiplexing pattern 3.   Moderator note: As pointed out by few companies, RAN1 agreement from #104 implies multiplexing pattern 3 is agreed to be supported for {SSB, CORESET#0/Type0-PDCCH} SCS = {120, 120} kHz.  Proposal 1.3-3: We support the proposal. There is a bracket on X>=0 - although we believe X cannot be 0, but it’s ok to leave it there.  Proposal 1.3-4: We support the proposal. Maybe the following rewording is more clear.   * If multiplexing pattern 3 is supported for {SSB, CORESET#0/Type0-PDCCH} SCS = {480, 480} kHz and {960, 960} kHz, ‘searchSpaceZero’ configuration uses the following table:   Issue 4: We support only monitoring one slot for Type0-PDCCH for 480 kHz and 960 kHz, to avoid back-to-back slot monitoring for such higher SCSs. The slot can be fixed as n0 or configurable between n0 and n1 (using reserved rows in searchSpaceZero)  Issue 5: It’s not preferable to have non-contiguous burst of RMSI, which cases many LBT operation for unlicensed band. |
| Interdigital | **Proposal 1.3-1**: Do not support 96 RBs as it is not necessary.  **Proposal 1.3-2**: Support the proposal.  **Proposal 1.3-3**: Support the proposal.  **Proposal 1.3-4**: Support the proposal. |
| LG Electronics | Proposal 1.3-1: We do not support introducing 96 PRBs since it is not essential.  Proposal 1.3-2: OK also with Samsung’s modifications.  Proposal 1.3-3: Support  Proposal 1.3-4: Support  Issue #4: We agree with Qualcomm that it can be discussed in 8.2.2.  Issue #5: This is tightly related with Proposal 1.2-2. If alt 1 (contiguous slot pattern) is adopted, we don’t need discuss any more on this proposal.  Issue #6: One way could be to keep the same RB offset values as in Rel-15 and inform it RAN4 to check whether it would be problematic or not when sync/channel rasters are designed. |
| Ericsson | Issue #1  **We do not support Proposal 1.3-1 (yet)**. As we stated before, we think this is a not essential optimization. However, we can be open to discuss this later after it is known how many entries of the CORESET0 configuration table are available, e.g., after RAN4 completes its channelization design and the RB offsets are known at least =for 48 and 24 RB CORESET0. Hence, for now this should be deferred.  Issue #2  We support Proposal 1.3-2 with the typo correction from Samsung.  Issue #3  **We support Proposal 1.3-3**. Agree with Samsung that the (≥0) can be removed from the first FFS. My mistake in the comments I made previously – it should have been X > 0.  **We do not support Proposal 1.3-4 (yet)**. This should be deferred, and if there is time left at the end of the WI to have a full design for multiplexing pattern 3 (including CORESET0 configuration and offsets), we can treat it then. We note the following from the WID:   * + - Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis.   Issue #4  We prefer a common design for all 3 SCSs.  We don't agree that this is an issue to be discussed.  Issue #5  We don't understand the rationale behind this proposal. What does "non-contignous number of SSB slots pattern" mean? This seems like a deviation from Rel-15 design, and we don’t see the point. Moreover, we prefer a common design for all 3 SCSs.  Issue #6  In our contribution on channelization design (R1-2109441), we investigate the needed SSB-CORESET0 offsets and find that they depend on (1) the sync raster granularity, and (2) the spectral utilization, i.e., # of RBs in a given nominal channel bandwidth (e.g., 66 RBs in 100 MHz BW in Rel-15). We found that if RAN4 follows the design paradigm from Rel-15 to have a regularly spaced channel and sync raster for the 57–71 GHz band, where the latter is more coarse than the former (Option 1-C being discussed in RAN4), the the following offsets are needed:   * 48 RB CORESET0: {2 14 26} RBs (assuming 86.4% spectral utilization) or {0 14 28} RBs (assuming > 90% spectral utilization) * 24 RB CORESET0: {0 4} RBs   Of course the final values will depend on what RAN4 decides, our view is that for multiplexing pattern 1 with both 1 and 2 symbol CORESET0, RAN1 should keep a placeholder for up to 3 offsets for 48 RB CORESET0 and up to 2 offsets for 24 RB CORESET0. |
| ETRI | For Issue #1, we support Proposal 1.3-1.  For Issue #2, we support Proposal 1.3-2.  For Issue #3, we support Proposal 1.3-3 and Proposal 1.3-4  For Issue #4, we agree with Qualcomm |
| Sharp | Issue #1: we are fine with Proposal 1.3-1.  Issue #2: we are fine with Proposal 1.3-2.  Issue #3: we generally support Proposal 1.3-3 and share the same view from Qualcomm on “first symbol index”. In addition, we think that the back-to-back Type0-PDCCH problem could be solved by shifting the first symbol index for the O > 0 cases. While for O = 0, {0, if  is even}, {, if  is odd} should be reused.  We are fine with Proposal 1.3-4.  Issue #4: Agree this issue should be handled in AI8.2.2. |
| Intel | Issue #1: Proposal 1.3-1 Support  Issue #2: Proposal 1.3-2 Support  Issue #3: Proposal 1.3-3 Support  Proposal 1.3-4 Support  For SCS 480 kHz and 960 kHz, we support X values of 2.75 and 1.5 respectively. Values smaller than this may potentially lead to overlapped placement of Type0-PDCCH in case of 128 SSB candidates. Existing values may not allow co-location of Type-0 PDDCH in the same slot as the SSB.  Issue #4: while our preference is to keep the monitoring behavior for Type0-PDCCH the same (i.e. two slots n0 and n0+1) but we are open for discussion. We would like to ask proponents of single slot monitoring, what kind of UE complexity benefit they think could be achieved given that Type0-PDCCH monitoring only happens every 20msec and only when system information needs to be decoded, which is very seldom event.  Issue #5: We propose modifying the PDCCH monitoring equation to account for non-contiguous slot numbering in case of 480 kHz and 960 kHz SCS. FR1 SSB slot pattern was consecutive since empty symbols in each slot could be utilized for uplink transmission. For 480 kHz and 960 kHz since the symbol and slot duration is smaller, the gNB will need to utilize empty slots after the SSB slots for uplink. The existing equation does not account for the non-contiguous numbering of the slot pattern. In the figure below (M=0.5), Type0-PDCCH for SSB#6 and SSB#7 will be monitored in slot 3, which in this example is a non-SSB carrying slot and collocation of Type0-PDCCH and SSB in the same slot will not be possible.    Issue #6: We propose RB offset values [0, 1] for multiplexing pattern 1 and [-20/-21] for multiplexing pattern 3 for 24, 48, 96 PRB CORESET. Based on our study, these values would be sufficient for spectrum utilization of 89% or higher. Some analysis is described in our Tdoc R1-2109598. |
| vivo | Proposal 1.3-1: Support.  Proposal 1.3-2: Support.  Proposal 1.3-3: We think the value of ‘X’ is also depended on the duration of candidate SSBs. It is preferable to determine the SSB resource pattern first.  Proposal 1.3-4: Support. |
| Huawei, HiSilicon | **Proposal 1.3-1:** Support  **Proposal 1.3-2:**  We cannot agree with the first sub-bullet of this proposal. We think that O values 2.5 and 7.5 are not justifiable for 120kHz FR2-2. These values are included in Table 13-12 of 38.213 to accommodate 120 kHz Type0-PDCCH allocation right after the 240 kHz SSB burst set. This is a non-existent scenario in FR2-2 and we don’t see why they need to be supported. We suggest the following modification Proposal 1.3-2 (modified)  * For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz,   + use Table 13-12 in TS38.213 for multiplexing pattern 1 excluding the rows corresponding to O=2.5 and O=7.5,   + use Table 13-15 in TS38.213 for multiplexing pattern 3.   **Proposal 1.3-3:** We can agree with the proposal if rows 6,7,8, 11 are removed (corresponding to {, if  is odd})  We are OK with the O values.We still have serious concern about the“First symbol index” values of {, if  is odd} and we think they should be removed due to the beam switching gap requirement. While Qualcomm’s proposal ({+ 1, if  is odd}) may address the beam switching gap requirement, considering that even index SSBs are located at symbol 2, the only way that CORESET0 of odd SSBs do not collide with the even SSBs is to configure CORESET0 set after the SSB burst set. In such a case, considering that SSB burst set length is at least 32 slots, we don’t see any real advantage of using {+ 1, if  is odd} compared to {7, if  is odd} for CORESET#0 location in terms of initial access latency reduction: If CORESET0 set has to be configured after at least 32 slots SSB burst set, configuring the odd CORESET0 4 or 5 symbols (7-(+1)) earlier within the same slot does not really contribute in initial access latency reduction.  More important, ({0, if  is even}, {7, if  is odd}) has another advantage compared to ({0, if  is even}, {, if  is odd}): It facilitates configuring PDSCH associated with Type0-PDCCH right after the corresponding Type0-PDCCH at symbol if i is even and 7+ if i is odd. This further relieves UE from beam switching for the whole half of the slot.  **Proposal 1.3-4:**  RAN1 has not agreed to support Multiplexing pattern 3 for {CORESET0, SSB} = {480, 480} kHz or {960, 960} kHz. Therefore, discussing the corresponding ‘searchSpaceZero’ Table for {480, 480} kHz or {960, 960} kHz seems to be premature. Also a minor note: k may go larger than 31 if DBTW is agreed for 480/960 kHz.  **Issue #6) RB offset values**  For us, the first priority regarding RB offset is that, for MUX1 and for any supported CORESET#0 #RBs and #Symbols, at least one of the lowest RB or the highest RB of CORESET#0 and SSB should be aligned (assuming synch/channel raster design does not impose any restriction against such a design). This facilitates allocating larger number of contiguous RBs on top or bottom of SSB for PDSCH associated with Type0-PDCCH. |

#### <Summary of 1st Round of Discussions>

[TBD]

### 2.14 ANR/CGI Reporting Aspects

* From [3] Spreadtrum:
  + The mechanism of two offsets in MIB defined for NR-U, i.e. Alt 2), can be reused for UE to determine CORESET#0/Type0-PDCCH.
* From [7] OPPO:
  + For ANR design, RAN1 considers one of the two options
    - Option 1: RAN1 holds ANR discussion until RAN4 concludes the channelization, LBT bandwidth and sync raster relationship.
    - Option 2: RAN1 does not follow R16 baseline solution and redesign ANR.
* From [9] CATT:
  + There is no need to study additional method(s) to enable support to obtain neighbor cell SIB1 contents related to CGI reporting in Rel-17.
* From [13] Samsung:
  + No need to support extra method for providing the CORESET#0/Type0-PDCCH configuration for ANR purpose.
* From [26] Qualcomm:
  + for ANR, do not consider additional methods (compared to current NR) to signal the NCGI

#### Summary of Discussions

3 Companies expressed that there is no need to consider additional methods to support neighbor cell SIB1 reading. 2 Companies mentioned the possibility of supporting offset based neighbor cell CORESET#0 determination, similar to what was defined for Rel-16 NR-U.

#### <Moderator’s Suggestion for Discussions>

From moderator’s understanding whether offset based neighbor cell determination is possible may depend on raster design in RAN4. Therefore, based on limited discussion from companies, and potential dependency on RAN4 decision, moderator suggest de-prioritize discussion in this meeting.

#### 1st Round of Discussions

Please provide further comments on moderator’s suggestion above. If there are any other issues that require discussion on ANR and CGI reporting, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| OPPO | As discussed in our contribution, ANR issue should be revisited after RAN4 concludes the channelization, LBT bandwidth and sync raster relationship. |
| LG Electronics | We agree with the Moderator’s suggestion, we can deprioritize the discussion on ANR issue in this meeting. |
| Ericsson | We agree that there is no need to support extra method for providing the CORESET#0/Type0-PDCCH configuration for ANR purpose.  Regarding the Rel-16 mechanism introcued for NR-U we don't think it will work for the 57 – 71 GHz band. However, we can reassess when more details are known on the channelization design. |
| Intel | Agree with Moderator’s suggestion. |
| vivo | Agree with the moderator’s suggestion. |

#### <Summary of 1st Round of Discussions>

[TBD]

### 2.1.5 Various other aspects on SSB Design

* From [3] Spreadtrum:
  + SSB with 240kHz SCS can be down-prioritized.
  + Supporting initial cell selection with 480kHz SSB should be an optional UE capability separately from supporting other processing with 480/960kHz SCS.
  + The SSB-based TRS/CSI-RS validation can be supported.
* From [7] OPPO:
  + The raster step size for 120kHz and 480kHz are 3\*17.28MHz and 15\*17.28MHz, respectively, leading to a total number of raster entries 428.
* From [9] CATT:
  + Symbol #6 and symbol #13 can be reserved for beam switching. Neither PDCCH nor PDSCH can be transmitted on the reserved symbols.
  + The default TDRA table for pattern 1 in TS 38.214 can be enhanced, e,g at least {S=6 ,L=7}, {S=2，L=11} is supported.
* From [12] Nokia, NSB:
  + It is possible to apply SCSe to one part of actually transmitted SSBs and LBT procedure for other/rest of the SSBs.
  + Consider semi-static or predetermined mechanism to determine which SSBs are under SCSe and which under LBT in certain time windows.
* From [13] Samsung:
  + RAN1 clarifies that the configurable SCS for initial BWP configured by SIB1 can be 120 kHz, 480 kHz, and 960 kHz.
  + For 480 and 960 kHz, support the following 4 configurations for NR carrier RSSI measurement:
    - Configuration #0: {0, 1};
    - Configuration #1: {0, 1, …, 5};
    - Configuration #2: {0, 1, …, 8};
    - Configuration #3: {0, 1, …, 12}.



* From [20] Lenovo, Motorola Mobility:
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, with higher subcarrier spacings (numerologies), coverage enhancement of channels and signals used for initial access should be considered for NR beyond 52.6 GHz
  + For initial access in NR unlicensed bands between 52.6 GHz and 71 GHz, with directional LBT based channel access mechanism, indication of sensing beams can be considered during the initial access
* From [25] Convida Wireless:
  + SSB coverage enhancement should be studied for higher SCS.

#### Summary of Discussions

* Companies have provided the following issues
  + Raster design
  + Capability aspect for initial access
  + Support of SSB based TRS/CSI-RS validiation
  + TDRA table update
  + Short control signal exemption applicability to signals
  + RSSI symbol update due to new SSB design
  + Coverage enhancement
  + Sensing beam indication

#### <Moderator’s Suggestion for Discussions>

For the following issues, moderator has provided comments on whether to further discuss during this meeting.

* Raster design
  + Should be discussed in RAN4
* Capability aspect for initial access
  + Should be discussed in 8.17.2
* Support of SSB based TRS/CSI-RS validiation
  + Moderator asks the proponent company to provide further information on what needs to be considered and specified in RAN1.
* TDRA table update
  + Moderator suggest to discuss further this meeting
* Short control signal exemption applicability to signals
  + Should be discussed in 8.2.6 channel access agenda
* RSSI symbol update due to new SSB design
  + Moderator suggest to discuss further this meeting
* Coverage enhancement
  + Moderator suggest to de-prioritize this discussion as coverage enhancement was explicitly de-scoped from the WID
* Sensing beam indication
  + Moderator thinks 8.2.6 channel access agenda might be a better suited agenda for discussion

Further discuss on the following proposals.

**Issue #1)** TDRA table update

Currently, Type0-PDCCH uses default TDRA A and C for CORESET multiplexing pattern 1 and 3, respectively. Please provide further comments on whether TDRA table should be updated and if so how it should be updated.

**Issue #2)** RSSI symbol update due to new SSB design for 480 and 960 kHz

##### Proposal 1.5-1

* For 480 and 960 kHz, support the following 4 configurations for NR carrier RSSI measurement:
  + Configuration #0: {0, 1};
  + Configuration #1: {0, 1, …, 5};
  + Configuration #2: {0, 1, …, 8};
  + Configuration #3: {0, 1, …, 12}.



#### 1st Round of Discussions

Please provide further comments on the above issue #1 and #2. If there are any other issues that require discussion, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | Issue #1: For TDRA C, since the SSBs start on symbols 2 and 9, for CORESET0 of 2 symbols, we may need to account for TDRA C “S = 11” and “L = 2” values. |
| Samsung | Issue #1:   * If pattern 3 is supported for 480/960 kHz, there is expected enhancement to the TDRA C table due to different SSB locations in a slot. * For TDRA A table, we are open to the discussion on enhancement if there is a need.   Issue #2: we support Proposal 1.5-1 as the proposing company. |
| LG Electronics | Issue #1: We agree with Qualcomm and Samsung that adjustment of TDRA C can be considered to be aligned with new SSB symbol-level pattern for 480/960 kHz.  Issue #2: We do not support Proposal 1.5-1. In NR-U/LAA, the symbol location to measure RSSI irrespective of synchronization signals. To be specific, the measurement duration can be configured among 1/14/28/42/70 symbols and those values can be reused also for FR2-2. Anyway, the relevant discussion can be discussed under 8.2.6. |
| Ericsson | Issue #1  We don't think we should spend time on optimizing the TDRA table – this was a very long discussion in Rel-16.  Issue #2  We don't see the need for optimizations of RSSI measurement configuration for the 57 – 71 GHz band. |
| Intel | We are fine with Proposal 1.5-1 |

#### <Summary of 1st Round of Discussions>

[TBD]

## 2.2 PRACH Aspects

### 2.2.1 PRACH Sequence and Format

* From [1] Huawei/HiSilicon:
  + Additionally support L=571 for 480 kHz PRACH.
* From [2] Futurewei:
  + Do not support PRACH length L=571 for 480kHz PRACH.
* From [4] ZTE, Sanechips:
  + Support sequence length 571 for 480KHz PRACH SCS for 52.6 to 71 GHz.
* From [5] vivo:
  + Support 120KHz and 480KHz as candidate SCS of initial UL BWP.
  + Support 480KHz and 960KHz SCS in addition to 120KHz SCS for PRACH.
* From [11] Ericsson:
  + We are open to further discuss whether or not L = 571 is supported for 480 kHz.
* From [12] Nokia, NSB:
  + Support L=571 for PRACH with 480kHz.
* From [13] Mediatek:
  + Support only sequence length L=139 when PRACH SCS=480 kHz.
* From [15] Intel:
  + Support PRACH formats A1~A3, B1~B4, C0, C2 for with SCS 480 kHz, i.e., .
* From [22] LG Electronics:
  + The 120 kHz PRACH SCS with sequence lengths L=571 and L=1151 are not required for the licensed spectrum where the regulatory requirements are not defined on PSD limit.
  + PRACH with sequence length L=571 can be supported for the 480 kHz SCS in addition to L=139 for initial/non-initial access and 960 kHz SCS PRACH with L=139 is only supported for non-initial access.
* From [23] Sharp:
  + Only support L = 139 for PRACH with 480kHz and 960 kHz SSB SCS.
* From [24] Apple:
  + Support PRACH length L=571 for 480 kHz PRACH.

#### Summary of Discussions

The following are previous agreements on PRACH sequence and formats.

|  |
| --- |
| **Agreement:**   * For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2. * For non-initial access use cases,   + if 480kHz and/or 960 kHz SSB SCS is agreed to be supported, support 480 and/or 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.     - FFS: support of sequence length L = 571, 1151 * FFS: Support of 480 and/or 960 kHz PRACH SCS for initial access use cases, if 480 and/or 960 kHz SSB SCS is agreed to be supported for initial access   Agreement:  Do not support PRACH length L=571, 1151 for 960kHz PRACH and at least L =1151 for 480kHz PRACH. |

* Supported sequence lengths
  + PRACH length L=571 for 480kHz
    - Support: Huawei/HiSilicon, ZTE/Sanechips, Nokia/NSB, Intel, LGE, Apple, Sharp
    - Do not support: Futurewei
* Supported subcarrier spacing for initial UL BWP
  + 120 kHz, 480 kHz: vivo

#### <Moderator’s Suggestion for Discussions>

Further discussion on following proposals.

##### Proposal 2.1-1

* Additionally support PRACH length L=571 for 480kHz

##### Proposal 2.1-2

* Support 120 kHz and 480 kHz subcarrier spacing for initial UL BWP

#### 1st Round of Discussions

Please provide further comments on the above issues (Proposal 2.1-1 and 2.1-2). Also, if there are any other issues that require discussion on PRACH sequences and formats, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | We support both Proposal 2.1-1 and Proposal 2.1-2.  Meanwhile, we would like to clarify whether proposal 2.1-2 means that 960 kHz subcarrier spacing is not supported for initial UL BWP. |
| NTT DOCOMO | We are fine with both proposals, 2.1-1 and 2.1-2. |
| OPPO | Proposal 2.1-1: not support.  Proposal 2.1-2: support. |
| Qualcomm | Proposal 2.1-2: support |
| Lenovo, Motorola Mobility | Proposal 2.1-1: support.  Proposal 2.1-2: support. |
| Interdigital | **Proposal 2.1-1**: Support the proposal.  **Proposal 2.1-2**: Support the proposal. |
| Ericsson | Proposal 2.1-1: We don't think this is strictly needed, but we okay to support it if the majority wants it.  Proposal 2.1-2: An initial UL BWP is configured on an SCell too (according to 38.331), so is 960 kHz SCS precluded on an SCell? Perhaps it should be clarified that the proposal is for PCell. |
| ETRI | We support both Proposal 2.1-1 and Proposal 2.1-2.  We also agree with LG’s comment regarding whether to support 960kHz for initial UL BWP. |
| Sharp | We are fine with both proposals. |
| Intel | Proposal 2.1-1: Support.  Proposal 2.1-2: Support.  As mentioned numerous times, our motivation for supporting Proposal 2.1-1 is to achieve at least 100 MHz for PRACH such that no transmission power penalty is applied by US regulations. |
| vivo | **Proposal 2.1-1**: Support.  **Proposal 2.1-2**: Support. |
| Huawei, HiSilicon | Proposal 2.1-1: Support  Proposal 2.1-2: Support |

#### <Summary of 1st Round of Discussions>

[TBD]

### 2.2.2 RACH Occasion Resources

* From [1] Huawei/HiSilicon:
  + For 480 kHz and 960 kHz PRACH, support one gap symbol between consecutive ROs in time domain at least for Formats A1, B1, and A1/B1.
  + For PRACH format A1, B1 and A1/B1, the first symbols for each RO in a reference slot can be derived using equation (2) if a gap symbol between consecutive ROs is introduced. The same triples of in Table 6.3.3.2-4 of 38.211 are reused.
    - Note: Equation (2) guarantees that no RO straddles between slots and .

(2)

* From [2] Futurewei:
  + If when the LBT is required prior to RACH transmissions there is no necessary to add extra gaps between successive RO in the same PRACH slot.
  + For 480kHz and 960 kHz SCS reuse Table 6.3.3.2-4: Random access configurations for FR2 and unpaired spectrum, where the slot index is scaled up by 4 and respectively by 8 as per prior agreement. For 120 kHz SCS use the Table 6.3.3.2-4 as is.
  + Update the table 8.1-2 to indicate the necessary Ngap for higher SCS.
* From [4] ZTE, Sanechips:
  + For 480kHz and 960kHz, it is unnecessary to introduce gap between ROs for LBT and/or beam switching.
  + For 480kHz and 960kHz, it is unnecessary to allow for additional values if the maximum that can be configured for the number of FD ROs is less than 8.
* From [5] vivo:
  + The gaps between the consecutive ROs should be supported for LBT and/or beam switching.
  + The ROs for a given PRACH configuration spanned more than one PRACH slot should not be supported.
* From [6] Fujitsu:
  + Gaps between time-domain ROs in a slot are needed not only for LBT/beam switching, but also to avoid strong inter-RO interference due to power ramping up and rolling down.
  + For FR2-2, support gaps between time-domain ROs in a slot. The gaps can be enabled and configured by RRC signaling.
* From [9] CATT:
  + The reference slot duration corresponds to 60 kHz SCS. PRACH slot index corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
  + For 480/960 kHz PRACH slots configuration, higher PRACH slot density or higher RO density in time domain can be supported to compensate the impact from MSGS –FDM decreasing and LBT/beam switching GAP.
    - For 480KHz SCS, PRACH slot density can be 2 or 4 times comparing to than 120KHz SCS
    - For 960KHz SCS, PRACH slot density can be 4 times comparing to 120KHz SCS
  + If gap for LBT or beam switching is needed before UE transmit a msg-1, one RO can be disabled by RRC in a 60 KHz reference slot, and UE can perform LBT or beam switching on the disable RO.
* From [10] Xiaomi:
  + Inconsecutive RO time domain configuration should be supported at least for 480 and 960 kHz case.
* From [11] Ericsson:
  + Do not support additional values if the maximum number of configured FD ROs is less than 8.
  + Do not specify gaps between consecutive PRACH occasions. If needed, gaps to account for gNB receive beam switching time can be created purely by gNB implementation based on the gNB's own knowledge of the switching time.
  + There is no need to further consider additional values for the case when a PRACH slot cannot contain all time domain PRACH occasions
  + Support the following values of
    - When number of PRACH slots in a reference slot is 1,
      * for 480kHz and for 960kHz PRACH
    - When the number of PRACH slots in a reference slot is 2,
      * for 480kHz and for 960kHz PRACH
* From [12] Nokia, NSB:
  + Do not introduce LBT gap between consecutive ROs.
  + Re-use the FR2-1 PRACH configuration for 120kHz sub-carrier spacing.
* From [13] Samsung:
  + Support non-consecutive RO configuration to alleviate the RACH LBT failure.
  + Postpone the decision of additional values until the gap generation method has been determined.
* From [14] Mediatek:
  + RAN 1 to discuss the value of for NR operation to 52.6-71 GHz.
* From [15] Intel:
  + If gaps between consecutive ROs are necessary, gNB is able to configure PRACH with a large number of repetitions where some extra repetitions may be skipped and, thus, serve as gaps between ROs.
* From [16] NTT Docomo:
  + For RO configuration for PRACH with 480/960 kHz SCS, no need to consider either LBT or beam switching gap for RO design in 52.6 – 71 GHz
* From [21] Interdigital:
  + Do not support gap insertion between consecutive ROs in time domain as it causes inefficiency and application ambiguity.
  + Consider the enhancements to RO configuration without inserting gaps in between consecutive ROs.
  + For 52.6 – 71 GHz with 120kHz, 480kHz, and 960kHz PRACH, inserting gaps to achieve non-consecutive RACH occasions is not supported.
  + For 52.6 – 71 GHz, support sharing and extending the COT for LBT-free PRACH transmission in the consecutive ROs.
* From [22] LG Electronics:
  + When LBT is used to transmit the PRACH preamble, consider to insert CCA gap between adjacent RACH occasions in time domain (e.g. X usec or Y symbol) to avoid inter-UE LBT blocking due to the propagation delay of PRACH transmitted in an earlier RO.
  + The starting PRACH slot index for 480/960 kHz is given by:
    - when the number of PRACH slots in a reference slot is 1,
      * for 480 kHz and for 960 kHz PRACH
    - when the number of PRACH slots in a reference slot is 2,
      * for 480 kHz and for 960 kHz PRACH
    - where X is the number of additional slots to provide a gap between all of consecutive RACH occasions corresponding to a PRACH configuration index in Table 6.3.3.2-4 of TS 38.211, based on the configured number of symbols for the gap required for LBT and/or beam switching.
      * Note: If a PRACH slot cannot contain all time domain PRACH occasions corresponding to a PRACH configuration index in Table 6.3.3.2-4 of TS 38.211 including gap(s) between consecutive PRACH occasions to account for LBT and/or beam switching, then X=0.
* From [23] Sharp:
  + Gaps between consecutive ROs should be supported at least for LBT purposes.
  + A starting symbol index of a PRACH occasion is given by If non-zero duration gaps are configured between consecutive ROs and the ROs would span multiple PRACH slots, for 480 and 960 kHz SCS, respectively. Otherwise, for 480 and 960 kHz SCS, respectively.
* From [24] Apple:
  + Maximum 4 PRACH ROs can be configured for 120kHz SCS with .
  + Maximum 2 PRACH ROs can be configured for 120kHz SCS with .
  + If a gap between consecutive PRACH occasions is not configured or not supported,
    - When number of PRACH slots in a reference slot is 1, for 480kHz and for 960kHz PRACH.
    - When number of PRACH slots in a reference slot is 2, for 480kHz and for 960kHz PRACH.
  + Pending confirmation from RAN4 on 59ns beam switching time, a SIB1-configurable gap between time-domain ROs cand be considered.
  + Keep the same values if the maximum that can be configured for the number of FD RO’s is less than 8
* From [26] Qualcomm:
  + a maximum of 4 and 2 FD multiplexed ROs for SCS = 120 kHz and sequence length = 571 and 1151, respectively
  + for SCS = 120 kHz, if the maximum number of FD ROs are reduced, consider ways to increase the TD ROs (to maintain the same capacity) with minimal specification impact
  + for higher RACH SCS (480 and 960 kHz), consider including a gap between ROs which can be symbol-level (for gNB beam switching delay) or RO-level (for LBT)
  + for 480 kHz and 960 kHz PRACH:
    - ROs for a given PRACH configuration may need extra PRACH slot if gaps between consecutive ROs are supported for LBT and/or beam switching purposes
      * Option A: TDM "RO + gap" until all required number of ROs are satisfied (even if they extend to an extra slot)
      * Option B: split the number of ROs as evenly as possible among multiple slots such that the pattern is the same for all slots (distribute the "RO + gap" among slots)
    - For the extra slots (if needed) consider the following 2 alternatives:
      * Alt1: the extra slots are added such that the distribution of the slots is even within the RACH reference slot
      * Alt2: the extra slots are added next to the original slots

Table

Description automatically generated

#### Summary of Discussions

The following are previous agreements on PRACH sequence and formats.

|  |
| --- |
| Agreement:  For 480 and 960kHz PRACH:   * At least the same RO density in time domain (i.e. number of specified RO per reference slot according the PRACH configuration index) as for 120kHz PRACH in FR2 is supported   + FFS: Support gap between consecutive ROs in time domain and the details to derive the gap   Agreement:  For 480 and 960kHz PRACH,   * When a PRACH slot can contain all time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,   + and when number of PRACH slots in a reference slot is 1,     - for 480kHz and for 960kHz PRACH   + and when the number of PRACH slots in a reference slot is 2,     - for 480kHz and for 960kHz PRACH * FFS: values, when a PRACH slot cannot contain all time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching. * FFS: whether to allow for additional values if the maximum that can be configured for the number of FD RO’s is less than 8 (due to BW limitation) |

The following is a summary of company views.

* Gap between consecutive ROs
  + Support: Huawei/HiSilicon (only for Formats A1, B1, A1/B1), vivo, Fujitsu, [CATT], [Xiaomi], Samsung, LGE, Sharp, Qualcomm
  + Do not support: ZTE/Sanechips, [Futurewei], Ericsson, Intel, Nokia/NSB, NTT Docomo, Interdigital
* Do not support ROs that span more than one PRACH slot
  + vivo
* RO disabling RRC configuration to provide gap for LBT or beam switching
  + CATT
* Maximum 4 PRACH ROs can be configured for 120kHz SCS with . Maximum 2 PRACH ROs can be configured for 120kHz SCS with .
  + Apple, Qualcomm
* Do not support additional values if the maximum number of configured FD ROs is less than 8.
  + Ericsson, ZTE/Sanechips, Apple
* values
  + If number of PRACH slots per reference slot is 1,
    - Confirm WA, for 480kHz and for 960kHz PRACH
      * Ericsson, Apple
    - for 480 kHz and for 960 kHz PRACH
      * LGE
    - If gap between RO is configured, for 480kHz and for 960kHz PRACH
      * Sharp
  + If number of PRACH slots per reference slot is 2,
    - Confirm WA, for 480kHz and for 960kHz PRACH
      * Ericsson, Apple
    - for 480 kHz and for 960 kHz PRACH
      * LGE

#### <Moderator’s Suggestion for Discussions>

Whether or not gap is supported between consecutive RO is the most controversial and critical issue that seems to impact other discussion for RO design. Suggest discussing and conclude on this aspect first. Please further discuss on the following proposal.

##### Proposal 2.1-1 – alternative to 2.1-2

* Support gap between consecutive ROs for 480kHz and 960kHz
  + FFS: whether supporting gaps is fixed in specification or RRC configured by gNB

##### Proposal 2.1-2 – alternative to 2.1-1

* Do not support gap between consecutive ROs for 480kHz and 960kHz

#### 1st Round of Discussions

Please provide further comments on the above issues (Proposal 2.1-1 or 2.1-2). Also, if there are any other issues that require discussion on PRACH ROs, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | We support Proposal 2.1-1 and the LBT gap is needed between the consecutive ROs to avoid inter-UE LBT blocking due to the propagation delay of PRACH transmitted in an earlier RO. The supporting gaps can be RRC configured by gNB since the required gap length may vary depending on whether the gap between ROs is for beam switching or LBT, and two or more 480/960 kHz PRACH slots may be required to maintain the same RO density for the gap for LBT. |
| NTT DOCOMO | As captured by FL, we support Proposal 2.1-2. We still think the necessity of gap between Ros would be questionable. |
| OPPO | We support gap between consecutive ROs for 480kHz and 960kHz. |
| Qualcomm | We support Proposal 2.1-1 |
| Lenovo, Motorola Mobility | We support Proposal 2.1-1. |
| Interdigital | **Proposal 2.1-2**: Support the proposal. As such, no gap is required between consecutive ROs. |
| Ericsson | Proposal 2.1-1: **We do not support gaps between consecutive ROs**.  For LBT, this was not needed in Rel-16, and it is even less motivated in the 57 – 71 GHz band where potential LBT blocking would be a virtually non-existent event considering that extensive system simulations have shown that LBT failure is rare. Moreover, in most regions LBT is not neede for PRACH.  For gNB Rx beam switching, if the gNB wants to create a gap due to it's own (known) beam switch time it can do so purely by gNB implementation as we discuss in our contribution. The gNB can simply drop several samples at the beginning of the PRACH reception during the time that it switches its beam.  Proposal 2.1-2. We support. |
| ETRI | We support Proposal 2.1-1. |
| Sharp | We support Proposal 2.1-1. |
| Intel | Proposal 2.1-1: Do not support  Proposal 2.1-2: Support  In both proposals there is no differentiation between types of the gaps. Therefore, we assume that both LBT and beam switching gaps are discussed.  We don’t see strong need in LBT gaps in PRACH as UE chooses one RO for RACH preamble transmission.  The beam switching gaps may be needed. However, it happens that gNB is able to configure a RACH preamble format with a large number of repetitions and use some of the extra repetitions for beam switching. This would effectively serve as a gap. |
| vivo | We support Proposal 2.1-1 to have LBT gap to avoid inter-UE blocking as mentioned by LG. |
| Huawei, HiSilicon | We think gap is required to accommodate beam switching latency especially for PRACH formats with smaller CP, that is A1, B1, A1/B1. We support Proposal 2.1-1 with the following modification: Proposal 2.1-1 – alternative to 2.1-2 (Modified)  * Support gap for between consecutive ROs for 480kHz and 960kHz   + FFS: whether supporting gaps is fixed in specification or RRC configured by gNB   + FFS: Whether gaps are supported for all PRACH formats or only for formats with smaller CP (eg, A1, B1, A1/B1) |

#### <Summary of 1st Round of Discussions>

[TBD]

### 2.2.3 RAR Window & RA Preamble ID

* From [1] Huawei/HiSilicon:
  + For the same RO density per reference slot as 120 KHz PRACH, the RA-RNTI corresponding to 480 kHz and 960 kHz ROs can be generated according to equation (5) by compressing the t\_id to .
    - When some ROs are backward shifted to the immediately preceding slot of the specified slot due to the use of a gap symbol between consecutive ROs, support a 1 bit indication field in the DCI scheduling RAR/MsgB to resolve the PRACH slot ambiguity.
    - RA-RNTI = 1+s\_id+14×floor(t\_id⁄2^(μ-3) )+14×80×f\_id+14×80×8×ul\_carrier\_id (5)
  + Support maximum of 40 ms for ra-ResponseWindow for operation with shared spectrum and msgB-ResponseWindow for both operations with and without shared spectrum. Support indicating two LSBs of SFN at which gNB has received msg1 (MsgA) in DCI format 1\_0 with CRC scrambled by RA-RNTI (MsgB-RNTI).
* From [2] Futurewei:
  + For 480kHz and 960kHz use the following formula for RA-RNTI
    - RA-RNTI = 1 + s\_id + 14 × t\_id + 14 × 160 × f\_Id + 14 × 160 × 8 × ul\_carrier\_Id
    - and divide the RAR window in N segments where each segment is 160 slots, and signal the segment index in the DCI that schedules the MSG2/B.
* From [4] ZTE, Sanechips:
  + For higher PRACH SCS (480 and/or 960 kHz), consider the following options for further down-selection of RA-RNTI enhancements: option 2, 3, or 7
* From [5] vivo:
  + For larger PRACH SCS (480KHz/960KHz), the following options can be considered for RA-RNTI calculation:
    - Alt.1: Modify the RA-RNTI formula as following and introduce some contention resolution mechanism to resolve the conflict.
    - RA-RNTI = (1+s\_id+14×t\_id+14×X×f\_id +14×X×8×ul\_carrier\_id) mod A
    - Alt.2: Reuse the current RA-RNTI formula while introducing additional indicator field to indicate the time-frequency resource together with RA-RNTI.
    - Alt.3: Depending on the RO configuration pattern, reuse/modify the RA-RNTI formula and express the slot indexes t\_id based on a new specific subcarrier spacing.
* From [6] Fujitsu:
  + When calculating RA-RNTI for 480kHz and 960kHz PRACH, the following should be considered to uniquely identify a RO:
    - t\_id is determined in a way that more than one slot can have the same t\_id; and
    - DCI scheduling RAR indicates the local index among the slots having the same t\_id.
* From [9] CATT:
  + For supporting Msg1 transmission with 480 KHz/960 KHz SCS, RA-RNTI is divided into two parts. One part of RA-RNTI is carried by DCI, and the remaining 16-bit of RA-RNTI could be used to scramble CRC of the DCI1. Two possible options are:
    - Option A:
      * RA-RNTI = (1 + s\_id + 14 × t\_id + 14 ×× f\_id + 14 × × 8 × ul\_carrier\_id) mod
      * inDCI\_bit = floor ((1 + s\_id + 14 × t\_id + 14 ×× f\_id + 14 × × 8 × ul\_carrier\_id) /)
      * s\_id is the index of the first OFDM symbol of the PRACH occasion (0 ≤ s\_id < 14)
      * t\_id is the index of the first slot of the PRACH occasion in a system frame (0 ≤ t\_id < 640)
    - Option B:
      * RA-RNTI = 1 + s\_id + 14 ×(t\_id mod 80) + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id
      * inDCI\_bit =
      * s\_id is the index of the first OFDM symbol of the PRACH occasion (0 ≤ s\_id < 14)
      * t\_id is the index of the first slot of the PRACH occasion in a system frame (0 ≤ t\_id < 640)
* From [10] Xiaomi:
  + Confirm the working assumption that for 120 kHz SSB, the number of candidates SSBs in a half frame is 64.
  + For 480/960 kHz SSB, candidates SSB index can be up to 128.
  + Whether DBTW or Q is needed can be decoded together with Q value.
* From [11] Ericsson:
  + For 480/960 kHz PRACH, reuse the RA-RNTI expressions from Rel-15/16, with the additional statement that for 480/960 kHz PRACH, t\_id should be determined based on a subcarrier spacing of 120 kHz.
  + Postpone further discussions of RA-RNTI design until the PRACH configuration design is completed.
* From [12] Nokia, NSB:
  + Reuse RA-RNTI formula defined for 120 kHz SCS also for the cases PRACH is configured with 480 or 960 kHz SCS where
    - assumes 480/960 kHz SCS
    - assumes 120 kHz SCS
* From [15] Intel:
  + RA-RNTI computation equation should be adjusted to avoid overflow in case of PRACH SCS 480 kHz and 960 kHz;
    - Support the following modified equation for RA-RNTI computation:
      * ,
      * where t\_id is based on the value of specified in clause 5.3.2 of TS 38.211.
* From [19] ETRI:
  + Propose to reuse the current equation with minor modifications for RA preamble ID calculation.
    - RA-RNTI = 1 + s\_id + 14 × t\_id + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id
      * *t\_id is the index of 120kHz slot that contains RO in a system frame*
      * s\_id is the index of the first OFDM symbol of RO based on the value of specified in clause 5.3.2 of TS 38.211
      * If additional PRACH slots are configured, the index(s) of the first OFDM symbol of ROs may be configure not to overlap each other between two PRACH slots within a 120kHz slot.
* From [22] LG Electronics:
  + Since the same RO density in time domain as for 120 kHz PRACH in FR2 is maintained regardless of whether there is a gap between ROs, RA-RNTI/MSGB-RNTI associated with the PRACH occasion for 480 and 960 kHz SCS using the existing RA-RNTI equation, the following options can be considered:
    - In the case of mapping RA-RNTI to hypothetical 480/960 kHz PRACH slot assuming that the gap between RACH occasions is zero,
      * Option 1: Reuse the existing RA-RNTI/MSGB-RNTI equation by reinterpreting the slot indexes t\_id based on a new specific subcarrier spacing as the slot indexes of 120 kHz SCS (e.g., floor(t\_id/n) where n=4 for 480 kHz SCS and n=8 for 960 kHz).
    - In the case of mapping RA-RNTI to actual 480/960 kHz PRACH slot,
      * Option 2: Divide the RAR window for RA-RNTI (or msg2 window for MSGB-RNTI) into N sub-periods (where each sub-period is 80 slots using the used SCS) + signal the sub-period index using the DCI that schedules the MSG2/MSGB.
* From [23] Sharp:
  + Assuming RO density per reference slot is unchanged, without modifying the formula and definition of s\_id. Modify the definition of t\_id as the slot index referring to 120kHz SCS.
* From [24] Apple:
  + modifying the existing calculation equation or redefine t\_id based on 120kHz SCS to solve the RA-RNTI overflowing problem:
* From [26] Qualcomm:
  + for higher RACH SCS (480 and 960 kHz), consider the following options for the RA-RNTI:
    - Case 1: no extra RACH slots needed/configured
      * Same RA-RNTI equation as Rel-15/16
      * t\_id is the index of the first slot (based on 120 kHz numerology) of the PRACH occasion in a system frame (0 ≤ t\_id < 80)
    - Case 2: extra RACH slots needed/configured (but with the same number of ROs per reference slot)
      * Same RA-RNTI equation as Rel-15/16
      * s\_id is the index of the first OFDM symbol of the PRACH occasion within the one or more slots spanned by the ROs excluding any gaps (0 ≤ s\_id < 14)
      * t\_id is the index of the first slot (based on 120 kHz numerology) of the PRACH occasion in a system frame (0 ≤ t\_id < 80)
    - Case 3: extra RACH slots needed/configured (with more number of ROs per reference slot)
      * Option A: Extend s\_id to more than 14:
        + RA-RNTI = (1 + s\_id + S × t\_id + S × 80 × f\_id + S × 80 × 8 × ul\_carrier\_id) mod 216
        + s\_id is the index of the first OFDM symbol of the PRACH occasion within the one or more slots spanned by the ROs excluding any gaps (0 ≤ s\_id < S), S can take value > 14
        + t\_id is the index of the first slot (based on 120 kHz numerology) of the PRACH occasion in a system frame (0 ≤ t\_id < 80)
      * Option B:
        + Same RA-RNTI equation as Rel-15/16
        + t\_id is the index of the first slot (based on 120 kHz numerology) of the PRACH occasion in a system frame (0 ≤ t\_id < 80)
        + And signaling in the DL DCI that schedules the MSG2/MSGB the 480/960 kHz slot index within the 120 kHz slot

#### Summary of Discussions

The following list of options are from last meetings discussion.

|  |
| --- |
| * + **Plain Modulus Category**     - Option 1)   + **PRACH Sub-segmentation Method Category**     - Option 2)       * The same PRACH slot location in each 120kHz slot duration     - Option 3)       * Segment the PRACH into N segments       * is the index of the PRACH slot that contains the PRACH occasion in a segment.       * In DCI: RA-indication = Segment index     - Option 4)       * Segment the PRACH into N segments       * In DCI:     - Option 5)       * Segment the PRACH into N segments       * In DCI:     - Option 6)       * In DCI:   + **Compressing some indices Category (may require a matching RO configuration to work properly)**     - Option 7)       * is the index of the first 120kHz slot that contains the PRACH occasion in a system frame.       * is the index of the first OFDM symbol of the PRACH occasion based on the value of specified in clause 5.3.2 of TS 38.211.     - Option 8)       * RA-RNTI = 1 + s\_id + 14 × floor(t\_id / ) + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id,       * t\_id is based on the value of specified in clause 5.3.2 of TS 38.211. |

The following is summary of company views.

* Alt 1) Plain Modulus Category, some example in option 1
  + vivo
* Alt 2) PRACH Sub-segmentation Method Category, some examples in option 2 ~ 6
  + , Futurewei, ZTE/Sanechips, vivo, Fujitsu, CATT, LGE, Qualcomm
* Alt 3) Compressing some indices Category (may require a matching RO configuration to work properly), some examples in option 7 ~ 8
  + ZTE/Sanechips, Ericsson, Intel, vivo, Fujitsu, Nokia/NSB, ETRI, LGE, Sharp, Apple, Qualcomm, Huawei/HiSilicon

#### <Moderator’s Suggestion for Discussions>

RO design needs to be further progressed in order to assess which scheme is most suitable for fixing the RA-RNTI overflow issues. Suggest discussing this further once RO gap issue has been resolved and are determined.

#### 1st Round of Discussions

Please provide further comments on the moderator’s suggestion. Also, if there are any other issues that require discussion on RAR window and RA preamble ID, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | We are fine with Moderator’s Suggestion. However, we can consider the method of calculating RA-RNTI (regardless of configured RO gap) by mapping RA-RNTI to hypothetical 480/960 kHz PRACH slot assuming that the gap between RACH occasions is zero (corresponding to Option 1 in our contribution). |
| Ericsson | Fine with moderator's suggestion. |
| Intel | We are fine with Moderator’s suggestion. |
| vivo | Fine with moderator's suggestion. |

#### <Summary of 1st Round of Discussions>

[TBD]

### 2.2.4 Other aspects on PRACH

* From [2] Futurewei:
  + Support short control signaling LBT exception for RACH transmissions.

#### Summary of Discussions

One company provided inputs on applicability of short control signal exemption for PRACH transmission.

#### <Moderator’s Suggestion for Discussions>

Moderator suggest discussing short control signal exemption aspects under 8.2.6 channel access agenda.

#### 1st Round of Discussions

Please provide further comments on moderator’s suggestion above. Also, if there are any other issues that require discussion other aspects of PRACH, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| LG Electronics | We support the Moderator’s suggestion that discussing short control exemption aspects under 8.2.6. |
| Ericsson | SCS exemption has already been agreed in channel access AI. |
| Intel | This was agreed in RAN1#105-e:  Agreement:   * Contention Exempt Short Control Signaling rules apply to the transmission of msg1 for the 4 step RACH and MsgA for the 2-step RACH for all supported SCS.   + Note restriction for short control signalling transmissions apply (10% over any 100ms intervals)   + Alt 1: The 10% over any 100ms interval restriction is applicable to all available msg1/msgA resources configured (not limited to the resources actually used) in a cell   + Alt 2: The 10% over any 100ms interval restriction is applicable to the msg1/msgA transmission from one UE perspective * FFS: Other UL signals/channels can be transmitted with Contention Exempt Short Control Signaling rule, such as msg3, SRS, PUCCH, PUSCH without user plain data, etc |

#### <Summary of 1st Round of Discussions>

[TBD]

## 2.3 Others Aspects

* From [1] ZTE, Sanechips:
  + The existing parameter subCarrierSpacingCommon in MIB should be captured into Rel-17 RRC parameter table, as it will no longer be used to indicate the SCS of CORESET#0 in FR2-2.

#### Summary of Discussions

One company provided inputs on RRC parameters needed for initial access.

#### <Moderator’s Suggestion for Discussions>

Moderator suggest discussing the RRC parameters related issues under 8.2 RRC parameter discussion thread, “[106bis-e-R17-RRC-60GHz] Email discussion on Rel-17 RRC parameters for supporting NR from 52.6 GHz to 71 GHz – Jing (Qualcomm).”

#### 1st Round of Discussions

Please provide further comments on moderator’s suggestion above. Also, if there are any other issues that require discussion on issues not discussed in this summary document, please comment them here.

|  |  |
| --- | --- |
| Company | Comments |
| Ericsson | Agree to discuss in RRC thread |
| Intel | We agree with Moderator’s suggestion |

#### <Summary of 1st Round of Discussions>

[TBD]

# Reference

1. R1-2108767, “Initial access signals and channels for 52-71GHz spectrum,” Huawei, HiSilicon
2. R1-2108782, “Initial access for Beyond 52.6GHz,” FUTUREWEI
3. R1-2108902, “Discussion on initial access aspects for NR for 60GHz,” Spreadtrum Communications
4. R1-2108934, “Discussion on the initial access aspects for 52.6 to 71GHz,” ZTE, Sanechips
5. R1-2108959, “Discussions on initial access aspects for NR operation from 52.6GHz to 71GHz,” vivo
6. R1-2109032, “Considerations on initial access for NR from 52.6GHz to 71 GHz,” Fujitsu
7. R1-2109070, “Discusson on initial access aspects,” OPPO
8. R1-2109120, “Discussion on initial access aspects supporting NR from 52.6 to 71 GHz,” NEC
9. R1-2109208, “Initial access aspects for up to 71GHz operation,” CATT
10. R1-2109401, “On initial access aspects for NR from 52.6-71 GHz,” Xiaomi
11. R1-2109433, “Initial Access Aspects,” Ericsson
12. R1-2109442, “Initial access aspects,” Nokia, Nokia Shanghai Bell
13. R1-2109476, “Initial access aspects for NR from 52.6 GHz to 71 GHz,” Samsung
14. R1-2109557, “Remaining issues on initial access of 52.6-71 GHz NR operation,” MediaTek Inc.
15. R1-2109598, “Discussion on initial access aspects for extending NR up to 71 GHz,” Intel Corporation
16. R1-2109665, “Initial access aspects for NR from 52.6 to 71 GHz,” NTT DOCOMO, INC.
17. R1-2109741, “Initial access aspects for NR from 52.6 GHz to 71 GHz,” Panasonic Corporation
18. R1-2109777, “Considerations on initial access aspects for NR from 52.6 GHz to 71 GHz,” Sony
19. R1-2109808, “Discussion on initial access aspects for NR from 52.6 to 71GHz,” ETRI
20. R1-2109897, “Initial access aspects for NR from 52.6 GHz to 71GHz,” Lenovo, Motorola Mobility
21. R1-2109903, “Discussion on initial access channels and signals for operation in 52.6-71GHz,” InterDigital, Inc.
22. R1-2109961, “Initial access aspects to support NR above 52.6 GHz,” LG Electronics
23. R1-2109992, “Initial access aspects,” Sharp
24. R1-2110021, “Initial access signals and channels,” Apple
25. R1-2110109, “NR SSB design consideration for 52.6 GHz to 71 GHz,” Convida Wireless
26. R1-2110172, “Initial access aspects for NR in 52.6 to 71GHz band,” Qualcomm Incorporated
27. R1-2110320, “Discussion on initial access aspects for NR beyond 52.6GHz,” WILUS Inc.