**3GPP TSG RAN WG1 Meeting #105-e R1-2105978**

**e-Meeting, May 19 – 27, 2021**

**Source: Moderator (Intel Corporation)**

**Title: Summary #1 of email discussion on initial access aspects of NR extension up to 71 GHz**

**Agenda item: 8.2.1**

**Document for: Discussion**

# Introduction

This contribution summarizes discussions on initial access aspects of NR extension up to 71 GHz. The discussion of the initial access aspects has been approved for email discussion until May 27, 2021.

* [105-e-NR-52-71GHz-01] Email discussion/approval on initial access aspects with checkpoints for agreements on May-24, May-27 – Daewon (Intel)

# Summary of issues

## 2.1 SSB Aspects

### 2.1.1 Supported Numerology

* From [1] Futurewei:
  + Support no more than one additional SCS for CD-SSB. If an additional SCS is supported, the support should be mandatory for CD-SSB.
  + Support only the CD-SSB SCSs in for CORESET#0, SIB1, PRACH CBRA.
* From [2] Huawei, HiSilicon:
  + Following the agreement in RAN1 #104-e, no further discussion on supported SSB SCSs is required. Continue discussions on other aspects of initial access design based on the current agreements regarding the supported SSB SCSs.
* From [3] vivo:
  + Support 480/960 kHz SCS for both initial BWP and SSB
  + Support ALT1 and ALT4 as the solution for SSB and initial/non-initial BWP design, and prefer ALT4.
    - ALT 1)
      * Support SSB with 240/480/960 kHz for initial and non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB.
      * It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries in the 57 – 71 GHz band no larger than 400 (Note: the total number of synchronization raster entries in FR2 for band n259 is 344). If the assumption cannot be satisfied, it’s up to RAN4 to decide which of 240/480/960 kHz SCS are supported for initial access of such band.
      * RAN1 prioritizes time-domain multiplex of SSB and CORESET0 to minimize the number of needed synchronization raster entries.
      * Supporting 480 kHz SCS and 960 kHz SCS for SSB are UE capabilities:
        + UE is not expected to support 480 kHz SCS for SSB if it doesn’t support 480 kHz SCS for data/control channels.
        + UE is not expected to support 960 kHz SCS for SSB if it doesn’t support 960 kHz SCS for data/control channels.
      * Send an LS to RAN2 and RAN4.
    - ALT 4)
      * Support SSB with 240 and one of 480 or 960 kHz for initial and non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB.
        + [SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical]
        + [only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS]
      * It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries in the 57 – 71 GHz band no larger than 400 (Note: the total number of synchronization raster entries in FR2 for band n259 is 344). per band. If the assumption cannot be satisfied, it’s up to RAN4 to decide which of 240/480/960 kHz SCS are supported for initial access of such band.
      * RAN1 prioritizes time-domain multiplex of SSB and CORESET0 to minimize the number of needed synchronization raster entries.
      * Supporting 480 kHz SCS and 960 kHz SCS for SSB are UE capabilities:
        + UE is not expected to support 480 kHz SCS for SSB if it doesn’t support 480 kHz SCS for data/control channels.
        + UE is not expected to support 960 kHz SCS for SSB if it doesn’t support 960 kHz SCS for data/control channels.
* From [4] Spreadtrum:
  + SSB with 240kHz SCS can be down-prioritized.
  + SSB with 480/960kHz SCS can be supported for the case where SSB is configured with Type0-PDCCH.
  + SSB with 480/960kHz SCS can be supported for the case where SSB is used for initial cell selection, if the following conditions are satisfied:
    - The sync raster for 480/960kHz SSB is sparse enough;
    - Initial cell selection with 480/960kHz SSB is an optional UE capability, and to allow UE only supporting initial cell selection with 120kHz SSB to access a cell gNB should guarantee 120kHz SSB is deployed in the cell.
* From [5] Nokia, NSB:
  + Confirm that PSCell and SCell operation with 480kHz and 960kHz SSB is supported from RAN1 perspective.
  + Consider support for “initial access” (initial cell selection) for 480kHz and 960kHz kHz SCS SSB and mitigate the UE complexity via properly defining SS-raster.
  + Support 240 kHz SCS for the SSB transmission in NR bands ranging between 52.6 GHz to 71 GHz
* From [6] CATT:
  + Support of 480 KHz and/or 960 KHz SCS for initial access can be considered after RAN4’s confirmation for channelization design with acceptable synchronization raster entries.
* From [8] Qualcomm:
  + RAN1 can continue to discuss other options for the SSB SCS support, but prioritize design on the already agreed choices (120 kHz SCS for initial access and 480 kHz and 960 kHz for non-initial access case where SSB location and SCS are explicitly provided to the UE and SSB does not configure Type-0 PDCCH)
* From [9] OPPO:
  + For above 52.6GHz, adopt single numerology for initial access, where the numerology candidates are 120kHz, 480kHz and 960kHz.
  + For above 52.6GHz, 240kHz SSB SCS is not supported.
* From [10] ZTE, Sanechips:
  + SSB with 480/960kHz SCS should be supported in both initial and non-initial access cases.
* From [11] Intel:
  + Support 480 kHz and 960 kHz SCS for SSB for initial access cases.
    - Note: support of 480kHz and/or 960kHz SCS for SSB is optional.
* From [14] Sony:
  + 480 kHz and 960 kHz SCS for SSB for initial access should be supported for NR above 52.6 GHz.
    - If neither 480 kHz nor 960 kHz SCS is supported for SSB for initial access, 240 kHz SCS for SSB for initial access should be supported.
  + 480 kHz and 960 kHz SCS for initial access related signals and channels should be supported for NR above 52.6 GHz regardless of supporting SCS SSB.
* From [16] Samsung:
  + Support 480 kHz and 960 kHz SCS for SS/PBCH block in initial access case.
* From [18] LGE:
  + Support 240 kHz SCS for SS/PBCH block in frequency range from 52.6 GHz to 71 GHz.
  + At most one of 480 and 960 kHz SCSs can be additionally supported for SS/PBCH block with initial access.
* From [19] Lenovo, Motorola Mobility:
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, support the same numerologies of data channel for SSB including 480kHz and 960kHz for both initial access and non-initial access cases
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, if higher subcarrier spacings (numerologies) are adopted for initial access, coverage enhancement of channels and signals used for initial access should be considered for NR beyond 52.6 GHz.
* From [20] Xiaomi:
  + Beyond 120k Hz SCS, at least one of 240/480/960 kHz SCSs should be configured for cell defined SSB.
  + SSB and CORESET0 multiplexing configuration tables can be reused for 120kHz SCS SSB, but may need update if additional SCS for SSB is agreed for initial access.
* From [21] Interdigital:
  + Further study necessity of SSBs and initial access related signals/channels for additional SCSs in Rel-17.
* From [22] Convida:
  + The support of non-initial SSB design for higher SCS 480 KHz and 960 KHz can be based on Rel-15/16 SSB design as baseline to minimize the specification impact.
* From [23] NTT Docomo:
  + For SSB SCS, in addition to 120 kHz:
    - 480 and/or 960 kHz SCS should be supported for initial access case.
    - The support of 480 and/or 960 kHz SCS for SSB can be optional as well as for the other signals/channels.
  + For SCS used for CORESET#0 PDCCH and SIB1 PDSCH, in addition to 120 kHz:
    - Both 480 and 960 kHz SCS should be supported.

#### Summary of Discussions

* Various views on SSB SCS
  + No need to discuss further:
    - Huawei, HiSilicon
  + Support 240kHz SSB
    - LGE, Nokia, NSB,
  + No more than 1 additional SCS for cell defining SSB
    - Futurewei
  + Support at least one of 120, 480, or 960kHz SSB for initial access
    - Xiaomi
  + Support one of 480 and 960kHz SSB for initial access
    - Vivo, LGE
  + Support 480 and 960kHz SSB for initial access (with conditions: e.g. optional UE capability, sparse SS raster)
    - Spreadtrum, Nokia, NSB, CATT
  + Support 480 and 960kHz SSB for initial access
    - OPPO, ZTE, Sanechip, Intel, Sony, Samsung, Lenovo, Motorola Mobility, Docomo
  + Continue discussions
    - Qualcomm (prioritize current agreed choices in design), Interdigital
* Moderator suggestions:
  + any companies have discussed this issue, continue discussion over email along with other issues.
  + Given the limited TU and agreement from last RAN1 meeting, moderator suggests to only bring this issue up in GTW if there is close to consensus on a proposal.
    - Proposals described by vivo or Samsung might be good starting point for discussions.

#### **1st Round Discussion:**

Discussion on support of CORESET#0/Type0-PDCCH configuration in MIB can be discussed in Section 2.1.2 and 2.1.5. Please provide further comments on 240/480/960kHz SSB and clarification on optionality.

* Further discussion on 240/480/960kHz SSB
  + Alt 1) Supporting 240, 480, and 960 kHz SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
  + Alt 2) Supporting 240 kHz and one of 480 or 960 kHz SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
  + Alt 3) Supporting one of 240, 480, or 960 kHz SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
  + Alt 4) Supporting 480 and 960 kHz for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
  + Alt 5) Supporting one of 480 or 960 kHz SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
  + Alt 6) conclude no support of 240, 480, and 960kHz SSB for initial access.
  + Additional constraints:
    - Limited sync raster entry numbers (details can be sorted out if generally acceptable)
    - only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS
    - SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical
* Clarification on optionality of 480/960kHz SCS.
  + Supporting 480 kHz SCS and 960 kHz SCS for SSB are UE capabilities:
    - UE is not expected to support 480 kHz SCS for SSB if it doesn’t support 480 kHz SCS for data/control channels.
    - UE is not expected to support 960 kHz SCS for SSB if it doesn’t support 960 kHz SCS for data/control channels
  + Optionally Supporting 480/960kHz SSB is:
    - Alt A) same capability as supporting 480/960kHz SCS, respectively (e.g. single capability per SCS, UE indicates support of 480kHz SCS mean support 480kHz SSB and 480kHz data/control/RS)
    - Alt B-1) separate capability from supporting 480/960kHz SCS for data/control/RS, respectively, and same capability for supporting initial access (if this case is supported) & non-initial access (2 different capability for each SCS)
    - Alt B-2) separate capability from supporting 480/960kHz SCS for data/control/RS, respectively, and seperate capability for supporting initial access (if this case is supported) & non-initial access (3 different capability for each SCS)

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| **Company** | **Comment** |
| DOCOMO | For the 1st bullet, our best preference is Alt 1. Second preference is Alt 4 or Alt 5. Not prefer Alt 2 nor Alt 3, but we can live with them also if it gets clear majority. Not support Alt 6. For additional constraints, we are ok with the captured three sub-sub-bullets but it should depend on the exact alternative we will take in our view.  For the 2nd bullet, while we prefer to discuss about anything related to optionality, our preference is to associate it with the optionality on the support of 480/960k SCS for data/control, i.e. the 2nd sub-sub-bullet in the 1st sub-bullet and Alt A. |
| LG Electronics | Our first preference is to support 240 for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints. So, please add   * Alt 7) Supporting 240 for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints   As a compromise, we can accept Alt 2.  Regarding UE capabilities on 480/960 kHz SCS, we prefer Alt A. By the way, Alt B can be updated as follows.   * + - Alt B-1) separate capability from supporting 480/960kHz SCS for SSB and data/control/RS, respectively, and same capability for supporting initial access (if this case is supported) & non-initial access (2 different capability for each SCS)     - Alt B-2) separate capability from supporting 480/960kHz SCS for SSB and data/control/RS, respectively, and separate capability for supporting initial access (if this case is supported) & non-initial access (3 different capability for each SCS) |
| Samsung | Our first preference is Alt 5), and can compromise to Alt 1) or 4). 2) and 3) seem need to be modified, since we already agreed to support 480 and 960 for non-initial access case, and if our understanding is correct, the “one of 480 or 960” only applies to initial access case. With such clarification, we are also ok with Alt 2) as a compromise.  For the UE capability discussion, we already provide our understanding in the tdoc, and we are also with defining the same UE capability for SSB and data/control/RS for each SCS. |
| Huawei, HiSilicon | * Regarding discussion on 240/480/960kHz SSB:   + Alt 6): The reason to support 480 kHz or 960 kHz SSB SCS was to facilitate a single-numerology operation. However, this is already achievable under the current agreements (supporting 120 kHz SSB SCS for both initial access and non-initial access and supporting 480/960 kHz SSB SCS for non-initial access case with SSB not configuring Type-0 PDCCH) by means of having all initial access signals/channels in 120 kHz and, after RRC connection, entirely operating on a BWP with a configured 480 kHz or 960 kHz SCS if needed. Moreover, we have already agreed in RAN1 #104-e that ***“Whether or not to support 240 kHz, 480kHz and 960kHz SCS for SSB and the conditions under which SSB for 240 kHz, 480 kHz and 960 kHz may be supported will be decided no later than RAN1#104bis-e.”*** We do not see any reason to revert this agreement and continue discussion on supported SSB SCSs. * Regarding clarification on optionality of 480/960kHz SCS:   + The detail of the UE capability can be discussed at a later stage. Moreover, we do not think it is useful to discuss whether one UE capability bit or two different UE capability bits are required for the support of 480(960) kHz SSB for initial access and non-initial access case. Such a discussion is on a subject that has no urgency (UE capability bits) and, further, is speculative, as based on current agreements, 480(960) kHz SSB for initial access is not supported. If there is a need to make progress in this regard, we suggest to formally agree on the two sub-bullets of the first bullet which actually help us to in the UE capability discussion down the road:     - ***Proposal:***        * ***UE is not expected to support 480 kHz SCS for SSB if it doesn’t support 480 kHz SCS for data/control channels.***       * ***UE is not expected to support 960 kHz SCS for SSB if it doesn’t support 960 kHz SCS for data/control channels*** |
| Qualcomm | For the 1st bullet, Alt 6 can be considered as the default/baseline assumption based on the agreement we had so far (in RAN1#104-e and RAN#104bis-e), namely: “*Whether or not to support 240 kHz, 480kHz and 960kHz SCS for SSB and the conditions under which SSB for 240 kHz, 480 kHz and 960 kHz may be supported will be decided no later than RAN1#104bis-e.”*  However, if further discussions are needed, we support Alt 7 (as proposed by LG with a small modification), namely: *Supporting 240 kHz SCS SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB ~~with constraints~~*. For the reasons mentioned our paper, we prefer not to support 480/960 kHz for initial access.  For non-initial access (*with support of CORESET0/Type0-PDCCH configuration in the MIB*), we can support 480/960 kHz SCS only if the timing of the SSB is known to the UE:  Alt 8): Supporting 480 and 960 kHz SSB for non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB if the timing of the SSB is known to the UE.  For the 2nd bullet, we support Alt A. |
| Mediatek | Alt 6 is the preferred option. We share similar with Huawei that based on current agreement, single numerology operation can be obtained. Besides, the significance of 480/960 kHz SCS for ANR purpose is not clear to us, since by using 120 kHz SCS, the CGI information can be provided to UE. It would be very much appreciated if it can be further clarified. |
| ZTE, Sanechips | Alt 4 is our first preference. But as a compromise, Alt 1, 2 and 5 can also be accepted for us.  From the perspective of future evolution, SSB supporting SCS 480/960 kHz may help 5G NR to have a unified design to support even higher frequency band in the future, such as above 71 GHz. We should allow some enhancements in this WI to make the system more efficient. The additional standardization impact of supporting SSB SCS 480/960 kHz in initial access case is relatively small, since we have already agreed to support two SCSs in non-initial access.  For the discussion on optionality, the first bullet and corresponding sub-bullets are fine to us. As for the 2nd bullet, we support Alt A. |
| Nokia | For the first main bullet, our preference would be Alt 1), we can also compromise to Alt 4) if majority so prefers. If we need to limit further to single additional scs for initial access, based on e.g. Alt3 or 5, our preference would be in order of 960kHz, 240kHz or 480kHz. We are also OK with the proposed additional constraints.  On the second main bullet, we are fine with the first sub-bullet, i.e. support of 480kHz or 960kHz SSB/SCS is not mandatory for the UE. We would prefer Alt-A for defining the relation between control/data support and SSB support. |
| Xiaomi | Alt2 and Alt3 are our preference, we do not support Alt6. Other FL’s proposal is ok to us. |
| OPPO | For 240/480/960kHz SSB, we support Alt 4) and can compromise to Alt 5) or 1).  For optionality of 480/960kHz SCS, we support Alt A). |
| Futurewei | We prefer Alt-6 as the first option, which is the status quo and sufficient for single numerology operation. As a compromise Alt-7 proposed by LGE with Qualcomm modifications can be acceptable to us. For the second bullet we support Alt-A. |
| Lenovo, Motorola Mobility | For the first bullet, we prefer Alt. 4, supporting both 480 and 960kHz for SSB for initial/non-initial access to allow single numerology operation and to avoid the necessity of BWP switching when data/control use these values. We are also fine with Alt. 1 to support 240kHz as an additional numerology since it is already supported for FR2. We don’t see the motivation to select only one SCS among 240, 480, and 960kHz. For the second bullet, we are fine with the sub-sub-bullets under the first sub-bullet and Alt A for the second sub-bullet. |
| Interdigital | As for the supported SCS for the SSB, our preferences are Alt.4 and Alt.5 and we do not support Alt.6.  As for the UE capability, we support the UE capability for SSB SCS to be the same as that of the data/control channels’ SCS. So, we support Alt A implying the single capability per SCS. |
| CATT | For the first bullet, we can accept Alt5 (with constraint satisfied), or alt6 with the ANR issue resolved. For UE capability discussion , we agree that UE is not expected to support 480 /960 kHz SCS for SSB if it doesn’t support 480/960 kHz SCS for data/control channels. But in general we think these discussion should happen at later stages. |
| Intel | Regarding SCS of SSB for initial access, our first preference is Alt.4 or Alt.5. We could also agree on Alt.1 or Alt.2. We think Alt.3 should be excluded from the list as it spurs further discussion on down-selection between SCS values. A clearer approach in that sense is to include Alt. 7 (from LG) into the list instead of Alt.3. We don’t think Alt.8 (from Qualcomm) is a real alternative suitable for discussion here as it says nothing about initial access case. Probably, it’s better to treat Alt.8 as part of discussion on Section 2.1.2 or 2.1.5.  We don’t support Alt. 6 or Alt. 7. We still don’t agree that any of Alt.6 or Alt.7 can provide true single numerology operation as either of the alternatives mandates non-standalone (e.g., dual carrier) operation for devices which demand high data rates relying on wide bandwidth with large SCS.  Regarding the clarification on optionality, we support the first sub-bullet. For the second sub-bullet, we are open for discussion among the different choices. If supporting different capability aids getting the group closer to agreement on SSB issues, we will be positive for it. |
| vivo | For the 1st bullet, our first preference is Alt 5, and can compromise to Alt 1 or Alt. 2 or Alt 4. We don’t support Alt. 6 and Alt. 7.  As discussed is our contribution, if 480K/960KHz can’t be used for initial access case, the possible deployment scenarios allowed by spec are not suitable or efficient especially in managed networks. In this scenario, standalone operation in unlicensed band is typical. For Alt. 6, at least two BWPs or carriers with different SCS are mandatory to be supported in both network and UE side.  For the 2nd bullet, we support Alt A. |
| Convida Wireless | For SSB SCS, we prefer Alt 4 and are open for Alt 1. Also, if SCS 480/960 KHz for SSB are supported, then Alt A is the first preference. |
| Ericsson | Clearly Alt-6 is the baseline/fallback if there is no consensus.  We support Alt-7 as proposed by LGE, since it requires no specification effort (already specified in Rel-15 FR2).  We can accept Alt-1 to enable more use cases. We are okay with the additional constraints as long as both licensed and unlicensed operation are taken into account. However, to limit the work, we think there should also be a constraint on the supported SSB-CORESET0 multiplexing patterns.  Regarding capabilities, we think that discussion can be deferred. There doesn't seem to be an urgency to settle that now. That being said, Alt-A with single capability per SCS seems logical. |
| Sony | For SSB SCS, alt 4 or alt 5 is our first preference. Alt 1 or alt 2 could be fine for us since 240 kHz SCS has already been supported in FR2. |
| WILUS | For the 1st bullet on SCS for SSB, our first preference is Alt 4 or Alt 5. We are also fine with Alt 1 or Alt 2, but we do not support Alt. 6 or Alt 7.  Regarding the 2nd bullet on optionality of 480/960kHz SCS, we support the 1st sub-bullet and support Alt A implying the single capability per SCS. |
| Spreadtrum | We support Alt 4. 480kHz and 960kHz SCS for SSB have equal positions, and 480kHz and 960kHz SCS for data/control also have equal positions.  For initial access capability, we support separate capability for 480/960kHz respectively. For data/control capability, it should be not be discussed at this sub-topic, and it can be finalized in UE feature discussion. |

#### **1st Round Discussion Summary:**

Summary of responses from companies are provided below.

* Further discussion on 240/480/960kHz SSB
  + Alt 1) Supporting 240, 480, and 960 kHz SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
    - Docomo, Samsung, ZTE, Sanechips, Nokia, NSB, OPPO, ~~Futurewei,~~ Lenovo, Motorola Mobility, vivo, Ericsson, OPPO, Convida, Sony
  + Alt 2) Supporting 240 kHz and one of 480 or 960 kHz SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
    - LGE, Samsung, ZTE, Sanechips, vivo, Xiaomi, Sony
  + Alt 3) Supporting one of 240, 480, or 960 kHz SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
  + Alt 4) Supporting 480 and 960 kHz for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
    - Docomo, Samsung, ZTE, Sanechips, ~~Futurewei,~~ Lenovo, Motorola Mobility, Interdigital, Intel, WILUS, Spreadtrum, OPPO, Convida, Sony, Spreadtrum
  + Alt 5) Supporting one of 480 or 960 kHz SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
    - Docomo, Samsung, ZTE, Sanechips, Nokia, NSB, OPPO, ~~Futurewei,~~ Interdigital, CATT, Intel, vivo, WILUS, Sony
  + Alt 6) conclude no support of 240, 480, and 960kHz SSB for initial access.
    - Huawei, HiSilicon, Qualcomm, Mediatek, Futurewei, CATT(with ANR resolved)
  + Alt 7) Supporting 240kHz SCS SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB
    - LGE, Qualcomm, Ericsson, Futurewei
  + Alt 8) Supporting 480 and 960 kHz SSB for non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB if the timing of the SSB is known to the UE.
    - Qualcomm
  + Additional constraints:
    - Limited sync raster entry numbers (details can be sorted out if generally acceptable)
    - only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS
    - SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical
* Clarification on optionality of 480/960kHz SCS.
  + Supporting 480 kHz SCS and 960 kHz SCS for SSB are UE capabilities:
    - UE is not expected to support 480 kHz SCS for SSB if it doesn’t support 480 kHz SCS for data/control channels.
    - UE is not expected to support 960 kHz SCS for SSB if it doesn’t support 960 kHz SCS for data/control channels
  + Optionally Supporting 480/960kHz SSB is:
    - Alt A) same capability as supporting 480/960kHz SCS, respectively (e.g. single capability per SCS, UE indicates support of 480kHz SCS mean support 480kHz SSB and 480kHz data/control/RS)
      * Docomo, Samsung, Qualcomm, ZTE, Sanechips, Futurewei, Lenovo, Motorola Mobility, Interdigital, vivo, Convida Wireless, Ericsson, WILUS
    - Alt B-1) separate capability from supporting 480/960kHz SCS for data/control/RS and SSB, respectively, and same capability for supporting initial access (if this case is supported) & non-initial access (2 different capability for each SCS)
      * Spreadtrum
    - Alt B-2) separate capability from supporting 480/960kHz SCS for data/control/RS and SSB, respectively, and separate capability for supporting initial access (if this case is supported) & non-initial access (3 different capability for each SCS)
      * Spreadtrum

#### **2nd Round Discussion – Part 1:**

For the clarification on optionality of 480/960kHz SCS, all companies seem to be in alignment.

Suggest agreeing to following proposal:

##### **Proposal 1.1-1)**

* Supporting 480 kHz SCS and 960 kHz SCS are UE capabilities:
  + UE supporting 480kHz SCS for data/control channels also support reception of SSB with 480kHz SCS.
  + UE supporting 960kHz SCS for data/control channels also support reception of SSB with 960kHz SCS.
  + UE is not expected to support 480 kHz and 960 kHz SCS for SSB if it doesn’t support 480 kHz and 960 kHz SCS for data/control channels, respectively.

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| **Company** | **Comment** |
| Samsung | We support the proposal. |
| Qualcomm | We support the proposal with this addition/clarification:   * *Supporting 480 kHz SCS and 960 kHz SCS are UE capabilities:*    + *UE supporting 480kHz SCS for data/control channels also support reception of SSB with 480kHz SCS (for the agreed access cases and conditions)*   + *UE supporting 960kHz SCS for data/control channels also support reception of SSB with 960kHz SCS (for the agreed access cases and conditions)*   + *UE is not expected to support 480 kHz and 960 kHz SCS for SSB if it doesn’t support 480 kHz and 960 kHz SCS for data/control channels, respectively.* |

#### **2nd Round Discussion – Part 2:**

For the SCS issues, focusing on alternatives that has the largest support, the following seems to the list that RAN1 should focus on.

* Further discussion on 240/480/960kHz SSB
  + Alt 1) Supporting **240, 480, and 960** kHz SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
  + Alt 4) Supporting **480 and 960** kHz for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
  + Alt 5) Supporting **one of 480 or 960** kHz SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.
  + Alt 6) conclude **no support of 240, 480, and 960kHz** SSB for initial access.
  + Additional constraints:
    - Limited sync raster entry numbers (details can be sorted out if generally acceptable)
    - only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS
    - SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical

Additionally, from the list Huawei, HiSilicon, Qualcomm, and Mediatek are the companies who prefer Alt 6, who do not have alternative proposals they could live with that are largely favored by companies. The reasons for each company support some alternatives were discussed in the previous meeting pretty thoroughly.

* So moderator would like to ask Huawei, HiSilicon, Qualcomm, and Mediatek if there are nothing from the Alt 1, 4, 5 they can accept and briefly comment on the main concerning aspect for either Alt 1, 4, 5.
* Similarly to proponents of either Alt 1, 4, 5, briefly comment on the main concerning aspect for Alt 6, which is likely the implicitly conclusion when there is lack of additional agreements.
* Lastly, if there is some alternative that companies think would help breach this impasse, please comment so.

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| **Company** | **Comment** |
| Samsung | One comment from our previous round is not addressed. The supporting for 480 and 960 kHz for non-initial access case is already agreed, so Alt 5) is a little bit against such agreement by only allowing one of them for non-initial access case.  Alt 5) Supporting **one of 480 or 960** kHz SSB for initial ~~& non-initial access~~ with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints.  For Alt 6), our concern is the too limited implementation flexibility allowed by the network, and the system has to implement in mixed numerology if one wishes to implement a standalone system with 480/960 kHz data/control/RS.  Alt 6) is also not beneficial from the forward compatibility point of view. Rel-17 is the first release for supporting the new frequency range, and if there is no specification support for flexible choice of the SCS in initial access, there is no chance in future release to address this issue.  If companies have concern on the complexity of initial cell search (i.e., the sync raster design), RAN1 can try to provide specification support for the SCSs and leave the choice of SCS for initial access per band to RAN4. More specifically, we are considering the following as a way forward (just a general description of the intention, and wording can be further polished).  RAN1 provides specification support for 240, 480, and 960 kHz SSB for initial & non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with constraints, and up to RAN4 to decide the SCS of SSB for initial access for each band in 52.6 to 71 GHz. |
| LG Electronics | First of all, we agree with Samsung’s comments for Alt 5.  It is unfortunate our preferred alternatives disappear from the table. For the sake of progress, we can accept Alt 5 with modification from Samsung which has the least UE implementation burden among Alternatives 1, 4, and 5. |

#### **2nd Round Summary:**

TBD

### 2.1.2 ANR and CGI Reporting

* From [2] Huawei, HiSilicon:
  + Support CGI report on cells that broadcast 120 kHz SSB in 52.6 GHz to 71 GHz spectrum as in Rel-15/16.
  + RAN1 further discuss whether and how to support inter-operator PCI collision for 480/960 kHz SSBs whose SSB location and SCS are explicitly provided to the UE (non-initial access) and SSB does not configure Type-0 PDCCH.
* From [3] vivo:
  + ANR should be supported for 480/960KHz SSB by indicating Type-0 PDCCH in the SSB.
* From [7] CATT:
  + The agreement of supporting 480 KHz and 960 KHz SCS for non-initial access should be extended to include the feature to address ANR issue.
* From [10] ZTE, Sanechips:
  + In non-initial access cases, SSB with 480/960kHz SCS should be allowed to configure Type0-PDCCH in the MIB for supporting ANR function and CGI reporting.
* From [16] Samsung:
  + Support ANR and inter-operator PCI confusion resolution for all supported SS/PBCH block subcarrier spacings, and the CORESET#0/Type0-PDCCH configuration is provided by the MIB of the SS/PBCH block.
* From [17] Mediatek:
  + Solution to enable ANR use case can be discussed after LBT bandwidth and the number of synchronization raster within a LBT bandwidth are decided.
* From [18] LGE:
  + Further discuss whether/how to support ANR functionality for SS/PBCH block with a SCS when SS/PBCH block with the SCS does not configure CORESET#0 and type0-PDCCH CSS set.
* From [28] AT&T, NTT DOCOMO, INC., T-Mobile USA:
  + RAN1 shall provide solutions to support ANR and inter-operator PCI confusion resolution for all supported SSB subcarrier spacings in 52.6 GHz and beyond

#### Summary of Discussions

* Discussion further on how to support inter-operator PCI confusion resolution for 480/960kHz SSB case
  + Huawei, HiSilicon, LGE, MEdiatek
* Support ANR by supporting CORESET#0/Type0-PDCCH configuration in 480/960kHz SSB
  + vivo, Intel, ZTE, Sanechips, Samsung, [CATT]
* RAN1 to conclude provide support for ANR and inter-operator PCI confusion resolution for all supported SSB SCS
  + AT&T, NTT DOCOMO, INC., T-Mobile USA
* Moderator suggestions:
  + Most companies seems to hint ANR and PCI confusion resolution issues are something worth while to resolve, and moderator suggests to further discuss over email.
  + Given the many company support, moderator suggests to further discuss (as starting point) based on following proposal:
    - Support ANR by supporting CORESET#0/Type0-PDCCH configuration in 480/960kHz SSB

#### **1st Round Discussion:**

Moderator suggest discussing on the following proposal. Moderator would like to encourage companies who prefer Alt 2 of Proposal 1.2-1 to describe the method.

##### **Proposal 1.2-1)**

* To support ANR and PCI confusion resolution,
  + Alt 1) Support CORESET#0/Type0-PDCCH configuration in MIB of 480 and 960kHz SSB
  + Alt 2) [alternative method] to enable support to obtain neighbor cell PCI and SIB1 contents related to CGI reporting

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| **Company** | **Comment** |
| DOCOMO | We prefer to support Alt 1 regardless of the support of Alt 2 since Alt 1 could be simpler solution which is something already supported in the previous releases in NR. |
| LG Electronics | Alt 2 is preferred. One possible way could be that MIB (e.g., with 960 kHz SCS) indicates frequency domain location of SS/PBCH (e.g., with 120 kHz SCS) being able to configure CORESET#0 and type0-PDCCH CSS set. |
| Samsung | We believe there is no confusion on how to support the ANR purpose for 120 kHz (current spec already supports so), so in this sense, Alt 2 should be also for 480 and 960kHz SSB only, or more straightforward to restrict the discussion for 480 and 960kHz SSB in the main bullet.   * To support ANR and PCI confusion resolution for 480 and 960 kHz SSB,   As explained in the contribution, we don’t know how dedicated signalling can work for resolving PCI confusion for inter-operator case. If Alt 2 refers to the dedicated signalling approach, please clarify; if not, please provide the details of such alternative method. |
| Huawei, HiSilicon | While we are open to discuss the need to support PCI confusion resolution, we cannot agree with Proposal 1.2-1 in this form due to the following three reasons:   1. **If there is a PCI confusion on a reported PCID from a 480/960 kHz SSB, it does not result in a HO failure. As such, the need for PCI confusion resolution for 480/960 kHz SSB should be clarified:** To our understanding, the main reason for PCI confusion resolution is to avoid a subsequent HO failure. However, as we have explained in our t-doc (R1-2104273) as well as in the previous meeting, given the fact that, based on the current agreements, 480/960 kHz SSBs do not configure Type-0 PDCCH (and, hence, do not configure SIB1), even if there is a PCI confusion of a reported PCID on 480/960 kHz SSB, such a PCI confusion does not result in HO failure. Let us provide further clarification using the following example: If a UE measures a neighboring Cell-A, the measurement report that includes SS-RSRP along with a PCI is associated with a corresponding MeasObject, which, itself, includes the target SSB frequency and the SSB SCS. In other words, the reported PCI/SS-RSRP back to the serving gNB is appended with a (SSB Freq., SSB SCS) pair. As such, if the appended SSB SCS = 480/960 kHz, since serving gNB knows “No cell of any operator transmits a 480/960 kHz SSB that configures SIB1” (let’s call it **Side Information A**), it already knows that the reported Cell-A does not broadcast SIB1, and, as such, the serving gNB does not initiate HO process for the reported Cell-A. Therefore, even if there are multiple cells with the same PCI from potentially multiple operators, regardless of whether none, some, or all these cells are included in the serving gNB’s NCRT, since all gNBs of all operators have **Side Information A**, the PCI confusion (or PCI collision) does not result in any subsequent HO failure: Irrespective to the single or multiple operators scenario, all gNBs know that if a reported PCI is associated with a SSB SCS = 480/960 kHz, the corresponding cell does not broadcast SIB1 and the gNB would not initiate HO process for such a target cell.   **Note:** Please note that the mere fact that PCI confusion mechanism was supported in Rel-16 is not a strong reason to support such a mechanism in Rel-17 for 480/960 kHz SSBs. In Rel-16, all supported SSBs can potentially configure SIB1 and be used a cell-defining SSB for PCells. Based on the current agreements, this is certainly not the case for 480/960 kHz SSBs in Rel-17.   1. **Even if PCI confusion resolution for 480/960 kHz SSBs is deemed required, there are mechanisms to support it without UE CGI report. This is an alternative that is not considered in Proposal 1.2-1:** As we discussed in our t-doc (R12104273), there are mechanisms to support ANR and PCI confusion resolution without UE involvement. These include:    1. *Monitoring of DL channels by gNBs*   In this mechanism, gNBs monitor DL channel and collect detectable PCI/CGI information of the neighboring cells. This mechanism can be used in both intra-operator and inter-operator scenarios. OAM can reassign PCID of each gNB if there is a PCI collision between cells of the gNB and those of neighboring cells.   * 1. *Neighbour information exchange using Xn signaling*   In this mechanism, gNBs share their served cell PCI/CGI information using Xn interface. Therefore, PCI collision can be avoided without any UE involvement. Specification 38.300 provides the following lines regarding this mechanism:   |  | | --- | | *Excerpt from 38.300 Clause 15.3.3 Automatic Neighbour Cell Relation Function*  NOTE: The neighbour information exchange, which occurs during the Xn Setup procedure or in the gNB Configuration Update procedure, may be used for ANR purpose. |   Note that this mechanism can be used if Xn interface is stablished among gNBs. Xn interface is typically stablished among gNBs of the same operator. It may also be stablished in inter-operator scenario if operators use the same vendor.  CGI report and above two mechanisms to support PCI confusion resolution have their own advantages and disadvantages. It is noteworthy that, a disadvantage of CGI report is that it is a costly method since it requires additional UE reporting and may also have a higher latency   1. **Even if PCI confusion resolution for 480/960 kHz SSBs is deemed required, and, further, UE CGI report is deemed necessary to support PCI confusion resolution, CORESET#0/Type0-PDCCH configuration in MIB of 480/960 kHz SSB for the mere support of CGI report (Alt 1 in Proposal 1.2-1) is not an acceptable alternative:** CGI report can be easily and more efficiently supported using dedicated signaling (Explained further below). Note that if we specify CORESET#0 and Type0-PDCCH CSS set monitoring occasions just for CGI report (use a similar mechanism that enables UE to read SIB1 in Type0-PDSCH for Initial access), it means that we would have to design CORESET#0 including supported {SSB, CORESET#0} multiplexing patterns, number of supported RBs, number of symbols, RB offsets, and also design PDCCH monitoring occasions for Type0-PDCCH CSS set for both 480 and 960 kHz SSBs. In addition, SIB1 carried in Type0-PDSCH is up to 2976 bits and can contain more than 100 parameters including parameters related to cell access, access category information, cell selection, connection establishment failure control, acquisition of OSI, UE’s timers and constants, cell specific parameters of a UE including the position in burst, periodicity, and power of serving cell SSB, cell specific Uplink/Downlink TDD configuration, common parameters of the initial UL and DL BWPs which include Paging related configuration, cell specific parameters for PDCCH, PDSCH, PUCCH, PUSCH, RACH, MsgA and so on… Among all these parameters, only three (PLMN identity, cell Id, cellReservedForOperatorUse bit) in cell access related information IE are required for CGI report. Going through all these specification efforts to support broadcasting SIB1 that, in general, provides all cell-specific configurations and contains much larger parameter set than what is required for CGI report is not justifiable in our view.   **How to support CGI report using dedicated signaling:**  Let’s say there is a PCell and Cell-1 and Cell-2. Cell-1 and Cell-2 both transmit 480(960) kHz SSB without CORESET#0 and both have PCID-1. Cell-1 and PCell belong to the same operator and, as such, Xn signaling is stablished between them while Cell-2 belongs to another operator. Since PCell and Cell-1 are connected using Xn, PCell can know the location at which Cell-1 transmits its CGI parameters (eg: Cell ID and PLMN ID --let’s call them collectively as CGI-Info). Now, if UE reports a PCID-1 derived from a detected 480(960) kHz SSB to PCell, PCell may ask UE to read the CGI-info using DCI. DCI provides the CGI-info location of Cell-1 to the UE. If UE cannot find the CGI-info in the provided location, it simply means that UE had actually detected Cell-2. In such a case, UE reports an ERROR (or a message like “noSIB1”) so PCell would know that the detected cell is not cell-1 and belongs to another operator. In the unlikely situation that the location of PCI-Info for cell-1 and cell-2 happen to be the same, there is still no problem: UE can just detect the CGI corresponding to the actually detected cell and report the CGI back.  **Summary:**  Given all above discussion, we can provide the following proposal as a compromise:  ***Proposal:***   * ***RAN1 further discuss whether/ how to support PCI collision resolution mechanism for 480/960 kHz SSBs whose SSB location and SCS are explicitly provided to the UE (non-initial access) and SSB does not configure Type-0 PDCCH.*** * ***For the discussion to support PCI collision resolution, following alternatives are considered:***   + ***PCI collision resolution mechanism is implemented without UE CGI report.***     - ***Examples: Monitoring of DL channels by gNBs, Neighbour information exchange using Xn signaling***   + ***PCI collision resolution mechanism is specified based on UE CGI report where PDCCH associated with the PDSCH carrying CGI parameters is provided by dedicated signaling*** |
| Qualcomm | We support Alt 1 under the restriction of known timing. We are also open discussing Alt 2 depending on the designs proposed. |
| DOCOMO2 | On the proposal made by HW:   * For the first bullet, we are ok if it is concluded that 480/960 kHz SCS are not supported for SSB during initial access. * For the second bullet about alternatives,   + Given the following considerations, if we have the examples HW has kindly proposed, we are not sure why we need to preclude UE CGI report as a measure for ANR.     - Monitoring of DL channels by gNBs enforces to deploy gNB with IAB-like capability only, which we believe makes practical operation more complex than CGI report     - As HW kindly pointed out in their tdoc, Xn signaling is basically possible between intra-operator gNBs or inter-operator gNBs by same vendor only, by which PCI collision between inter operator with different vendor’s gNB is not possible. It could be too much restriction if gNBs with same vendor only have to be deployed even by different operators in 60 GHz. We believe such restriction can make the practical deployment much harder. Why 3GPP needs to have such restrictions would be unclear for us.   + For the second sub-bullet, why we have to go directly with the discussion about “how to support CGI report carried by PDSCH” with the same feeling as Samsung. We think there still be another way to support ANR with neither such PDSCH carrying CGI report nor CORESET#0/SIB1 with larger SCSs. At least referring 120 kHz CORESET#0/SIB1 can be considered although our preference is still Alt 1.   Note that PCI collision is necessary not only for HO failure but also RRM measurement. So we still see the strong necessity to support ANR. |
| Mediatek | As commented in 2.1.1, the significance of 480/960 kHz SCS for ANR purpose is not clear to us, since by using 120 kHz SCS, the CGI information can be provided to UE. It would be very much appreciated if it can be further clarified. |
| ZTE, Sanechips | Alt 1 is a simple solution to support ANR and PCI confusion resolution, thus Alt 1 is preferred for us. Supporting Alt 1 does not mean excluding any other possible methods, only if we have consensus on these methods. |
| Nokia | Our preference would be Alt1. This functionality is rather elementary for the system operation, thus the simplest and most straight forward method to support it is to provide the CORESET#0/Type0-PDCCH configuration in MIB.  Based on existing agreements, we could assume to have PCell on some other band (≠B52GHz band), and have the Pscell or Scell on B52GHz band. In such scenarios it may not be feasible to fall back to obtain the CGI from the e.g. 120kHz SSB, if the device in question does not support said band. For Xn based procedure or for PDSCH based mechanism to work successfully, we are in practice assuming known (intra-vendor/operator) cell, like pointed out by DOCOMO. For unlicensed band operation, we are not convinced that this can always be assumed. |
| OPPO | We are open to discuss Alt 1 and Alt 2 for ANR and PCI confusion resolution. |

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| Futurewei | We prefer further discussions on this topic; we see a lot of opinions and questions that need further clarification before a decision. |
| AT&T | We support Alt. 1. Specifically, we don’t want a band specific solution for ANR/PCI confusion resolution. Lastly, regarding Huawei’s proposal, similar to Samsung, we don’t understand how dedicated signaling can address the problem we are trying to solve here. Dedicated signaling and the whole topic of inter-operator PCI confusion resolution was discussed at length in NR-U in Rel. 16 in RAN1, RAN2, and RAN. We have little sympathy for why we need to repeat that discussion in Rel. 17 for 52.6 GHz and beyond. The situation is exactly the same. Repeating past discussions is not appropriate. We also share Docomo’s concerns on Huawei’s proposals in terms of complexity and feasibility. |
| Lenovo, Motorola Mobility | We support Alt 1 as a basic functionality which is already supported in Rel15. We are also fine to discuss the support of Alt 2. |
| Interdigital | As we have already discussed in the tdoc, the UE should be provided with the CORESET#0/Type0-PDCCH configuration for the ANR function. Though Alt.1 is the straightforward option, the Alt.2 can be considered as the alternative in case the configuration based on Alt.1 is not available.  Alt.2 can be implemented by having the semi-static configuration of the parameters for the CORESET#0 and Type0-PDCCH, where the time and frequency allocations and the multiplexing patterns are (pre)configured in fixed settings. Then the UE may identify the (pre)configured location of CORESET#0 and Type0-PDCCH based on the SCS, the carrier frequency, or the RRC settings. |
| CATT | We are OK with Alt1. It may have some complexity involved but it is a simple solution. If companies can have consensus for a specific alt2 solution we are also open. |
| Intel | Support Alt.1 as it’s a well-known solution. Continue discussing Alt.2.  One of the important things to note is future forward compatibility. In section 2.1.1, we are discussing the possibility of supporting initial access for 480kHz and 960kHz. If such feature does not get introduced, the current Release-17 will be defined in a such way to have quite negative impact to introduction of new features and modes of operation. CORESET#0/Type0-PDCCH signaling can be a key aspect in keeping forward compatibility. Therefore, we suggest supporting Alt.1 first now as it will resolve ANR issues and provide forward compatibility with whatever we support in Section 2.1.1 or in future releases. |
| vivo | We support Alt 1 due to the need of solving ANR and PCI confusion issue.  Regarding Huawei’s comment on the reasons of not supporting Alt. 1, we have the following response:  For Reason 1, we think PCI confusion is needed with the following clarification:  We agree that PCI confusion won’t cause HO failure if 480K/960K SSB is not used for initial access case. However, it will result in wrong configuration of Scell or PScell due to misunderstanding of the RRM measurement. One example is provided below: UE1 belongs to operator 1 and have dual connectivity to gNB1a and gNB1c from operator 1. Since gNB1b is a neighbor cell of gNB1a, UE1 will be configured with measurement on PCI 2. However, due to the same PCI between gNB1b and gNB2b, UE1 will report the measurement on gNB2b to gNB1a and thus gNB1a may misunderstand UE1 is closer to gNB1b. So gNB1a will configure gNB1b as PScell for UE1 which result in performance loss. We hope this could clarify the need of solving PCI confusion between operators.    For Reason 2, it lists several alternatives to solve PCI confusion and ANR problem other than CGI reporting, we don’t think they are applicable.   * For Alt. a “Monitoring of DL channels by gNBs”, we think monitoring of DL channels is UE function and not implemented in legacy gNB. Even gNB can monitor DL channel, gNB1b may not hear gNB2b and the PCI confusion can’t be solved either. * For Alt. b “Neighbour information exchange using Xn signaling”, we don’t think the gNBs belonging to different operators could have Xn interface.   For Reason 3, we don’t think CGI reporting via dedicated signaling could serve the purpose of ANR.  As discussed in our Tdoc R1-2104348, the purpose of ANR function is to relieve the operator from the burden of manually managing neighbor cell relations (NCRs), which are mainly used for mobility purpose (p.s. in practice, NCRs largely are configured manually). NCRs are cell-to-cell relations, while an Xn link is set up between two gNBs. One typical deployment scenario is illustrated below: gNB1&2&3 are legacy carriers in FR2 with 120K PCell and gNB a, b ,c ,d are newly deployed carriers in 52.6-71GHz with 960K PScell. The Xn interface should be established between them. One way is manual configuration which impose high burden to operators. ANR provides a good way to managing this automatically, which is the main reason to introduce ANR. In this case, how to use dedicated signaling for CGI reporting before there is Xn interface between them (e.g. dashed line in the following figure)    In summary, Alt. 1 is the only way to perform CGI reporting for solving ANR and PCI confusion problem. |
| Convida Wireless | We prefer Alt 1. |
| Ericsson | We support both Alt-1 and Alt-2.  We also agree with other companies that it makes sense to restrict the discussion to 480/960 since there is no specification work needed for 120 kHz  We think it would be more appropriate to change the wording of the main bullet as follows:  To support ANR and PCI conflict detection ~~confusion resolution~~  since the functionality we are discussing is only the first step of ANR, i.e., methods for the UE to report ECGI for the gNB to learn if there is a PCI conflict. Once the gNB determines there is a conflict within the same/different operator, how to resolve the conflict is outside of the scope of RAN1.  The reason for supporting Alt-2 is that if we cannot achieve consensus on CORESET#0/Type0-PDCCH configuration being provided by MIB of 480/960 kHz SSB (Alt-1), then we would need a fallback solution (Alt-2), and we think a workable fallback solution exists via provision of CORESET#0/Type0-PDCCH configuration through dedicated signaling. At heart, ECGI reporting for ANR is about using the UEs as sensors for PCI conflict detection, and different UEs (sensors) can be provided with different CORESET#0/Type0-PDCCH configurations, using the observation that for a given SSB frequency domain location (already provided to the UE by dedicated signaling), there are a quite limited number of possible CORESET#0/Type0-PDCCH configurations that could be configured by any operator. If different UEs are provided with different configuration candidates, and any one or more of the UEs reports an ECGI that is unknown to the gNB, then the PCI conflict is detected.  Already in Rel-15, both the SSB frequency domain location (ARFCN) for the UE to measure is explicitly provided to the UE in *measObjectNR,* and the PCI for which to report ECGI is explicitly provided in *reportConfigNR*, both through dedicated signaling when the UE is in CONNECTED mode. It seems like a simple extension to also include a parameter that provides the CORESET0/Type0-PDCCH configuration. |
| WILUS | We support Alt 1 and open to discuss Alt-2 as an alternative for ANR and PCI confusion resolution. |
| Spreadtrum | We support Alt 1. |

#### **1st Round Discussion Summary:**

Summary of responses from companies are provided below.

* To support ANR and PCI confusion detection for 480/960kHz,
  + Alt 1) Support CORESET#0/Type0-PDCCH configuration in MIB of 480 and 960kHz SSB
    - Agree: Docomo, Samsung, ZTE, Sanechips, Nokia, OPPO, AT&T, Lenovo, Motorola Mobility, Interdigital, CATT, Intel, vivo, Convida Wireless, Ericsson, WILUS, Spreadtrum
      * Main reasons:
        + Unclear why CGI reporting for 480/960kHz is precluded

gNB directly monitoring requires gNB to support IAB-like capability

Xn is only possible for same operator

* + - * + Inter-operator ANR
        + PCI confusion is not only for avoiding HO, but also to relive operator burden for manual managing neighbor cell relation (NCR)
        + Future forward compatibility
    - Object: Huawei, HiSilicon
      * Main reasons:
        + Believe PCI confusion is to avoid HO failure, and alternative method exist to avoid HO failure
        + Following techniques are possible for ANR:

gNB directly detecting neighbor cell SSB

Xn signaling to exchange information between connected gNB

* + - * + SIB1 overhead is too large just for sharing PLMN info
        + DCI based CGI-info transmission (new feature?)
  + Alt 2) [alternative method] to enable support to obtain neighbor cell PCI and SIB1 contents related to CGI reporting
    - Agree: LGE, OPPO, Interdigital, Ericsson
    - FFS: Lenovo, Mobility Mobility, CATT, Intel, WILUS

#### **2nd Round Discussion:**

Based on the discussion so far, the path forward on this issue seems clear. Moderator suggests focusing on alt 1 and while keeping alt 2 as FFS. At the very least we could try to work with this as working assumption.

##### **Proposal 1.2-2)**

* For agreement or working assumption:
  + To support ANR and PCI confusion detection for 480/960kHz SCS based SSB, support CORESET#0/Type0-PDCCH configuration in MIB of 480 and 960kHz SSB
    - FFS: additional method(s) to enable support to obtain neighbor cell PCI and SIB1 contents related to CGI reporting

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| **Company** | **Comment** |
| Samsung | We support the proposal.  We already expressed our concern on the feasibility of using dedicated signalling for providing the CORESET#0/Type0-PDCCH configuration. If there are other approach under the FFS, we are ok to list as details as part of the proposal for further discussion (it’s more clear to judge whether such additional method is needed). |
| AT&T | In RP-191581, RAN agreed that this is “essential functionality” in unlicensed spectrum. Subsequently, RAN1 specified the feature in TS 38.213, Section 13 for operation with shared spectrum channel access. The feature was also endorsed by both RAN1 (3GPP TR 38.889 V16.0.0, Study on NR-based access to unlicensed spectrum) and RAN2 (Chairman notes for 3GPP RAN2 #103bis meeting, Chengdu, China, October 2018) during the study item phase. In light of the above history and the vast number of existing agreements on this issue in two WGs and RAN during Rel. 16, we would like to hear from Huawei, who according to the summary is the only objecting company and to my recollection did not have any concerns in Rel. 16 when this feature was agreed in RAN1 for NR-U, what is so fundamentally different in 52.6-71 GHz compared to 5 and 6 GHz that they now object to this feature. Given that only a single company objects, while 18 companies, incl. three operators strongly support the feature, a working assumption is the very least that should be agreed. In fact, it is very unfortunate how much time RAN1 is forced to spend on this topic given the exact same discussion already took place in Rel. 16 where everything was agreed and specified by consensus. |
| Qualcomm | We support this proposal |
| LG Electronics | Still it seems that companies have different views on the necessity of ANR support for 480/960 kHz SCS, which is optional feature. It should be noted that ANR can be already supported with 120 kHz SCS SSB/CORESET#0. Nevertheless, if we go with alt 1 due to majority view, we suggest to add the following note in order to minimize specification impact for optional features.   * + - Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible |

#### **2nd Round Discussion Summary:**

TBD

### 2.1.3 DRS Related Aspects

* From [1] Futurewei:
  + Support DBTW at least for SSB with 120 kHz SCS with the following requirements:
    - PBCH payload size is no greater than that for FR2
    - Duration of DBTW is no greater than 5 ms
    - Number of PBCH DMRS sequences is the same as for FR2
  + Support mechanisms to indicate or inform UEs that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs
  + Support signaling to indicate that LBT is disabled or enabled for the RACH procedure for UE in IDLE and CONNECTED modes
  + Consider using CSI-RS presence in the discovery burst for possible ways to do beam refinement during the initial channel access.
  + Consider selection of multiple SS/PBCH blocks at UE to perform transmissions of multiple RACH preambles (MSG1/MSG A) during initial channel access.
  + When RACH exchange may be considered as short control/management frames that can be exempt from LBT, gNB should signal to UEs if RACH exchange is LBT exempt.
* From [2] Huawei, HiSilicon:
  + Configure DBTW length in SIB1 for operations with shared spectrum in 52.6GHz to 71GHz with the following values:
    - 120 kHz SCS: {40, 32, 24, 20, 16, 10, 4} slots
    - 480 kHz SCS: {72, 32, 26, 20, 16, 14, 8, 4} slots
    - 960 kHz SCS: {64, 32, 26, 20, 16, 14, 8, 4} slots
  + To indicate for operation with shared spectrum in 52.6GHz to 71GHz, three bits are used from MIB payload as follows:
  + For SSB with 120 kHz, one bit from subCarrierSpacingCommon, one bit from ssb-SubcarrierOffset, and one bit from searchSpaceZero in pdcch-ConfigSIB1.
  + For SSB with 480 kHz or 960 kHz, one of the following alternatives can be selected:
    - Alt 1) one bit from subCarrierSpacingCommon, one bit from ssb-SubcarrierOffset, and one bit from pdcch-ConfigSIB1.
    - Alt 2) one bit from subCarrierSpacingCommon, two bits from pdcch-ConfigSIB1.
    - Alt 3) three bits from pdcch-ConfigSIB1.
* From [3] vivo:
  + Support DBTW in un-licensed band from 52.6 GHz to 71 GHz, no matter which SSB SCS.
  + The following methods could be considered to determine whether there is DBTW:
    - Alt. 1: Frequency band (licensed or un-licensed);
    - Alt. 2: The indicator in PBCH;
    - Alt. 3: The design of SSB sequence (PSS, SSS and DMRS).
  + The following methods could be considered to indicate the value of Q:
    - Alt. 1: Specify the value of Q for each SCS;
    - Alt. 2: Utilize the bits in PBCH;
  + With the increase value of Q and the introduction of DBTW, the ssbPositionsInBurst in SIB1 should be clarified.
* From [4] Spreadtrum:
  + DBTW can be supported.
* From [5] Nokia, NSB:
  + Support operation with and without DBTW for initial access.
  + If the DBTW assumption is to be provided to the UE, it would need to be available from the start to be useful.
  + If DBTW assumption can be changed, it should be available to the UE starting from initial cell selection.
  + It is possible to apply SCSe to one part of actually transmitted SSBs and LBT procedure for other/rest of the SSBs.
  + Consider semi-static or predetermined mechanism to determine which SSBs are under SCSe and which under LBT in certain time windows.
* From [6] Ericsson:
  + RAN1 needs to conclude on how to indicate LBT on/off (especially addressing the issue of DCI 1\_0 size during SIB1 reading) before any decision on supporting a DBTW is made.
  + Conclude that a DBTW is not supported for shared spectrum in the 52.6 – 71 GHz band.
* From [7] CATT:
  + For NR operation in 60 GHz unlicensed spectrum, the discovery burst transmission window (DBTW) shall be supported for 120 KHz SSB when gNB configures more than 56 SSBs transmission.
  + DBTW is not needed for SSB with 480 KHz/960 KHz SCS since the duty cycle is less than 10% over the 100 ms observation window for the short control signaling transmissions.
  + For indicating the DBTW enabling/disabling, following options can be further studied.
    - Option 1：1bit indication in MIB/PBCH, e.g. subCarrierSpacingCommon can be used if Type0-PDCH SCS can be implicitly indicated from SSB SCS.
    - Option 2：1 bit information indicated by SIB-1.
    - Option 3：If 1 bit is not available in PBCH/MIB, PBCH/MIB and SIB1 can be used jointly to indicate DBTW enabling/disabling.
  + If the actual number of SSB configured is up to 64, the scheme that DBTW is performed only for a sub-set SSB can be considered.
* From [8] Qualcomm:
  + for an unlicensed band that requires LBT, do not support discovery burst transmission window (DBTW) for SSB for all SCSs
  + for an unlicensed band that requires LBT, if DBTW for SSB is adopted for 120KHz SSB:
    - Minimize the number of bits needed to signal Q (1 or 2 bits) and thus the values (2 or 4 values)
    - Enabling/disabling DBTW can be implicit in the Q value
    - Based on other agreements/designs, consider getting the bits needed from one or more of the following: controlResourceSetZero, searchSpaceZero, ssb-SubcarrierOffset, subCarrierSpacingCommon (in case 120 kHz SSB and 480/960 kHz CORESET0 is not adopted)
    - Do not introduce new candidate SSB positions outside the FR2 Case D pattern, and the QCL relationship is introduced among the existing 64 candidate SSB positions
    - Consider having a subset of the SSBs (< 64) transmitted under the short control signal assumption while another subset can be best effort or have multiple positions per beam (have a Q factor within the subset)
* From [9] OPPO:
  + For above 52.6GH unlicensed spectrum, the DBTW within which additional SSB candidate positions may be configured is supported.
  + Reuse NRU mechanism to determine QCL relationship between SSB candidate indexes.
* From [10] ZTE, Sanechips:
  + Discovery burst transmission window (DBTW) should be supported for 120 kHz SSB SCS and other SSB SCSs.
  + For LBT exempt operation and overlapping licensed/unlicensed bands, it is not necessary to enable/disable the DBTW by explicit signaling. The impacts on LBT exempt operation brought by DBTW can be eliminated by configuration implementation.
* From [11] Intel:
  + At least for SSB SCS 120 kHz:
    - Support DBTW
    - Support signaling of enable/disable of DB and DBTW
    - Consider supporting Option 1 and/or 2 for DB and DBTW for 120kHz SSB:
      * Option 1:
        + Increase the number of candidate SSB indices up to 80, i.e., ;
        + Support additional values of n, such as 4, 9, 14, 19, in the equation defining the first symbols of candidate SS/PBCH blocks
        + For QCL relationship indication across SSBs, reuse Rel-16 NR-U mechanism by introducing parameter

FFS: or ;

* + - * + No changes to MIB payload size. Further discuss and consider reinterpreting bits from some bit fields within MIB to extend candidate SSB index and information.
      * Option 2:
        + Support floating DBTW, where the time (or slot) offset for DBTW can be smaller than 5msec.

FFS: smallest supported DBTW offset (i.e. granularity of the floating DBTW)

* + - * If neither Option 1 nor 2 is supported, RAN1 to support mechanism to balance out SSB DTX (among all SSB beams) from LBT failure.
* From [13] Apple:
  + If DBTW is introduced for above 52.6GHz frequency band, support enabling/disabling the DBTW by scrambling CRC bits of PBCH payload.
  + If DBTW is introduced, for above 52.6GHz frequency band, consider re-purposing the 1-bit 'subCarrierSpacingCommon' and 1-bit MSB of controlResourceSetZero to signal the Q value.
* From [14] Sony:
  + Discovery Burst Transmission Window should be supported.
  + If Discovery Burst Transmission Window is supported for 120 kHz SSB, additional n values (4, 9, 14, 19) should be supported.
* From [15] NEC:
  + DBTW should be supported at least for SSB transmission with 120 kHz SCS.
  + The long term sensing could be considered as an approach to mechanism for enabling/disabling DBTW.
  + The application of DBTW for SSB transmission could be indicated per SSB/beam.
  + The indication of Q value in NR-U should be reused to indicate DBTW enabling/disabling and Q value jointly at least for 120 kHz SSB SCS.
  + Additional discovery burst transmission window in the adjacent frame could be considered as a method of cycling SSB transmission.
  + With concurrent spatial multiplexing DBTWs, all SSBs could be transmitted in a cycling transmission fashion.
* From [16] Samsung:
  + Support discovery burst transmission window for 60 GHz unlicensed band.
    - The indication of Q can be in MIB for a best effort, and if not possible, in SIB1;
    - The indication of DBTW disabling can be joint coded with the indication of Q;
    - Support more than 64 candidate SS/PBCH block locations within a half frame;
      * Current PBCH payload can support timing indication of up to 128 candidate SS/PBCH block candidate locations;
      * For example, for 120 kHz SCS, support 80 candidate SS/PBCH block locations within a half frame;
    - For initial access, different synchronization raster entries are applied for licensed and unlicensed operations; for non-initial access, support an explicit indication of licensed or licensed operation when configuring a cell.
* From [17] MediaTek:
  + Do not support DBTW for SSB.
* From [18] LGE:
  + Consider the following methods to indicate enabled/disabled DBTW for idle and/or connected mode UEs.
    - Separate two sets of GSCN values where one set corresponds to the case of disabled DBTW while the other set corresponds to the case of enabled DBTW
    - Signalling via system information (e.g., measObject)
    - UE-specific RRC signaling (e.g., for SCell addition)
  + Consider all or some of the following bits to indicate candidate values.
    - subCarrierSpacingCommon
    - LSB(s) of ssb-SubcarrierOffset
    - dmrs-TypeA-Position
  + Discuss how to signal actually transmitted SSBs via ssb-PositionsInBurst when can be indicated to be less than 64 in MIB.
* From [19] Lenovo, Motorola Mobility:
  + For NR operation in unlicensed bands between 52.6 GHz and 71 GHz, potential enhancements related to periodic transmission of DRS such as SSB/PBCH/CORESET#0 are needed including:
    - performing directional LBT prior to the transmission of SSB according to the ssb-PositionsInBurst
    - directional LBT on multiple beams at the same time at the beginning of the DRS window
    - Cat 2 LBT (depending on the gap) before actual transmission
* From [20] Xiaomi:
  + Indication of DBTW information for initial access should be supported and could be carried in the PBCH.
* From [21] Interdigital:
  + Enhance the initial access operation to support Discovery Burst (DB) and Discovery Burst Transmission Window (DBTW) in unlicensed spectrum operations that require LBT in beyond 52.6GHz spectrum.
  + Consider the enhancements to indicate the enabling/disabling of the DBTW in initial access operations for the support of DBTW in shared spectrum in beyond 52.6GHz.
  + Support the enhancements on the reference tables in indication of the Q parameter for up to 64 SSB beams in initial access operations for unlicensed spectrum in beyond 52.6GHz, e.g., subsamples of the Q parameter.
* From [23] Sharp:
  + Adopt DBTW for SSB with 120 kHz SCS in above 52.6GHz.
* From [26] Charter:
  + DBTW is supported for 120 kHz, 480 kHz, and 960 kHz SCS SSB even in the non-initial access case.
* From [27] WILUS:
  + It seems beneficial to introduce discovery burst transmission window (DBTW) which makes it possible to define candidate SSB positions within the DBTW with support of DB which was already agreed.
  + It should be further considered that the additional candidate SS/PBCH block locations within a DBTW can be set to the closest slot locations after LBT failure at candidate SS/PBCH blocks locations as defined in FR2.

#### Summary of Discussions

* Companies have provided several detailed proposals. Most of the proposals are suggestions and answers to several sub-issues. Moderator suggest to continue discussion with the following question list, and try to resolve each question during the RAN1 meeting.
  + Whether or not to support DBTW for 120/480/960kHz SSB
  + Mechanisms to support enabling/disabling LBT & DBTW, including DCI 1\_0 size issue and where to signal enable/disable (if supported)
  + Additional information needed to be included in MIB to support DBTW, including which bits to re-purpose for the additional information
  + Supported DBTW lengths
  + Supported values
  + Whether to support floating DBTW
  + Whether to support mechanism to balance out SSB DTX (from LBT failure)
  + Number of candidate SSB positions (not number of Tx SSBs)

#### **1st Round Discussion:**

Companies are encouraged to provide inputs on the following questions

* Q1) Whether or not to support DBTW for 120/480/960kHz SSB
* Q2) Mechanisms to support enabling/disabling LBT & DBTW, including DCI 1\_0 size issue and where to signal enable/disable (if supported)
* Q3) Additional information needed to be included in MIB to support DBTW, including which bits to re-purpose for the additional information
* Q4) Supported DBTW lengths
* Q5) Supported values
* Q6) Whether to support floating DBTW
* Q7) Whether to support mechanism to balance out SSB DTX (from LBT failure)
* Q8) Number of candidate SSB positions (not number of Tx SSBs)

If there are other aspects that require discussion, please comment them and moderator will update the list accordingly.

|  |  |
| --- | --- |
| **Company** | **Comment** |
| DOCOMO | Q1) we support to introduce DBTW for all the supported SCSs in 52.6 – 71 GHz. As LBT can be mandatory for any SCS, the operation with DBTW should be possible with any SCS.  Q2) It can be associated with LBT on/off switching and/or whether LBT needs to be performed for the associated DB transmissions.  Q3) We prefer not to have any additional information in MIB for DBTW purpose.  Q4) We prefer to keep it as Rel-16 NR-U to avoid increasing UE implementation burden.  Q5) If only SSB and CORESET#0 multiplexing with the same numerology is supported, same as Rel-16 NR-U should be supported.  Q6) We do not prefer it from SSB detection complexity perspective at UE.  Q7) we do not see the necessity to support any other functionality than DBTW.  Q8) Ok with further study about this, but it should be realized under the same overhead as Rel-16 NR-U in our view. |
| LG Electronics | * Q1) Whether of not to support DBTW for 120/480/960kHz SSB   + Prefer to support DBTW for all of 120/480/960 kHz SSB * Q2) Mechanisms to support enabling/disabling LBT & DBTW, including DCI 1\_0 size issue and where to signal enable/disable (if supported)   + Three methods can be used for different purposes. The first method is to separate two sets of GSCN values where one set corresponds to the case of disabled DBTW while the other set corresponds to the case of enabled DBTW, which is for initial access. The second methods is to indicate LBT & DBTW is enabled/disabled via system information, which is at least for neighbor cell measurement. The third methods is to indicate LBT & DBTW is enabled/disabled via UE-specific RRC signaling, which is at least for SCell addition. * Q3) Additional information needed to be included in MIB to support DBTW, including which bits to re-purpose for the additional information   + values need to be included in MIB and {*subCarrierSpacingCommon,* LSB(s) of *ssb-SubcarrierOffset, dmrs-TypeA-Position*}can be used for indicating values. * Q4) Supported DBTW lengths   + The same values (i.e., 0.5/1/2/3/4/5 ms) with R16 can be the starting point. * Q5) Supported values   + {8, 16, 32, 64} values are preferred. * Q6) Whether to support floating DBTW   + The motivation to introduce floating DBTW is unclear. * Q7) Whether to support mechanism to balance out SSB DTX (from LBT failure)   + Not sure whether any specific mechanism other than DBTW is needed. * Q8) Number of candidate SSB positions (not number of Tx SSBs)   + 64 candidate SSB positions might be enough, but open to discuss whether to define more candidate positions, which depends on the availability of MIB to indicate the increased number of candidate SSB positions. |
| Samsung | 1) We support DBTW for 120/480/960kHz SSB  2) Enabling/Disabling LBT & DBTW can be jointly coded with the indication of Q, since Q is only applicable to LBT & DBTW enabled. The indication can be in MIB if the number of bits are enough, and in SIB1 otherwise. We didn’t see there is an impact on the DCI 1\_0 size.  3) Indicate 4th LSB of SFN in MIB, and reinterpret the 4th LSB of SFN in PHY bits as the 7th LSB of the candidate SSB index.  4) Within 5 ms, and the maximum number of SSB candidate locations for each SCS can be further discussed, based on the indication capacity without increasing PBCH payload size.  5) {1, 2, 4, 8, 16, 32, 64} as the starting point for discussion, and can remove some small values to save the number of bits.  6) “Floating DBTW” needs extra intra indication on the timing offset. Better to clarify its purpose first before discussing other details.  7) Didn’t quite get the intention of the question. We thought supporting DBTW is already a way to balance out SSB DTX (from LBT failure), and no other method is needed.  8) 80 candidate SSB locations for 120 kHz, and up to 128 candidate SSB locations for 480/960 kHz. |
| Huawei, HiSilicon | Q1) Support DBTW for all applicable numerologies.  Q2) To answer this question, three points should be noted:   * 480/960 kHz SSB are supported when SSB location and SCS are explicitly provided to the UE (non-initial access) and SSB does not configure Type-0 PDCCH. Therefore, there is no need to discuss how to indicate enabling/disabling DBTW for 480/960 kHz SSB during initial access as UE does not try to find 480/960 kHz SSB during initial access. * For both cases of initial access and non-initial access UE, when both DBTW length and are known to the UE, UE can infer whether or not DBTW is enabled by comparing DBTW length and values as follows:   + If DBTW length is equal to or smaller than the time duration from the beginning of the half frame to the end of the slot containing the candidate SSB index -1, DBTW is disabled.   + If DBTW length is larger than the time duration from the beginning of the half frame to the end of the slot containing the candidate SSB index -1, DBTW is enabled. * For 120 kHz SSB, if , it means that SSB burst covers the whole 5 ms half frame and SSB burst cant be sliding within DBTW, or, equivalently, DBTW is disabled.   So, to answer Q2, we can provide the following table:  **Mechanism to indicate enabling/disabling DBTW**   |  |  |  | | --- | --- | --- | |  | Initial access | Non-initial access | | 120 kHz SSB | By comparing DBTW length (provided in SIB1) and (Provided in MIB). If , no need to read DBTW length from SIB1 and DBTW is assumed to be disabled. | By comparing DBTW length (provided in SIB1) and (Provided in MIB). Additionally, both DBTW length and are provided using dedicated signaling. | | 480/960 kHz SSB | No need for any mechanism. UE does not support 480/960 kHz SSB | By comparing DBTW length and . Both provided using dedicated signaling. |   Q3) No need to indicate DBTW in MIB. As discussed in Q2:   * For 120 kHz: similar to Rel-16 NR-U, DBTW length is indicated in SIB1 and also using dedicated signaling * For 480/960 kHz: DBTW length is indicated using dedicated signaling.   Q4)  We think that supported DBTW lengths should depend on the SSB pattern design and the supported values for . Otherwise, UE cannot use the comparison between and DBTW length to infer whether or not DBTW is enabled and explicit signaling may be required to indicate DBTW enabling/disabling.  Based on our proposed values for and our proposed SSB pattern, we suggest the following values for DBTW length:   * 120 kHz SCS: {40, 32, 24, 20, 16, 10, 4} slots * 480 kHz SCS: {72, 32, 26, 20, 16, 14, 8, 4} slots * 960 kHz SCS: {64, 32, 26, 20, 16, 14, 8, 4} slots   Q5)  We think supporting would provide enough flexibility in all supported numerologies.  ***Q6)***  This seems to be an optimization with a quite a bit of specification impact. This requires the SSB burst to be potentially not confined in a half frame and spills over to the next half frame. Then we have to discuss the meaning of half frame indicator, discuss how such a spilled-over SSB burst may affect the minimum periodicity of 5 ms (which is in fact the default periodicity in RRC connected state if the SSB periodicity is not explicitly provided), and how the UE may obtain the beginning of frame. We could discuss this later on as a lower priority optimization though  Q7)  In our view, this is also a lower priority optimization. In 120 kHz SCS, if the SSBs with lower candidate indexes are dropped too often due to LBT failure, gNB can always reduce the total number of transmitted SSB indexes and slide the SSB burst within the 5 ms DBTW. The optimization seems to be mainly applicable in the scenario that gNB aims to transmit 64 (or as many as possible SSB indexes) within DBTW.  Q8)  120 kHz: 64 (similar design as in FR2)  480/960 kHz: 128   * Any number above 64 up to 128 needs 7 bits in MIB/PBCH payload. So, we suggest 128 to provide maximum flexibility. |
| Qualcomm | Q1) We do not support introducing DBTW for any supported SCSs in 52.6 – 71 GHz for we do not see obvious benefit.  However, if DBTW was agreed, here are our views for the rest of the questions:  Q2) If the maximum number of candidate SSB positions is 64, enabling/disabling DBTW can be implicitly indicated as part of Q  Q3) Defer details for this until other SSB/CORESET0 related discussions (e.g., mux pattern details, number of CORESET RBs, etc…) are agreed. This can help identify which bits can be repurposed  Q4) Keep DBTW length to be 5 ms maximum for SCS 120 kHz  Q5) The number of values should be minimized (e.g., 2 or 4 max) to support the minimum number of bits (also 64 should be one of the numbers in order to be able to implicitly disable DBTW)  Q6) Not preferrable  Q7) Not preferrable  Q8) Maximum 64 |
| Mediatek | Q1) We are open to discuss it but We do not see the necessity or need of DBTW  Q2) This can be based on using system information for LBT indication (i.e., LBT mode or no LBT mode) discussed in channel access AI.  Q3) Discussion for this question can be deferred, after the value of Q, SSB candidate positions, DBTW on/off is determined, it’s easier to find out bits in MIB that can be repurposed.  Q4) If it’s supported, we prefer to keep it being 5ms  Q5) 4 should be the maximum number of supported values  Q6) We don’t see strong need  Q7) We don’t see strong need  Q8) Maximum 64 SSB candidate positions |
| NEC | Q1)We support DBTW for 120/480/960kHz SSB.  Q2) Because Q value indication is related to the application of DBTW in general, DBTW enabling/disabling state and Q value can be jointly indicated via system information to support UEs performing initial access without any prior information on DBTW and facilitate neighbor cell measurement at least.  Q3) Based on potential decisions about SSB and CORESET#0 multiplexing numerology and pattern, the *subCarrierSpacingCommon,* the LSB of *ssb-SubcarrierOffset* bits and the *MSB of controlResourceSetZero* could be considered to indicate Q value and enabling/disabling DBTW jointly.  Q4) Under the constraint of max 5ms duration, DBTW length can be discussed further depending on the number of candidate SSBs.  Q5) {8, 16, 32, 64} Q values are supported.  Q6) Regarding floating DBTW, additional information for timing offset should be indicated to UE, we suggest to discuss this issue on the basis of results of other questions, such as DBTW length and Q values.  Q7) We prefer not to support the mechanism other than DBTW for improving LBT performance to keep system simplicity.  Q8) If DBTW is supported, up to 80 SSB candidate positions for 120 kHz SCS, and be open to discuss that for 480/960kHz SCS. |
| ZTE, Sanechips | For Q1), support DBTW for all SSB SCSs including 120/480/960kHz.  For Q2), for LBT exempt operation and overlapping licensed/unlicensed bands, it is not necessary to enable/disable the DBTW by explicit signaling. The impacts on LBT exempt operation brought by DBTW can be eliminated by configuration implementation, e.g. configuring a length of DBTW to match the duration of 64 SSBs.  For Q3), it can be discussed after SCSs/configuration of SSB and CORESET#0 are determined.  For Q4), the values for DBTW lengths in Rel-16 NR-U can be the starting point. More smaller values can be considered as SCSs are also smaller.  For Q5), in order to reduce the number of bits indicating Q value, four candidate values for Q are preferred, such as {8,16,32,64}. If more bits are available, we are open to support more values of Q.  For Q6), more discussion is needed to illustrate its necessity.  For Q7), it seems no necessity to support any mechanisms other than DBTW.  For Q8), in order to reduce the impact of standardization caused by indicating candidate SSB indices, the maximum number of candidate SSB defined in the half-frame can be kept unchanged (maintain 64) or limited to 128 for 240/480/960 kHz SSB SCS |
| Nokia | Q1) We would propose to support DBTW for all, 120kHz/480kHz/960kHz.  Q2) As DBTW could affect the monitoring time needed for initial cell selection, we would propose to separate these by SS-raster locations. This maybe bit pending on the Channel Access discussions, i.e. if we can assume that when DBTW is not enabled, LBT can be enabled. If DBTW presence is indicated via SS-raster location, and we can in this case always assume that LBT is enabled, we would need to be able to be explicitly indicate if LBT is used only when DBTW is not enabled. Thus it would be possible to use/share the bits used for DBTW support (SSB candidate location relation).  Q3) As we do not have sufficient number of alternative candidate locations for all the SSBs at 120kHz scs, if number of SSBs is larger than 32, the NR-U (Q) based mechanism does not seem feasible. Therefore, we think that we should be able to directly indicate in the SSB whether it is a re-transmission of a given SSB for example:   * *subCarrierSpacingCommon* indicates whether or not detected SSB is in additional position   + *subcarrierSpacingCommon* may be obsolete parameter in the frequency range of interest because Type0-PDCCH is likely to use the same SCS as the SSB * SSB index signaled using PBCH DMRS and MSB bits in the PBCH physical layer bits signals the actual SSB index when the SSB is transmitted in the additional position * *k*SSB bits are repurposed so that the UE can determine the received SSB position within the group of additional positions. I.e. possible re-transmission locations are grouped so that e.g. SSB#0 can be re-transmitted on certain additional positions.   Similar mechanism could also be adopted for 480kHz and 960kHz SSBs.  Q4) For 120kHz, 5ms window can be assumed, but for 480kHz and 960kHz shorter time could be considered. The final value would depend on the SSB pattern design, and number of additional candidate locations supported.  Q5) As noted in Q3, we don’t think the NR-U based method is feasible in most scenarios due to limited number of additional candidate locations at least for 120kHz.  Q6) Unless I’m mistaken, the floating approach would mean that the actual DBTW window time from UE perspective is increased. Not sure if that is preferable/according to the earlier agreements.  Q7) We think that this is needed, for both, DBTW and possible for the short control signaling exemption for 120kHz. In case of DBTW the possible candidate locations for retransmission could be shared in time multiplexing manner so that part of the time re-transmission is allowed for certain SSBs.  Q8) If we introduce the additional candidate locations between the SSB bursts, 80 candidate locations could be supported. If no additional positions are supported, we should enable using the positions not used by ‘actually transmitted SSBs’ to be used as candidate locations. For 480kHz and 960kHz, we are open to discuss whether we need to support full range of 128 positions. |
| Xiaomi | Q1) Support the DBTW for the SCSs agreed  Q2) By system information or implicitly by Q value.  Q3) FFS.  Q4) Yes, values smaller than 5ms can be discussed and defined for 480kHz/960kHz.  Q5) Yes, at least {8,16,32,64} should be supported, others can be FFS.  Q6) No, we prefer not, but we are open at current stage.  Q7) Not preferable.  Q8) Maximum 64. |
| OPPO | Q1) Support DBTW for 120/480/960kHz SSB  Q2) Support enabling/disabling LBT & DBTW, details can be further discussed.  Q3) Agree that additional information e.g., QCL indication, needed to be included in MIB to support DBTW.  Q4) Supported the same DBTW lengths as NR-U (i.e., 0.5/1/2/3/4/5 ms)  Q5) Supported values {16, 64}  Q6) Don’t support floating DBTW  Q7) Don’t support other mechanisms to balance out SSB DTX (from LBT failure)  Q8) Maximum number of candidate SSB positions is 64 |

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| Futurewei | Q1) We support to introduce DBTW for all the supported SCSs in 52.6 – 71 GHz.  Q2) It can be associated with LBT on/off switching and/or if (based on Short Control Signaling case) LBT is necessary for DB.  Q3) We prefer not to have any additional information in MIB for DBTW purpose.  Q4) We prefer to keep it as maximum 5ms, the existing values from Rel-16 are acceptable.  Q5) Four candidates are preferred {8,16,32, 64} for Q. We are OK to further discuss if more additions are necessary.  Q6) We do not see the necessity.  Q7) We do not see the necessity for functionality other than DBTW.  Q8) We prefer 64 as the maximum number SSB for 120kHz SCS, and Ok with further study for other SCS values. |
| Lenovo, Motorola Mobility | Q1) Support DBTW for all SCS of SSB since LBT could be mandatory regardless of the SCS value.  Q2) Enabling and disabling the DBTW can be implicitly based on the LBT mode or no-LBT mode/short control signaling exemption.  Q3) Agree with Qualcomm, the discussion on the details of which bit information to be/how to be used can be postponed after multiplexing patterns of SSB and CORESET0 details are agreed  Q4) Support Rel-16 NR-U 5ms as a starting point, discuss further the need to have shorter lengths for 480/960kHz which depend also on the agreements on the SSB patterns as well.  Q5) Support {8, 16, 32, 64}  Q6) Not preferred  Q7) We don’t see a need for supporting it  Q8) 64 candidate SSB positions, open to discuss larger values based on the availability of the required extra bits in MIB payload |
| Interdigital | Q1) We support DBTW for all supported SCS for SSB.  Q2) The enabling/disabling of the DBTW can be associated with a specific sync raster offset, where sync raster offsets within a specific range imply that DBTW is enabled and the sync raster offsets outside the range imply that DBTW is disabled.  Q3) The parameters that may be unused in MIB can indicate the enabled/disabled DBTW. For instance, there might be some unused bits in *searchSpaceZero* or *controlResourceSetZero* in *pdcch-ConfigSIB1* that can be interpreted/re-purposed as the indication for the enabled/disabled DBTW.  Q4) We support the settings for the DBTW to be the same as Rel-16 NR-U.  Q5) We support using a subset of the possible values, e.g., {4,8,32,64} or {8,16,32,64}, to limit the indication of the Q parameter to two bits. |
| CATT | Q1) We support to DBTW for 120khz, for 480kHz/960kHz we think since the duty cycle is less than 10% there’s no need to introduce DBTW.  Q2) It can be indicated via system information.  Q3) Information in MIB can be repurposed for DBTW purpose. It will depend on the result of the discussion for SSB/CORESET#0 configuration.  Q4) Maximum 5ms .  Q5) We are Ok with {8,16,32, 64}  Q6) We do not see the necessity.  Q7) We do not see the necessity for functionality other than DBTW.  Q8) We prefer 80 for 120kHz SCS. |
| Intel | Q1) Support DBTW for 120/480/960kHz SSB  Q2) Explicit or implicit signalling in MIB. Alternatively, explicit signalling in SIB1.  Q3) Certainly, no changes should be applied to MIB size. Some of MIB and/or PBCH payload bits certainly could be repurposed after discussing availability of CORESET#0 configuration in SSB.  Q4) A single fixed DBTW length, e.g., 5 ms, is preferred to avoid configuration signalling.  Q5) The set of possible values should be limited to 2 or 4 values to minimize the number of signalling bits needed. The exact values of are FFS.  Q6) The floating DBTW is an alternative solution which does not require changes in ordering of SSBs (within the DBTW). It relies on using both halves of radio frame for SS burst transmission. It could be supported if no additional candidate SSB positions could be found within a fixed DBTW. In this case, some changes in RRM measurement gaps seem to be needed.  Q7) Consider supporting a mechanism to balance out SSB DTX if DBTW is not supported.  Q8) In case of DBTW, the number of candidate SSB positions should be increased. At least 80 candidate SSB positions could be considered for SCS 120 kHz. |
| vivo | Q1) Support DBTW for all applicable SCS  Q2) Three methods can be used to indicate whether there is DBTW:   * Alt. 1: Frequency band (licensed or un-licensed); * Alt. 2: The indicator in PBCH; * Alt. 3: The design of SSB sequence (PSS, SSS and DMRS).   Q3) The additional bits can from ‘*subCarrierSpacingCommon’* or‘*pdcch-ConfigSIB1’*  Q4) The DBTW length can be depended on the different SCS. Such as, the lengthe of DBTW is 0.5/1/2/3/4/5ms and 0.125/0.25/0.5/0.75/1/1.25ms under 120K SCS and 480K SCS respectively.  Q5) The supported values can be {8,16,32,64}, two methods can be used to indicate the value of Q:   * Alt. 1: Specify the value of Q for each SCS; * Alt. 2: Utilize the bits in PBCH;   Q6) No support  Q7) No support  Q8) 120 kHz: 64; 480/960 kHz: 128 |
| Ericsson | Q1) We do not support DBTW for any of 120/480/960 kHz SSB  However, we provide input on the remaining questions in case there can be consensus to support. We have a strong concern that there are quite a few details that need to be worked out before feasibility can be assessed and a decision can be made on support/no support.  Q2) A reserved value of Q (e.g., Q = 64) can be used to indicate DBTW on/off  However, before support of DBTW can be decided, it needs to be decided how to indicate LBT on/off. In the GTW it was agreed to discuss this in the channel access AI. The reason for the dependency is that the size of DCI 1\_0 with CRC scrambled by SI-RNTI (i.e., the Type0-PDCCH used to schedule PDSCH carrying SIB1) has a different size depending on shared/non-shared spectrum (see highlighted sentence in below extract from 38.212 Section 7.3.1.2.1. Hence two alternatives for handling this are:   1. the UE does 2 blind decodes assuming the 2 different sizes 2. LBT on/off is indicated in MIB so that the UE can avoid 2 blind decodes   Clearly, if solution (2) is adopted, one bit needs to be found in MIB for indicating LBT on/off in addition to bits for Q.  --- Extract from 38.212 Section 7.3.1.2.1 ---  The following information is transmitted by means of the DCI format 1\_0 with CRC scrambled by SI-RNTI:  - Frequency domain resource assignment – bits  -  is the size of CORESET 0  - Time domain resource assignment – 4 bits as defined in Clause 5.1.2.1 of [6, TS38.214]  - VRB-to-PRB mapping – 1 bit according to Table 7.3.1.2.2-5  - Modulation and coding scheme – 5 bits as defined in Clause 5.1.3 of [6, TS38.214], using Table 5.1.3.1-1  - Redundancy version – 2 bits as defined in Table 7.3.1.1.1-2  - System information indicator – 1 bit as defined in Table 7.3.1.2.1-2  - Reserved bits – 17 bits for operation in a cell with shared spectrum channel access; otherwise 15 bits  --- End extract ---    Q3) No additional information other than Q and LBT on/off is needed. As previously agreed, the PBCH payload should remain the same as Rel-16. It is not clear which bits could potentially be repurposed. The (SSB,CORESET0) SCS combinations are not yet known; it seems clear that all 4 bits are needed for signaling k\_SSB (12 values) unless RAN4 designs a very specialized sync raster; and the CORESET0 configuration table is not yet decided.  Q4) No more than 5 ms (as previously agreed).  Q5) It seems that at least 4 values are needed, e.g., Q = 8, 16, 32, 64, where Q = 64 indicates DBTW on/off  Q6) "Floating DBTW" is a new concept which has not been previously discussed. Not clear of the motivation, and seems to be a departure from Rel-16. Not preferrable to specify a new approach from the perspective of reuse of implementations.  Q7) Not clear; not preferred.  Q8) No more than Q = 64 since that is what Rel-15 PBCH is able to signal today with 6 bits (3 bits from DMRS sequence and 3 bits from PBCH payload). |
| Sony | Q1) we support DBTW for all supported SCS.  Q2) we support enabling/disabling LBT & DBTW. Enabling/disabling DBTW and Q could be jointly indicated via system information.  Q3) Although the detailed discussion which bits to be used should be postponed until SSB/CORESET#0 related discussion is agreed, *subCarrierSpacingCommon*, LSB of *ssb-SubcarrierOffset*, and *controlResourceSetZero* in MIB could be candidate bits to indicate DBTW related parameters.  Q4) Maximum 5 msec should be baseline. We can further discuss small length for 480 kHz and 960 kHz SCS.  Q5) {1, 2, 4, 8, 16, 32, 64} as starting point and some small values could be removed to save bits.  Q6) we don’t support floating DBTW because it causes increasing detection complexity and large spec impact.  Q7) we don’t see necessity to support the mechanism other than DBTW.  Q8) 80 candidate SSB locations for 120 kHz SCS. Up to 128 candidate SSB location for 480 and 960 kHz SCS. |
| WILUS | Q1) Support DBTW for all applicable SCS  Q2) Explicit or implicit signaling in MIB. Alternatively, explicit signaling in SIB1.  Q3) Prefer not to have any additional information in MIB for DBTW purpose  Q4) Prefer to have a single fixed DBTW length to avoid configuration signaling.  Q5) The number of supported values to minimize required signaling bits as 1 or 2 bits should be limited.  Q6) We are not clear to support this, but we are open to discuss whether or not support “Floating DBTW”.  Q7) Support mechanism to balance out SSB DTX from LBT failure.  Q8) In case of DBTW, the number of candidate SSB positions should be increased. At least 80 candidate SSB positions could be considered for SCS 120 kHz. |
| Spreadtrum | Q1) Support DBTW for all applicable SCS  Q2) Implicit or explicit indication in MIB  Q3) Strive to not introduce new bit in MIB |

#### **1st Round Discussion Summary:**

Summary of responses from companies are provided below.

* Q1) Whether or not to support DBTW for 120/480/960kHz SSB
  + Support: Docomo, LGE, Samsung, Huawei, HiSilicon, NEC, ZTE, Sanechips, Nokia, NSB, Xiaomi, OPPO, Futurewei, Lenovo, Motorola Mobility, Interdigital, CATT (for 120kHz), Intel, Spreadtrum
  + Do not support: Qualcomm, Mediatek, CATT (for 480/960kHz), Ericsson
* Q2) Mechanisms to support enabling/disabling LBT & DBTW, including DCI 1\_0 size issue and where to signal enable/disable (if supported)
  + Indicate via : Samsung, Qualcomm, NEC, Xiaomi
  + Distinct GSCN values for LBT cases & non-LBT cases: LGE, Nokia, NSB, Interdigital
  + Indicate via SI: LGE, Mediatek
  + Indicate via MIB: Interdigital, CATT, Intel, Spreadtrum
  + Indicate via UE specific RRC: LGE
  + Indicate by combination of and DBTW lengths: Huawei, HiSilicon (assume means DBTW is disabled)
  + Indication not needed: ZTE, Sanechips
  + Tied to LBT on/off: Lenovo, Motorola Mobility, Futurwei
  + FFS: OPPO
  + Indication in MIB will be needed to avoid double blind detection of DCI sizes: Ericsson
* Q3) Additional information needed to be included in MIB to support DBTW, including which bits to re-purpose for the additional information
  + No need for additional information in MIB: Docomo, Huawei, HiSilicon, Futurewei, Spreadtrum
  + : LGE, NEC, Samsung, OPPO, Ericsson (if DBTW is supported)
  + FFS: Qualcomm, Mediatek, ZTE, Sanechips, Xiaomi, Lenovo, Motorola Mobility
  + Additional SSB position: Nokia, NSB
  + Enable/disable DBTW: CATT, Ericsson (if DBTW is supported)
* Q4) Supported DBTW lengths
  + Same as NR-U (0.5/1/2/3/4/5 msec): Docomo, LGE, ZTE, Sanechips, OPPO, Futurewei, Lenovo, Motorola Mobility, Interdigital
  + {1,2,4,8,16,32,64}: Samsung
  + {40, 32, 24, 20, 16, 10, 4} slots for 120kHz, {72, 32, 26, 20, 16, 14, 8, 4} slots for 480kHz, {64, 32, 26, 20, 16, 14, 8, 4} slots for 960kHz: Huawei, HiSilicon
  + Max 5 msec: Qualcomm, CATT, Ericsson (if DBTW is supported)
  + 5msec: Mediatek, NEC, Nokia, NSB, Intel
* Q5) Supported values
  + Same values as in NR-U: Docomo
  + FFS: Samsung
  + {8,16,28,32,40,52,64}: Huawei, HiSilicon
  + Max 2 or 4 values: Qualcomm (include 64 at least), Intel
  + Max 4 values: Mediatek
  + {8,16,32,64}: NEC, ZTE, Sanechips, Xiaomi, Futurewei, Lenovo, Motorola Mobility, Interdigital, CATT, Ericsson (if DBTW is supported)
  + {4,8,32,64}: Interdigital
  + {16, 64}: OPPO
* Q6) Whether to support floating DBTW
  + Do not support: Docomo, LGE, Qualcomm, Mediatek, ZTE, Sanechips, Nokia, NSB, Xiaomi, OPPO, Futurewei, Lenovo, Motorola Mobility, CATT, Ericsson
  + Further clarification needed: Samsung, NEC
  + FFS: Huawei, HiSilicon
  + If additional candidate SSB position not available: Intel
* Q7) Whether to support mechanism to balance out SSB DTX (from LBT failure)
  + Support: Nokia, NSB, Intel (if DBTW is not supported)
  + Do not support: Docomo, LGE, Qualcomm, Mediatek, NEC, ZTE, Sanechips, Xiaomi, OPPO, Futurewei, Lenovo, Motorola Mobility, CATT, Ericsson
  + FFS : Huawei, HiSilicon
* Q8) Number of candidate SSB positions (not number of Tx SSBs)
  + FFS: Docomo
  + 64: LGE (open for further discussion), Qualcomm, Mediatek, Xiaomi, OPPO, Lenovo, Motorola Mobility, Ericsson
  + 64 for 120kHz: Huawei, HiSilicon, Futurewei
  + 80 for 120kHz: Samsung, NEC, Nokia, NSB, CATT, Intel
  + 128 for 480/960kHz: Samsung, Huawei, HiSilicon, Nokia, NSB

#### **2nd Round Discussion:**

From the discussions, three companies commented DBTW is not needed (one company commented DBTW for 480/906kHz is not needed), and larger number of the companies think DBTW would be needed. Moderator suggests focusing on getting further progress with the direction that DBTW are to be supported. Moderator has formulated a proposal that could be used for further discussions.

##### **Proposal 1.3-1)**

* Support DBTW for 120/480/960kHz SSB
  + Enable/disable of DBTW is indicated by one or more of the following methods:
    - Option 1) signaling in MIB
      * Option 1-1) indicated by a specific state/index of
      * Option 1-2) indicated by other bit fields in MIB
      * FFS: between option 1-1 and 1-2.
    - Option 2) distinct GSCN used by the SSB
    - FFS: whether to support option 1, 2, or both.
    - Note: enable/disable signaling of DBTW by MIB or GSCN does not preclude other signaling methods
  + MIB to support signaling of
    - Total number of valid values of to not exceed 4
    - Working assumption: {[8], [16], [32], [64]}
      * FFS: on whether can be used to disable DBTW
  + Support DBTW lengths:
    - 0.5, 1, 2, 3, 4, 5 msec
      * Note: same as Rel-16 FR1 NR-U
  + Number of candidate positions when DBTW is enabled
    - For 120kHz SSB
      * FFS: between 64 or 80
    - For 480/960kHz SSB
      * FFS: between 64 or 128
  + FFS:
    - Whether or not to support floating DBTW
    - Whether or not to support mechanism to balance out SSB DTX (from LBT failure)

One question from moderator on option 1-1 is that if 1 state is used to indicate disabling of DBTW in , does this mean if 2 bits are used for only 3 valid values and 1 state for disable exist?

Also please comment further on how to deal with DCI format size difference if DBTW is used (issue Ericsson brought up). Moderator assumes support of option 1-1 or 1-2 should resolve this issue, but would like to receive comments form companies.

Please note the proposal is just a starting point for focus for further discussions. Please comment further on how the proposal should be updated. If there are better alternatives, please provide them.

|  |  |
| --- | --- |
| **Company** | **Comment** |
| Samsung | We are in general ok with the proposal, with some comments for the details:   * has its particular operation to decide the SSB index, so it would not be proper to say one index of is used for indicating DBTW is disabled. One alternative way of expressing the option could be jointly coding DBTW disabling with , e.g. {16, 32, 64, DBTW disabled}. * The current options for indicating DBTW disabling and enabling is only for initial access case, and there should be options for indicating using RRC parameter for non-initial access. If the common understanding is to discuss that later, we are ok. * The whole bullet of using MIB to indicate should be working assumption, since we don’t know whether enough bits can be re-interpreted for this purpose yet. * The value of may depend on which option adopted in Option 1, e.g. 3 valid value or 4. The valid values should also be further discussed, since if 64 is maximum number of candidate SSB, then we may not need 64 for .   For moderator’s question, yes, that’s our understanding.  Based on the comment above, we have the following suggestions for the proposal:   * Support DBTW for 120/480/960kHz SSB   + Enable/disable of DBTW is indicated by one or more of the following methods:     - Option 1) signaling in MIB       * Option 1-1) ~~indicated by a specific state/index of~~ disabling DBTW is jointly coded with       * Option 1-2) indicated by other bit fields in MIB       * FFS: between option 1-1 and 1-2.     - Option 2) distinct GSCN used by the SSB     - FFS: whether to support option 1, 2, or both.     - Note: enable/disable signaling of DBTW by MIB or GSCN does not preclude other signaling methods   + Working assumption: MIB to support signaling of     - Total number of valid values of to not exceed 4     - ~~Working assumption: {[8], [16], [32], [64]}~~   + Support DBTW lengths:     - 0.5, 1, 2, 3, 4, 5 msec       * Note: same as Rel-16 FR1 NR-U   + Number of candidate positions when DBTW is enabled     - For 120kHz SSB       * FFS: between 64 or 80     - For 480/960kHz SSB       * FFS: between 64 or 128   + FFS:     - Whether or not to support floating DBTW     - Whether or not to support mechanism to balance out SSB DTX (from LBT failure) |
| Qualcomm | If DBTW is to be supported, we think that it should only apply to 120 kHz SCS. The higher SCSs (480/960 kHz) clearly can support the short control signal exemptions and do not need LBT. Adding DBTW to these SCSs will add more un-necessary complexity and specification efforts. |
| LG Electronics | We are generally fine with moderator’s proposal. But, we don’t support adding the last two FFS points, which are unclear and not supported by majority companies. So, we would suggest to remove the last FFS (i.e., Whether or not to support floating DBTW and Whether or not to support mechanism to balance out SSB DTX (from LBT failure)).  Regarding its applicability to 480/960 kHz SCSs, we’d like to know if all of regional regulations mandating LBT procedure in 60 GHz provide short control signal exemption rule. If not, it seems necessary to apply DBTW to 480/960 kHz SCS as well. |

#### **2nd Round Discussion Summary:**

TBD

### 2.1.4 SSB Resource Pattern

* From [2] Huawei, HiSilicon:
  + Other than the agreed values of n corresponding to Cased D SSB pattern, do not support any additional values of n for SSB with 120kHz SCS in operation with shared or without shared spectrum.
  + Support following patterns for SSB with 480 kHz and 960 kHz SCS:
    - For operations without shared spectrum:
      * {2,8}+14n, (n=0,1,2,…,31) for both 480 kHz and 960 kHz SCS
    - For operations with shared spectrum:
      * {2,8}+14n, (n=0,1,2,…,31,40,…,71) for 480 kHz SCS;
      * {2,8}+14n, (n=0,1,2,…,63) for 960 kHz SCS.
* From [3] vivo:
  + Support of additional n values to support of DBTW, and the value of n can be 4, 9, 14, 19.
  + Support to reuse case D as the baseline for designing the SCS 480 kHz and 960 kHz time domain pattern.
  + The following alternatives could be considered to solve beam switching problem for contiguous candidate SSBs:
    - Alt. 1: New SSB pattern introducing gaps between contiguous candidate SSBs;
    - Alt. 2: The same QCL assumptions for contiguous candidate SSBs;
* From [4] Spreadtrum:
  + If the symbol gap between SSB positions is agreed to be supported, the SSB pattern of Case A/C for SSB with 15/30kHz SCS can be considered for SSB with 480/960kHz SCS.
* From [5] Nokia, NSB:
  + Define additional SSB locations for the purpose of SSB retransmissions
  + Group additional SSB locations and associate each group to set of regular SSB positions, e.g. after each block of 16 regular SSB positions there is associated group of up to four additional positions that can be used to retransmit any of the associated actual SSBs.
  + For carrier frequencies within 52.6 GHz to 71GHz, at 120kHz SSB, introduce additional candidate locations for SSB transmission support for 𝑛 = 4, 9, 14, 19.
    - The first symbols of the additional candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n.
  + For carrier frequencies within 52.6 GHz to 71GHz, at 240kHz SSB, introduce additional candidate locations for SSB transmission support for 𝑛 = 10, 11, 12, 13, 15, 16, 17, 18.
    - The first symbols of the candidate SS/PBCH blocks have indexes {8, 12, 16, 20, 32, 36, 40, 44} + 56×n.
* From [6] Ericsson:
  + For SS/PBCH block with 120 kHz SCS, support Case D pattern as defined in Rel-15. No new values of n are supported.
  + Pending decision from RAN4 on beam switching times, if beam switching can be performed within the cyclic prefix, support the FR2 Case D pattern for time domain pattern for SSB transmissions with 480 kHz and 960 kHz SCS.
* From [7] CATT:
  + More than 64 SSB transmission opportunities shall be defined within a 5ms SSB burst set to support up to 64 beams for SSB beam sweeping in case of occasional LBT failure. The issue of supporting additional bit(s) for the extension of SSB candidate index needs further study.
  + Additional n value such as #4, #9, #14, and #19 can be used for new SSB candidates if LBT/DBTW is needed for SSB transmission.
* From [8] Qualcomm:
  + for the SSB for NR operation in the frequency between 52.6GHz and 71GHz and SCS = 480 kHz and 960 kHz, consider defining an SSB pattern consisting of multiple “SSB slots” where SSB symbols for one or more beams are contained in the “SSB slot”
    - A beam switching gap of 1 symbol is inserted between SSBs within the “SSB slot”
    - Additional control symbols may be defined in the SSB slots with beam switching gaps between control and SSB symbols of different beams
    - Additional “gap slots” may be inserted between “SSB slots” to account for URLLC and UL traffic
    - Consider the option of aligning the higher SCS SSBs with the corresponding beams for the lower SCS SSB
* From [9] OPPO:
  + Wait for RAN4 response before further discuss beam switching gap issue.
* From [10] ZTE, Sanechips:
  + For designing SSB patterns with different SCSs for NR operation above 52.6 GHz, it is proposed to reuse the existing design (i.e. Case A/C, Case B/D and Case E) as much as possible, and take different impacts in single/mixed numerology operation into account.
  + The following options can be considered for supporting beam switching for SSB with SCS 480 kHz and 960 kHz if the CPs can not used to support beam switching and other functions simultaneously.
    - Option 1: In a half-frame, any two candidate SSBs are discontinuous in the time domain
    - Option 1-1: SSB pattern with SCS 480/960 kHz can adopt the existing pattern of Case A and Case C in one or two slots defined in Rel-15 NR
    - Option 1-2: SSB pattern with SCS 480/960 kHz should be re-designed to reserve at least one symbol between any two candidate SSBs, e.g. only defining one candidate SSB per slot, or shift the existing SSB by one or more symbols
    - Option 2: Multiple adjacent candidate SSBs are defined to have a same SSB index or QCL assumption
  + In order to reduce the impact of standardization caused by indicating candidate SSB indices, the maximum number of candidate SSB defined in the half-frame can be kept unchanged (maintain 64) or limited to 128 for 240/480/960 kHz SSB SCS.
* From [11] Intel:
  + Consider SSB pattern in a slot with 3 SSB containing slots, each slot with 2 SSB position, followed by 1 non-SSB carrying slot for 480 kHz and 6 SSB carrying slots followed by 2 non-SSB carrying slots for 960kHz, to accommodate Rx-Tx switching gap.
    - For 480kHz and 960kHz SCS based SSB, first symbols of the candidate SSB have indexes {2,9} + 14×n, where index 0 corresponds to the first symbol of the first slot in a half-frame.
    - For 480kHz, n = 0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 32,33,34, 36,37,38, 40,41.
    - For 960kHz, n = 0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40, 41.
* From [13] Apple:
  + Support to introduce a unified SSB Pattern for 480kHz SCS and 960kHz SCS (if supported):
    - The first symbol of candidate SSB have indexes {2,9,16,23} within each SSB burst.
    - Reserve 2 slots for DL/UL and UL/DL switching to allow for fast UL transmission between two SSB bursts.
* From [15] NEC:
  + Additional n values of 4, 9, 14 and 19 should be supported to indicate additional candidate SSBs in DBTW at least for 120 kHz SCS SSB pattern.
  + The indication of additional candidate SSBs based on additional n values should be investigated.
* From [16] Samsung:
  + Support the same SS/PBCH block pattern for 480 kHz and 960 kHz SCSs.
    - At least one symbol should be reserved between neighboring SS/PBCH block for beam sweeping delay.
    - Symbols should be reserved for CORESET and HARQ with SCS same as the SS/PBCH block.
    - For SS/PBCH block candidate locations in a slot, Case A or Case C can be reused.
* From [18] LGE:
  + Reuse existing SS/PBCH Case D (which is applied for 120 kHz SCS) for SS/PBCH block with 480/960 kHz SCS, if RAN4 confirms that no explicit switching gap is needed between successive SS/PBCH blocks.
  + Support of additional n values for the time domain pattern of SS/PBCH block with 120 kHz SCS can be considered to increase SS/PBCH block’s transmission opportunities, only if PBCH payload is sufficient to indicate the increased number of candidate SS/PBCH block indexes.
* From [19] Lenovo, Motorola Mobility:
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, if higher subcarrier spacings (numerologies) are adopted for SSB, then to allow the beam switching between contiguous SSBs, a gap (for example a symbol gap or post prefix) should be supported before beam switching.
* From [21] Interdigital:
  + Introduce the enhancements on SS/PBCH block transmission patterns to deliberately include the CORESET#0 and SIB1 in fixed time locations along with the corresponding SS/PBCH block to ensure the channel occupancy as much as possible, in the initial access operations for unlicensed spectrum in beyond 52.6GHz.
* From [22] Convida:
  + Increasing the number of SSB candidate positions to above 64 to increase transmission opportunities to cope with LBT failure should be considered.
* From [23] Sharp:
  + Based on SSB resource pattern Case D of FR2, other values of n (e.g., 4, 9, 14, 19) should be added for the SSB with 120kHz SCS in above 52.6GHz.
* From [25] NTT Docomo:
  + When new SCSs are supported for SSB, the two alternatives below can be considered for SSB mapping in time domain:
    - Two SSBs per slot, with guard period of at least 1 symbol between the SSBs
    - One SSB per slot
* From [27] WILUS:
  + At least one symbol gap in time domain between SS/PBCH blocks with different SSB indices should be considered for higher subcarrier spacing (e.g., 960kHz) by taking a beam switching gap into account due to a RF interruption time of Tx/Rx beams and/or LBT gap in unlicensed spectrum.

#### Summary of Discussions

* Several companies stated that RAN1 should wait for RAN4 reply LS on beam switching before deciding the exact SSB patterns.
* If exact SSB position within a slot(s) is difficult to conclude due to lack of information from RAN4, moderator suggests to discuss and conclude on other aspects of SSB pattern that do not require feedback from RAN4. For example:
  + number of SSB candidates per slot
  + slots that may contain candidate SSB(s) (including maximum number of candidate SSB in half-radio frame)

#### **1st Round Discussion:**

Based on input Moderator has put together possible options for SSB resource pattern.

* For 120kHz SSB:
  + Whether or not to add n = 4, 9, 14, 19 for the SSB candidate position
* For 480kHz SSB:
  + SSB candidate position defined over
    - Option 1-1) 1 slot (e.g. start position defined as {X,Y} + 14\*n)
    - Option 1-2) 2 consecutive slots (e.g. start position defined as {W,X,Y,Z} + 28\*n)
  + Assuming {X,Y} + 14×n, SSB candidate position, support
    - Option 2-1) n = 0,1,2,…,31
    - Option 2-2) n=0,1,2,…,31,40,…,71 (applicable only for unlicensed cases)
    - Option 2-3) n = 0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 32,33,34, 36,37,38, 40,41.
* For 960kHz SSB:
  + SSB candidate position defined over
    - Option 3-1) 1 slot (e.g. start position defined as {X,Y} + 14\*n)
    - Option 3-2) 2 consecutive slots (e.g. start position defined as {W,X,Y,Z} + 28\*n)
  + Assuming {X,Y} + 14×n, SSB candidate position, support
    - Option 4-1) n = 0,1,2,…,31
    - Option 4-2) n=0,1,2,…,63 (applicable only for unlicensed cases)
    - Option 4-3) n = 0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40, 41.

Given that there are many options, moderator suggest starting out by answering some fundamental questions (as suggested by few companies)

* For 120kHz:
  + Q1) Whether or not to add n = 4, 9, 14, 19 for the SSB candidate position for unlicensed operation
* For 480 and 960 kHz:
  + Q2) same SSB resource pattern within pair of consecutive slots?
  + Q3) 1 SSB per slot or 2 SSB per slot
  + Q4) same number of candidates depending on mode of operation (e.g. licensed and unlicensed or depending on LBT on or off)?
  + Q5) if different number of SSB candidates depending on mode of operation, SSB resource pattern for licensed/no LBT case a complete subset of the other case (i.e. value of n for one mode all included in the other mode)?
  + Q6) should there be non-SSB slots every few SSB containing slots (i.e. non-consecutive values of n) to support intermittent UL or other transmissions than SSB?

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| **Company** | **Comment** |
| DOCOMO | Q1) It seems related to DBTW, so should be discussed there.  Q2)  Q3) We support 1 SSB per slot since it has some benefits, e.g., relaxing beam sweeping overhead and resource utilization efficiency. 1 SSB per slot can achieve more resources available for other transmissions with the same beam within the slot. Also, the time required to complete beam sweeping will not be a significant issue since slot length is shortened with larger SCS.  Q4) It may depend on if DBTW is supported, but we basically think the same number of SSB candidates would be sufficient.  Q5) Yes.  Q6) We support to consider non-SSB slots. Its periodicity would need to be discussed further. |
| LG Electronics | For 120 kHz, we prefer not to add n = 4, 9, 14, 19 for the SSB candidate position for unlicensed operation. But adding n = 4, 9, 14, 19 can be considered if we can find bit location to indicate the increased SSB candidate position.  For 480/960 kHz, we have NOTE (Strive to minimize specification impact due to the new SCS for SSB) in the previous agreement. In that sense, we suggest legacy pattern (e.g., Case D) as the starting point. |
| Samsung | 1) Yes, if DBTW is supported for 120 kHz SSB.  2) Yes.  3) 2 SSB per slot  4) No, the number of candidate SSB locations for unlicensed band can be larger.  5) Yes, the candidate SSB locations for licensed band can be a subset of the ones for unlicensed band.  6) Yes, for licensed band. |
| Qualcomm | * For 120kHz:   + Q1) To allow for UL and URLLC traffic, do not add additional SSB candidate positions * For 480 and 960 kHz:   + Q2)   + Q3) Depending on the CORESET0/SIB1 multiplexing with SSB discussion (if SIB1 can be TDMed with SSB and CORESET0 in the same slot, then 1 SSB per slot can used). We can discuss SSB/CORESET0/SIB1 multiplexing patterns first   + Q4) Yes   + Q5) Same pattern for licensed and unlicensed   + Q6) Yes |
| Sharp | * For 120kHz:   + Q1) Yes * For 480 and 960 kHz:   + Q6) Yes |
| Mediatek | * + Q1) Do not add additional positioins   + Q2) yes   + Q3) 2 SSB per slot, but we are open to discuss.   + Q4) yes   + Q5 Prefer to use same pattern   + Q6) yes |
| ZTE, Sanechips | For Q1), we are open to add n = 4, 9, 14, 19 to increase candidate SSB positions if no other issues are raised.  For Q2), yes.  For Q3), 2 SSBs per slot are preferred.  For Q4), for cases in unlicensed or with LBT on, more candidate SSB can be defined than that of cases in licensed or with LBT off.  For Q5), yes.  For Q6), yes. |
| Nokia | Q1) If DBTW is supported, we would prefer to add additional positions (n = 4, 9, 14, 19)  Q2) We think that the SSB locations could be identical in all slots where SSBs are transmitted as it is not likely that symbols for UL transmission can be fitted in the slot due to DL-UL switching time.  Q3) We would support 2 SSBs per slot, but we are open to discuss e.g. based on RAN4 feedback on beam switching gap, or LBT gap.  Q4) If DBTW is supported, we would think that additional candidate locations would be preferred. We are open to discuss, whether we assume full set (64+64) or if fewer are supported. For no DBTW, only 64 are needed.  Q5) Yes, sub-set is preferred due to simplicity.  Q6) Yes, the period at which the UL slots would appear can be further discussed once RAN4 has concluded the UL-DL switching gap. |
| Xiaomi | Q1) n = 4, 9, 14, 19 is not preferred.  Q2) Yes  Q3) 2 SSB per slot  Q4) Yes  Q5) Same pattern is preferred.  Q6) Yes |

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| Huawei, HiSilicon | Q1) No. Reserve them for UL Tx as in Rel-15/16. DBTW for 120 kHz SSB can still be supported if Q<64.  Q2) Yes (of course, unless the slot is reserved for UL Tx).  Q3) 2 SSB per slots that are not reserved for UL Tx  Q4) No. Number of candidates for unlicensed band should be higher than the number of candidates for licensed band  Q5) Yes.  Q6) Yes. |
| OPPO | Q1) Don’t support additional SSB positions for 120kHz  Q2) yes  Q3) 2 SSB per slot, but open to discuss  Q4) yes, e.g., depending on the value of QCL indication  Q5) Prefer to use same pattern  Q6) yes |

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| Futurewei | Q1) Do not add additional positions for 120kHz SCS.  Q2) Yes  Q3) 2 SSB per slot  Q4) The same number of candidates for licensed and unlicensed  Q5) Same pattern for licensed and unlicensed  Q6) Yes |
| Lenovo, Motorola Mobility | Q1) Fine with adding n = 4, 9, 14, 19 for the SSB candidate position for unlicensed operation  Q2) yes  Q3) 2 SSB per slot  Q4)  Q5) yes  Q6) yes |
| Interdigital | Q1) We support the further evaluation to add the additional candicate locations.  Q2) Yes.  Q3) We support at least 2 SSB per slot.  Q4) Yes, the number of candidate locations can be the same for both licensed and unlicensed.  Q5) Yes.  Q6) We support to include non-SSB slots to reduce the PRACH latency. |
| CATT | Q1) We support adding #4,#9,#14,#19 for 120kHz SCS.  Q2) Yes  Q3) 2 SSB per slot  Q4) The number for unlicensed can be different from licensed  Q5) Yes, candidate SSB locations for licensed band can be a subset of those for unlicensed band  Q6) Yes |
| Intel | Q1) Additional n = 4, 9, 14, 19 could be supported if DBTW is supported and DBTW enable/disable signalling is also supported.  Q2) Yes  Q3) 2 SSB per slot  Q4) The number of candidate SSBs could be different for LBT and no-LBT cases as long as DBTW enable/disable signalling is supported.  Q5) Yes  Q6) Yes. But this could not be always guaranteed. |
| NEC | Q1) If DBTW is supported, yes.  Q2)  Q3)  Q4) No, there should be more candidate SSB positions for unlicensed case than licensed case.  Q5)Yes, SSB resource pattern for licensed/no LBT case can be a complete subset of that for unlicensed case.  Q6) Yes. |
| vivo | Q1) Could be discussed further  Q2)  Q3) 2 SSB per slot  Q4) For unlicensed band, the number of candidates SSB locations can be larger.  Q5) Yes  Q6) Fine to discuss but better to be discussed until RAN4 LS back |
| Convida Wireless | Q1) There is no need to update NRB for 120 KHz. However, we are open for the other options.  Q2) Yes.  Q3) Yes  Q4) We are fine with SSB and COREST#0 are with same SCS, i.e., (SSB, Type0-PDCCH): = {480, 480}, {960, 960}. |
| Ericsson | Q1) We do not support additional value n = 4, 9, 14, 19. According to the WID, the maximum number of SS/PBCH block beams is 64. It is also the maximum number of candidate SSB positions that can be signalled in the SS/PBCH block using 3 bits from the DMRS sequence and 3 bits from the PBCH payload. Hence, if the motivation to support additional values of *n* is to somehow increase the number of candidate SSB positions (in case DBTW is supported), then adding other values of *n* would imply that some of the existing values would need to be removed. This would be in contradiction to the agreement that existing *n* values shall be supported. Furthermore, according to the WID, the overall objective is "supporting NR above 52.6GHz and leveraging FR2 design to the extent possible." As a final note, as commented by DOCOMO, this discussion seems to be related to DBTW, so it should be handled in that context.  Q2) As pointed out by LGE, for 480/960 kHz, we have NOTE (Strive to minimize specification impact due to the new SCS for SSB) in the previous agreement. In that sense, we suggest legacy pattern (e.g., Case D) as the starting point  Q3) Our preference is Case D as the starting point, so that implies up to 2 SSB/slot  Q4) Our strong preference is to have a common design for unlicensed / licensed, to avoid unnecessary implementation complexity, hence we support the same number of candidates (64) for both  Q5) N/A since we prefer same number of candidates for each mode (64)  Q6) Yes, we think those can be preserved assuming Case D pattern as starting point of design. |
| Sony | Q1) We support adding n =4, 9, 14, 19 if DBTW is supported.  Q2) Yes  Q3) 2 SSB per slot  Q4) No, the number of candidate SSB position for unlicensed would be larger than that for licensed if DBWT is supported.  Q5) Yes  Q6) Yes |
| WILUS | Q1) Yes, Additional n = 4, 9, 14, 19 could be supported if DBTW is supported for 120 kHz SSB.  Q2) Yes.  Q3) 2 SSB per slot  Q4) No, the number of candidates SSB locations for unlicensed band can be larger and also the number of candidate SSBs could be different for LBT and no-LBT cases even for unlicensed band.  Q5) Yes, the candidate SSB locations for licensed band can be a subset of the ones for unlicensed band.  Q6) Yes |
| Spreadtrum | Q1) prefer no additional n values for 120kHz. If low latency is addressed by 120kHz SCS data/control, the slots reserved for UL transmission is preferred. If not, there could be additional n values.  Q2) same pattern  Q3) two SSBs in a slot  Q4) No need to maintain the same number of candidates for licensed and unlicensed. Even if the number of candidates is the same and predefined with large number for unlicensed, DBTW can be used to reduce the number of candidates as well.  Q5) can be subset  Q6) Yes. The design principle can follow R15/16 FR2. |

#### **1st Round Discussion Summary:**

Summary of responses from companies are provided below.

* For 120kHz:
  + Q1) Whether or not to add n = 4, 9, 14, 19 for the SSB candidate position for unlicensed operation
    - Yes: Samsung, Sharp, ZTE, Sanechip, Nokia, NSB, Lenovo, Motorola Mobility, CATT, Intel, NEC
    - No: LGE, Qualcomm, Mediatek, Xioami, Huawei, HiSilicon, OPPO, Futurwei, Spreadtrum, Ericsson
    - FFS: Interdigital
* For 480 and 960 kHz:
  + Q2) same SSB resource pattern within pair of consecutive slots?
    - Yes: Samsung, Mediatek, ZTE, Sanechip, Nokia, NSB, Xioami, Huawei, HiSilicon, OPPO, Futurwei, Lenovo, Motorola Mobility, Interdigital, CATT, Intel, Spreadtrum
    - No / use legacy design (case D): Ericsson
  + Q3) 1 SSB per slot or 2 SSB per slot
    - 1 SSB per slot: Docomo
    - 2 SSB per slot: LGE(case D), Samsung, mediatek, ZTE, Sanechip, Nokia, NSB, Xioami, Huawei, HiSilicon, OPPO, Futurwei, Lenovo, Motorola Mobility, Interdigital, CATT, Intel, Spreadtrum, Ericsson
    - FFS: Qualcomm
  + Q4) same number of candidates depending on mode of operation (e.g. licensed and unlicensed or depending on LBT on or off)?
    - Same number: Docomo, Qualcomm, Mediatek, Xioami, Futurwei, Ericsson
    - larger number for unlicensed: Samsung, ZTE, Sanechip, Nokia, NSB, Huawei, HiSilicon, OPPO, CATT, Intel, NEC, Spreadtrum
  + Q5) if different number of SSB candidates depending on mode of operation, SSB resource pattern for licensed/no LBT case a complete subset of the other case (i.e. value of n for one mode all included in the other mode)?
    - Yes: Docomo, Samsung, Qualcomm, Mediatek, ZTE, Sanechip, Nokia, NSB, Xioami, Huawei, HiSilicon, OPPO, Futurwei, Lenovo, Motorola Mobility, Interdigital, CATT, Intel, NEC, Spreadtrum
  + Q6) should there be non-SSB slots every few SSB containing slots (i.e. non-consecutive values of n) to support intermittent UL or other transmissions than SSB?
    - Yes: Docomo, Samsung(for licensed), Qualcomm. Sharp, Mediatek, ZTE, Sanechip, Nokia, NSB, Xioami, Huawei, HiSilicon, OPPO, Futurwei, Lenovo, Motorola Mobility, Interdigital, CATT, Intel, NEC, Spreadtrum, Ericsson

#### **2nd Round Discussion:**

For 120kHz SSB, the inclusion of inclusion of n = 4, 8, 14, 19 for when DBTW is enabled seems to need further discussions.

For 480/960kHz SSB, companies seem to be generally aligned in the direction of the design. Moderator has formulated a proposal 1.4-1 based on inputs received so far. Please comment further on whether the following is ok. Moderator has also added Proposal 1.4-2 which might be the other alternative companies mentioned.

##### **Proposal 1.4-1)**

For 480kHz/960kHz SSB:

* first symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
  + value of X and Y are identical for 480kHz and 960kHz
    - FFS: exact value of X and Y
  + ~~FFS:~~ values of n for 480kHz and 960kHz
    - FFS: whether number of values for ‘n’ depend on licensed/unlicensed operation (or alternatively enablement/disablement of DBTW)
    - FFS: exact values of ‘n’ for each SCS
    - Values of ‘n’ for licensed (or disabled DBTW) cases shall be strictly a subset of values for unlicensed (or enabled DBTW) cases.
    - Values of ‘n’ shall not be all consecutive integer values (i.e. non-candidate SSB slots are positioned every few candidate SSB slots)
      * FFS: pattern for non-candidate SSB slots

##### **Proposal 1.4-2)**

For 480kHz/960kHz SSB:

* first symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
  + ~~FFS:~~ values of n for 480kHz and 960kHz
    - FFS: whether number of values for ‘n’ depend on licensed/unlicensed operation (or alternatively enablement/disablement of DBTW)
    - FFS: exact values of ‘n’ for each SCS
    - Values of ‘n’ for licensed (or disabled DBTW) cases shall be strictly a subset of values for unlicensed (or enabled DBTW) cases.
    - Values of ‘n’ shall not be all consecutive integer values (i.e. non-candidate SSB slots are positioned every few candidate SSB slots)
      * FFS: pattern for non-candidate SSB slots

If companies have further suggestion for consideration, please provide further comments.

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| **Company** | **Comment** |
| Samsung | We support the proposal (proposal 1.4-1).  Just comments on the FFS below FFS. Is there any intention that some bullets are FFS under the FFS, while others are not? |
| Qualcomm | We support the proposal (proposal 1.4-1). |
| LG Electronics | Still we believe legacy SSB pattern should be the baseline. {2,8}+14\*n or {4,8,16,20}+28\*n can be the candidates. We don’t prefer to give full flexibility on X, Y, and n values for 480/960 kHz SSB pattern. |
| Moderator | Made minor updates to avoid confusion on FFS aspects. |

#### **2nd Round Discussion Summary:**

TBD

### 2.1.5 CORESET#0 Configuration

* From [2] Huawei, HiSilicon:
  + Support only {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {120, 120} kHz in 52.6GHz to 71GHz spectrum.
  + CORESET#0 with 96 PRB can be configured to make full use of allowed transmit power at least for operation with shared spectrum.
  + Support the following CORESET#0 RB offsets values for {SSB, CORESET#0} SCS={120, 120} kHz:
    - 24 RB and 48 RB CORESET#0: the same as supported values in Table 13-8 of 38.213
    - 96 RB CORESET#0: 0, 38, 76 RBs for multiplexing pattern 1 and -20 (-21) RBs when for multiplexing pattern 3.
* From [3] vivo:
  + The following SSB-Coreset 0 multiplexing patterns are supported for each SCS pair:
    - (120K, 120K): Pattern 1, Pattern 3
    - (480K, 480K): Pattern 1, Pattern 3
    - (960K, 960K): Pattern 1, Pattern 3
    - (960K, 480K): Pattern 1, Pattern 2
  + To save more bits, the CORESET design of un-licensed band operation from 52.6GHz to 71GHz can re-use the design criterion in NR-U, which occupies as much bandwidth as possible in the frequency domain.
* From [5] Nokia, NSB:
  + Support providing CORESET#0/Type0-PDCCH configuration for 480kHz and 960kHz kHz SCS SSB transmission in NR bands ranging between 52.6 GHz to 71 GHz.
  + Consider supporting at least SSB and CORESET multiplexing pattern 1 for {480, 480} case. Pending on the UE minimum BW capability, consider also SSB and CORESET multiplexing pattern 2 or 3.
  + Consider supporting at least SSB and CORESET multiplexing pattern 1 for {960, 960} case.
  + Consider supporting pattern 1 and pattern 2 for {240,120} case.
  + For CORESET#0 with 120kHz sub-carrier spacing, consider supporting also N\_{RB}^{CORESET}={96}. In case SSB and Type0 CORESET multiplexing pattern 1 removing option of N\_{RB}^{CORESET}={24} could be considered.
  + For SSB and CORESET#0 with 480kHz sub-carrier spacing, support following options:
    - For multiplexing pattern1
    - For multiplexing pattern2 or 3 (if supported)
  + For CORESET#0 with 480kHz sub-carrier spacing, support
  + For SSB and CORESET#0 with 960kHz sub-carrier spacing, support for multiplexing pattern 1
  + For CORESET#0 with 960kHz sub-carrier spacing, support
  + For SSB with 240kHz sub-carrier spacing and CORESET#0 with 120kHz sub-carrier spacing, support following options:
* From [7] CATT:
  + Multiplexing pattern 2 or 3 can be used for further multiplexing SSB/CORSET#0 with periodic CSI-RS/paging PDCCH&PDSCH in frequency.
  + For SSB and CORESET#0/Type0-PDCCH with 120 KHz SCS, support the following combinations of SSB/CORESET multiplexing pattern, number of RB and symbols for CORESET.
    - {mux pattern 1, 48 PRB CORESET, 1 symbol CORESET}
    - {mux pattern 1, 48 PRB CORESET, 2 symbol CORESET}
    - {mux pattern 3, 48 PRB CORESET, 2 symbol CORESET}
* From [8] Qualcomm:
  + For non-initial access where SSB does configure Type-0 PDCCH and timing of the SSB is known to the UE (within limits defined in Table 7.6.4-2 of TS 38.133): support SCS = 480/960 kHz
  + consider the following SSB and CORESET0 SCS combinations:
    - SSB SCS = 120 kHz, CORESET0 SCS = 120, 480, 960 kHz
    - If SSB SCS = 240 kHz is supported, support CORESET0 SCS = 120, 480, 960 kHz
    - If SSB SCS = 480/960 kHz is supported for non-initial access where SSB does configure Type-0 PDCCH and timing of the SSB is known to the UE, support CORESET0 SCS = SSB SCS
  + consider ways to have 2 bits (1 extra bit compared to FR2) to indicate the common SCS in the SSB structure or contents in case more than 2 values for the common SCS are allowed
  + NR Rel-16 SSB/CORESET0 multiplexing pattern 1 design may be reused with possibly some changes to the table (e.g., the need for < 2.5 ms options for the start of the CORESET0 wrt frame boundary) which depends on the outcome of the SSB pattern design
  + SSB/CORESET0 multiplexing pattern 2:
    - For the 240 kHz + 120 kHz combination (if supported): reuse the same design as in NR Rel-16
    - For the 120 kHz + 480/960 kHz combination (if supported): the CORESET0 symbols may be placed in the gap symbols between the SSBs (similar to the existing NR Rel-16 design)
  + NR Rel-16 SSB/CORESET0 multiplexing pattern 3 design may be reused for the valid combinations of 120 + 120 kHz, 480 + 480 kHz, and 960 + 960 kHz
  + consider introducing an SSB/CORESET0 multiplexing pattern for higher SCS SSB (480 and 960 kHz), where a time domain fixed location for the CORESET0 and SIB1 is considered
  + consider introducing an SSB/CORESET0 multiplexing pattern for higher SCS SSB (480 and 960 kHz), where TDM grouping of the SSB and the corresponding CORESET0/SIB1 is considered
* From [10] ZTE, Sanechips:
  + The following multiplexing patterns for three approved SCS combinations of SSB and Type0-PDCCH can be considered for Rel-17 NR above 52.6 GHz. Other SCS combinations could be precluded.
    - (SSB, Type0-PDCCH): SCS (120 kHz, 120 kHz) Multiplexing patterns: 1, 3
    - (SSB, Type0-PDCCH): SCS (480 kHz, 480 kHz) Multiplexing patterns: 1, 3
    - (SSB, Type0-PDCCH): SCS (960 kHz, 960 kHz) Multiplexing patterns: 1, 3
  + For {SSB, CORESET#0 for Type0-PDCCH} SCS = {120, 120} kHz, even though RAN4 has agreed the minimum CBW is increased to 100 MHz, at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 should still be supported.
* From [11] Intel:
  + Support CORESET#0/Type0-PDCCH configuration indication in MIB of SSB for all supported SSB SCS.
  + Consider only same SCS for SSB and CORESET#0 (configured by MIB) for 480 and 960 kHz SCS.
* From [16] Samsung:
  + For CORESET#0
    - Support SSB with 240/480/960 kHz for initial and non-initial access with support of CORESET0/Type0-PDCCH configuration in the MIB.
      * SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical
      * only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS
    - It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries in the 57 – 71 GHz band no larger than [400] (Note: the total number of synchronization raster entries in FR2 for band n259 is 344). If the assumption cannot be satisfied, it’s up to RAN4 to decide which of 240/480/960 kHz SCS are supported for initial access of such band.
    - RAN1 prioritizes time-domain multiplex of SSB and CORESET0 to minimize the number of needed synchronization raster entries.
    - Supporting 480 kHz SCS and 960 kHz SCS for SSB are UE capabilities:
      * UE is not expected to support 480 kHz SCS for SSB if it doesn’t support 480 kHz SCS for data/control channels.
      * UE is not expected to support 960 kHz SCS for SSB if it doesn’t support 960 kHz SCS for data/control channels.
    - Send an LS to RAN2 and RAN4.
  + For SS/PBCH block with 120 kHz SCS,
    - only support CORESET#0 SCS as 120 kHz;
    - additional CORESET#0 RB offsets are needed;
    - support 96 RB as the number of RBs for CORESET#0.
  + For SS/PBCH block with 480 kHz SCS and 960 kHz,
    - only support CORESET#0 SCS same as SS/PBCH block SCS;
    - support at least the same SS/PBCH block and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, and number of symbols as in 120 kHz SCS;
    - support 96 RB as the number of RBs for CORESET#0;
    - Further study the RB offset based on RAN4 design of channel and synchronization rasters.
* From [17] MediaTek:
  + CORESET#0 should have the same SCS as SSB in initial access.
* From [21] Interdigital:
  + Consider other means to convey the CORESET#0 and Type0-PDCCH to UE to avoid BWP and SCS switching.
  + Consider introducing the parameters for the CORESET#0 and Type0-PDCCH, where the time and frequency allocations and the multiplexing patterns are (pre)configured in fixed settings
* From [23] Sharp:
  + Regarding {SSB, CORESET#0/Type0-PDCCH} SCS combination of {120, 120} kHz, in principle reuse the CORESET#0 configuration table of FR2. The motivations of removing/adding/modifying row(s) should be justified.
* From [25] NTT Docomo:
  + When new SCS(s) is supported for SSB and a single numerology is used for both SSB and CORESET#0/SIB1, at least TDM between SSB and CORESET#0/SIB1 can be supported.
  + In case of TDM between SSB and CORESET#0 PDCCH/SIB1 PDSCH, support different structure(s) of TDM than the ones supported in Rel-15/-16 NR.
    - E.g., a group of SSB/CORESET#0 PDCCH/SIB1 PDSCH, which are associated with the same QCL, is allocated within a slot
  + When the supported SCS for SSB in initial access case is limited compared to non-initial access cases, mixed numerology between SSB and CORESET#0/SIB1 should be supported.
  + When lower SCS is used for SSB compared with that used for CORESET#0/SIB1, FDM between SSB and SIB1 PDSCH such as in pattern 2 can be considered.
* From [26] Charter:
  + For the case where SSB location and SCS are explicitly provided to the UE (non-initial access) and SSB configures Type-0 PDCCH, support 480 kHz and 960 kHz numerologies for the SSB.
* From [27] WILUS:
  + Regarding the multiplexing between SSB and CORESET#0/RMSI-PDSCH, after agreeing new SCSs for SSB above all, it should be decided which combinations and multiplexing patterns are supported for NR operation from 52.6GHz to 71GHz.
  + We propose that SS/PBCH block and CORESET#0/RMSI can be multiplexed in TDM/FDM within a slot considering multi-beam operation and it can be closely located without the gap between SSB and CORESET#0/RMSI for not allowing any in-between channel access operation in the unlicensed band.

#### Summary of Discussions

* Only support same SCS between SSB and CORESET#0/Type-PDCCH
  + Huawei/Hilicon (for 120kHz SSB which is the only currently agreed SSB for initial access), Intel, ZTE, Sanechip, Samsung (for 480/960kHz), Mediatek, Docomo (for new SCS)
* Support only 1 SCS for CORESET#0/Type0-PDCCH for each SSB SCS
  + Samsung
* Support CORESET#0/Type0-PDCCH configuration for 480/960kHz SSB
  + vivo, Nokia, NSB, Intel, Qualcomm, Samsung, Charter
* Moderator suggest to discuss further on following issues:
  + Whether or not support CORESET#0/Type0-PDCCH configuration for 480/960kHz SSB
  + Any updates/changes to existing CORESET#0/Type0-PDCCH configuration for 120kHz SSB (if needed)
  + Supported multiplexing patterns and CORESET#0/Type-PDCCH parameters for 480/960kHz (if supported)

#### **1st Round Discussion:**

Moderator asks companies to provide input on the following:

* Q1) Any updates/changes to existing CORESET#0/Type0-PDCCH configuration for 120kHz SSB? If so what are some of the aspects that need consideration for the update/changes
* Q2) Whether Support CORESET#0/Type0-PDCCH configuration for 480/960kHz SSB
* Q3) if supported in Q1, supported multiplexing patterns and CORESET#0/Type-PDCCH parameters for 480/960kHz
* Q4) Support only 1 SCS for CORESET#0/Type0-PDCCH for each SSB SCS agreeable?

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| **Company** | **Comment** |
| DOCOMO | Q1) If 480/960 kHz SCS is not supported for SSB during initial access, we prefer to support 480 and/or 960 kHz CORESET#0/Type0-PDCCH configuration in addition to 120 kHz SCS for SSB with 120 kHz SCS.  Q2) We strongly support it as it achieves ANR/CGI reporting which is essential from operator’s perspective.  Q3) TDM should be baseline. FDM can be considered but it needs to be carefully considered in terms of coverage of CORESET#0/SIB1.  Q4) it highly depend on other aspects. |
| LG Electronics | * Q1) Any updates/changes to existing CORESET#0/Type0-PDCCH configuration for 120kHz SSB? If so what are some of the aspects that need consideration for the update/changes   + Existing configuration seems sufficient. However, if additional configuration is required, then that configuration can be just added with current configurations kept. * Q2 & Q3   + They depend on the decision in proposals from Sections 2.1.1 and 2.1.2. * Q4) Support only 1 SCS for CORESET#0/Type0-PDCCH for each SSB SCS agreeable?   + We agree to support only 120 kHz CORESET#0/Type0-PDCCH for 120 kHz SSB SCS. |
| Samsung | 1) Yes.   * The number of RBs for CORESET#0 can consider 96 RBs, since the carrier bandwidth is much larger than FR2. * The RB offset for CORESET#0 needs to be reconsidered (after RAN4 finalizes the channel and sync raster design), since the minimum channel bandwidth is increased from FR2.   2) Yes.  3)   * Other than the RB offsets, the other parameters for CORESET#0 configuration for 480 and 960 kHz can reuse 120 kHz SSB. * Other than the offset O, the other parameters for Type0-PDCCH configuration for 480 and 960 kHz can reuse 120 kHz SSB.   4) Yes. |
| Qualcomm | Q1)   * For SSB + CORESET0 = 120 kHz + 120 kHz, no change is needed * Support SSB + CORESET0 = 120 kHz + 480/960 kHz (to support a single numerology deployment using 120 kHz SCS SSB (and 240 kHz SCS SSB if supported) and 480/960 kHz SCS data/control)   Q2) Depends on outcome for 2.1.1 and 2.1.2  Q3) Depending on SSB SCS. Recommend that we first agree on the SSB + CORESET0 combinations, then return to this  Q4) No. We would like to consider SSB + CORESET0 = { 120 + 480/960 and 120 + 120 } |
| Mediatek | Q1) We support only (SSB SCS, CORESET #0 SCS)=(120, 120)  Q2) No  Q3) We are not sure whether 480/960 kHz means CORESET SCS or SSB with 480/960 kHz SCS?  Q4) At least for SSB SCS=120 kHz, we don’t see strong need or obvious benefit to support CORESET SCS other than 120 kHz |
| ZTE, Sanechips | For Q1), for {SSB, CORESET#0 for Type0-PDCCH} SCS = {120, 120} kHz, at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 should still be supported. If additional configuration (e.g. introducing 96 PRBs) is proved to be feasible, the reserved bits can be used for it.  For Q2), we think "yes" but depending on the decision in section 2.1.1 and 2.1.2.  For Q3), depends on the decision in section 2.1.1 and 2.1.2.  For Q4), yes. We support CORESET#0/Type0-PDCCH is applied with a same SCS as the associated SSB SCS, e.g.   * (SSB, Type0-PDCCH): SCS (120 kHz, 120 kHz) * (SSB, Type0-PDCCH): SCS (480 kHz, 480 kHz) * (SSB, Type0-PDCCH): SCS (960 kHz, 960 kHz) |
| Nokia | Q1) For 120kHz CORESET#0 we could consider supporting also ={96}. Need of additional/different offsets are also pending on the RAN4 agreements.  Q2) Yes, we see this important to enable ANR/PCI confusion resolution.  Q3) Consider supporting at least SSB and CORESET multiplexing pattern 1. Support for multiplexing pattern 2 or 3 (assuming still single scs for CORESET#0/Type0-PDCCH and SSB) could be further considered.  Q4) While this depends on the other agreements, we think that if CORESET#0/Type0-PDCCH for 480/960kHz SSB is supported, we could assume single scs. |

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| Huawei, HiSilicon | Q1) In addition to the existing {SS/PBCH Block, CORESET#0 for Type0-PDCCH} for {120, 120} kHz SCS, support CORESET#0 with 96 PRB for {SS/PBCH Block, CORESET#0 for Type0-PDCCH} for {120, 120} kHz SCS.  Q2) No.  Based on the current agreements, 480/960kHz SSBs do not configure Type-0 PDCCH. There is no need to configure CORESET#0 for Type0-PDCCH for CGI-report. If CGI report for 480/960 kHz is necessary, it can be supported using dedicated signaling.  Q3) For the additional CORESET#0 with 96 PRB for {SS/PBCH Block, CORESET#0 for Type0-PDCCH} for {120, 120} kHz SCS, support CORESET0 RB offset with 0, 38, 76 RBs for multiplexing pattern 1 and -20 (-21) RBs when for multiplexing pattern 3.  Q4) For 120 kHz SSB, support only one 1 SCS for CORESET#0/Type0-PDCCH equal to 120 kHz.  For 480/960 kHz SSB, do not support any CORESET#0/Type0-PDCCH. |
| OPPO | Q1) No. For 120kHz SSB, we prefer to only support (SSB 120kHz, CORESET#0/Type0-PDCCH 120kHz).  Q2) Depends on the outcome of section 2.1.1 and 2.1.2.  Q3)  Q4) Yes. |

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| Futurewei | Q1) for {SSB, CORESET#0 for Type0-PDCCH} SCS = {120, 120} kHz, no changes are necessary  Q2) depends on the outcome of the decision in section 2.1.1 and 2.1.2  Q3) depends on the outcome of the decision in section 2.1.1 and 2.1.2  Q4) |
| Lenovo, Motorola Mobility | Q1) No changes needed for 120/120kHz SSB / CORESET0 multiplexing  Q2) yes  Q3) Agreements on the different mux patterns of SSB + CORESET0 should be met first  Q4) We prefer single SCS for both SSB and CORESET#0 |
| Interdigital | Q1) We support keeping the existing configurations for the 120kHz SCS.  Q2) Yes. |
| CATT | Q1) If 480/960 kHZ is not supported for initial access, then we need to further discuss if 480/960kHz CORESET#0  Q2) Depends on the outcome of the decision previously, for example this may be very important to support ANR  Q3) Depends on the outcome of the decision previously  Q4) Depends on the outcome of the decision previously, but if only 120kHz is supported for initial access there may be a need to consider {120,480/960}. |
| Intel | Q1) Reuse existing configurations for {SCS SSB, SCS CORESET#0/Type0-PDCCH} = 120kHz. Additional configurations could be further discussed.  Q2) Support  Q3) Pattern 1 is prioritized first. Pattern 3 could be also considered then.  Q4) Yes. The same SCS for SSB and CORESET#0/Type0-PDCCH |
| vivo | Q1)   * For SSB + CORESET0 = 120 kHz + 120 kHz un licensed band, the CORESET0 RB number can be increased. * Whether support SSB + CORESET0 = 120 kHz + 480/960 kHz can FFS.   Q2) Yes, CORESET#0/Type0-PDCCH configuration for 480/960kHz SSB is needed to support ANR.  Q3) It depends on the results from Sections 2.1.1 and 2.1.2. The design of multiplexing pattern can reuse the design in FR2.  Q4) It depends on whether 480/960K SSB could be used for initial access or not. If only 960K SSB is supported for initial access, it is still beneficial to consider SSB + CORESET0 = 960 kHz + 480 kHz. |
| Ericsson | Q1) We support reuse of the existing (120,120) tables in 38.213 Section 13   * Whether or not new SSB-CORESET0 offsets are needed (still an FFS item) depends on the RAN4 sync raster design. If the existing FR2 sync raster granularity (17.28 MHz) is maintained, now new offsets are needed to support 100 MHz minimum bandwidth. However, if the sync raster granularity is modified (e.g., every 2nd sync raster point = 34.56 MHz granularity), then an additional offset is needed for SSB-CORESET0 multiplexing pattern 1. The needed additional offset is 2 RBs for the case of 48 RB CORESET0 (Rel-15/16 supports only the value 14 RBs). * Some companies have suggested support for 96 RB CORESET; however, after investigation of link budgets between various signals/channels, we found that RMSI PDSCH is the limiting channel amongst SSB, Type0-PDCCH, RMSI PDSCH. Hence, increasing the number of RBs for Type0-PDCCH is not helpful in terms of coverage, so we don't see the motivation.   Q2) This topic is already treated in Section 2.1.1 and 2.1.2  Q3) Recommended we return to this once there is more clarity. In principle, however, we should strive to reuse as much as possible from the (120,120) design  Q4) Yes |
| Sony | Q1) If 480/960 kHz SCS SSB is not supported for initial access, 480/960 kHz CORESET#0 may need to be considered. If 480/960 kHz SCS SSB is supported for initial access, no need to change for CORESET#0/Type0-PDCCH configuration for 120kHz SSB.  Q2) Our preference is yes, but it depends on outcome in section 2.1.1 and 2.1.2  Q3) Depends on outcome in section 2.1.1 and 2.1.2  Q4) Yes, we prefer single numerology operation, but it depends on outcome in section 2.1.1 |
| WILUS | Q1) Reuse existing configurations for {SCS SSB, SCS CORESET#0/Type0-PDCCH} = 120kHz. Additional configurations could be further discussed.  Q2) Support but it depends on outcome of the decision in section 2.1.1 and 2.1.2.  Q3) Depends on the outcome of the decision in section 2.1.1 and 2.1.2.  Q4) Yes. |
| Spreadtrum | Q1) Open to discussion  Q2) Yes  Q3) multiplexing pattern 1 and 3 are prioritized  Q4) Yes |

#### **1st Round Discussion Summary:**

* Q1) Any updates/changes to existing CORESET#0/Type0-PDCCH configuration for 120kHz SSB? If so what are some of the aspects that need consideration for the update/changes
  + Support 96 PRB: Samsung, ZTE, Sanechips, Nokia, Huawei, HiSilicon
    - Do not see a need: Ericsson
  + RB offset for CORESET#0: Samsung
  + Support {120, 480} and {120, 960} SCS pair for SSB and CORESET#0/Type0-PDCCH: Qualcomm
  + Only support {120, 120} SCS pair for SSB and CORESET#0/Type0-PDCCH: Mediatek
* Q2) Whether Support CORESET#0/Type0-PDCCH configuration for 480/960kHz SSB
  + Yes: Docomo, Samsung, ZTE, Sanechips, Nokia, Lenovo, Motorola Mobility, Interdigital, Intel, Spreadtrum
  + No: Mediatek, Huawei, HiSilicon
* Q3) if supported in Q1, supported multiplexing patterns and CORESET#0/Type-PDCCH parameters for 480/960kHz
  + TDM (mux pattern 1): Docomo, Nokia, Intel, Spreadtrum
  + FDM (mux pattern 3): Spreadtrum
  + Reuse configuration (other than RB offset) from 120kHz Case: Samsung
  + FFS: Ericsson
* Q4) Support only 1 SCS for CORESET#0/Type0-PDCCH for each SSB SCS agreeable?
  + FFS: Docomo
  + Yes: LGE (for 120kHz), Samsung, Mediatek(for 120kHz), ZTE, Sanechips, Nokia, Huawei, HiSilicon (for 120kHz), OPPO, Motorola Mobility, Intel, Spreadtrum, Ericsson
  + No: Qualcomm, CATT(if only 120kHz is supported for initial access)

#### **2nd Round Discussion:**

Discussion on support of CORESET#0\Type0-PDCCH for 480/960kHz will be needed before further discussion.

For 120kHz, among the issues additional support for 96 PRB CORESET seems to be popular suggestion. However, there was at least 1 company who did not think such configuration was needed. Also supporting only 1 SCS for CORESET#0/Type0-PDCCH for a given SSB SCS seems to be something that has large support. Moderator has formulated two proposals based on inputs received.

##### **Proposal 1.5-1)**

* For 120kHz SSB, additionally support 96 PRB CORESET#0 configuration(s).
  + FFS which multiplexing pattern (i.e. 1, 2, and/or 3) and number of symbols (i.e. 1, 2, and/or 3) for 96 PRB CORESET#0 will be used with.

##### **Proposal 1.5-2)**

* RAN1 to support only 1 SCS for CORESET#0/Type0-PDCCH for a given SSB SCS

Please provide further comments on proposal 1.5-1 and 1.5-2.

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| **Company** | **Comment** |
| Samsung | We support Proposal 1.5-1. One comment on the FFS, the RB offset should also be added as part of the FFS to make the design complete.  We support Proposal 1.5-2. |
| Qualcomm | We support Proposal 1.5-1  We do not support Proposal 1.5-2 (we propose to consider SSB + CORESET0 = 120 kHz + 480/960 kHz (to support a single numerology deployment using 120 kHz SCS SSB (and 240 kHz SCS SSB if supported) and 480/960 kHz SCS data/control)) |
| LG Electronics | For Proposal 1.5-1, even though we are open to discuss the possibility of adding 96 PRBs for CORESET#0 configuration, we don’t think adding 96 PRBs is sufficiently justified. Minimum and maximum channel bandwidth for 120 kHz is the same as in Rel-15. In that case, what is the main motivation to add 96 PRBs for CORESET#0 configuration?  We support Proposal 1.5-2. |

#### **2nd Round Discussion Summary:**

TBD

### 2.1.5 Various other aspects on SSB Design

* From [2] Huawei, HiSilicon:
  + For operation with shared spectrum and for 480 kHz and 960 kHz SSBs, indicate the 7th bit of the candidate SSB index by borrowing the 4th LSB of SFN in the PBCH payload. Indicate the 4th LSB of SFB in MIB payload.
* From [3] vivo:
  + For initial cell search in 52.6-71GHz, a UE may assume that half frames with SSB occur with smaller period than FR2 (e.g. 5ms), or lower RAN4 requirement for the cell search time.
* From [4] Spreadtrum:
  + The SSB-based TRS/CSI-RS validation can be supported.
* From [8] Qualcomm:
  + For initial access, in cases where the SSB SCS is smaller than other channels’ SCS (e.g., PDCCH/PDSCH), consider WB DMRS or cell-specific TRS for further timing error corrections
    - For cell-specific TRS, consider studying the FD density needed
* From [21] Interdigital:
  + Consider the enhancements to indicate the license regime in initial access operations for licensed/unlicensed overlapping spectrum in beyond 52.6GHz.
* From [22] Convida:
  + SSB coverage enhancement should be studied for higher SCS.

#### Summary of Discussions

* Companies have provided discussion on considerations for SSB design.
  + For operation with shared spectrum and for 480 kHz and 960 kHz SSBs, indicate the 7th bit of the candidate SSB index by borrowing the 4th LSB of SFN in the PBCH payload. Indicate the 4th LSB of SFB in MIB payload.
  + For initial cell search in 52.6-71GHz, a UE may assume that half frames with SSB occur with smaller period than FR2 (e.g. 5ms), or lower RAN4 requirement for the cell search time.
  + The SSB-based TRS/CSI-RS validation can be supported.
  + For initial access, in cases where the SSB SCS is smaller than other channels’ SCS (e.g., PDCCH/PDSCH), consider WB DMRS or cell-specific TRS for further timing error corrections
    - For cell-specific TRS, consider studying the FD density needed
  + Consider the enhancements to indicate the license regime in initial access operations for licensed/unlicensed overlapping spectrum in beyond 52.6GHz.
  + SSB coverage enhancement should be studied for higher SCS.
* Moderator suggests discussing above listed issues further.

#### **1st Round Discussion:**

Moderator asks companies to provide input on the following issues:

* Support wideband DMRS or cell-specific TRS to aide timing error correction (for 120kHz SSB with 480 or 960kHz control/data transmission)
* Any changes to the default SSB periodicity to be assumed by the UE
* Methods to indicated licensed or unlicensed operation
  + This may need to be discussed under channel access agenda

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| **Company** | **Comment** |
| Samsung | * Is it for IDLE mode only? Seems more discussion is needed for this topic. * If DBTW is supported, the initial access performance may not be an issue. More discussion towards this seems needed. * Different sync raster can be assigned for licensed and unlicensed band for initial access purpose, and network can explicit configure this information after initial access. |
| Qualcomm | * For initial access, in cases where the SSB SCS is smaller than other channels’ SCS (e.g., PDCCH/PDSCH), consider WB DMRS or cell-specific TRS for further timing error corrections (for cell-specific TRS, consider studying the FD density needed). * No change to default SSB periodicity * Distinction of licensed, unlicensed, or unlicensed but no LBT can be in SIB1 or later |

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| Futurewei | * We support wideband DMRS or cell-specific TRS to aide timing error correction * No change to the default SSB periodicity |
| Lenovo, Motorola Mobility | * For initial access, we prefer a single numerology for SSB and data/control, hence no need for wideband DMRS |
| Interdigital | * We prefer a single numerology operation, so we don’t support wideband DMRS and TRS. * We don’t see the need to introduce any changes * Supporting different sync raster offsets would be a good option as for the indication of the license regime. If the different sync raster offsets are not available (e.g., to enable/disable DBTW), we can consider other options such as MIB. |
| vivo | * It depends on the discussion outcome on SSB SCS and initial DL BWP SCS * We think the cell search complexity even for 120KHz SSB should be studied, e.g. frequency domain synchronization complexity. If 480K/960K SSB is agreed for initial access purpose, the buffering complexity should also be studied. Based on the outcome on the study, we may decide whether the change of default initial access is needed or not. * Indication of licensed or unlicensed operation is needed and sync raster differentiation is a good way to achieve this. |
| Convida Wireless | * If SCS 480/960 KHz for SSB are supported, then coverage enhancement can be studied. |
| Ericsson | * Wideband DMRS/Cell Specific TRS   + We don't see a strong motivation for this, as during initial access performance should not require fine time/frequency tracking   + Furthermore, this seems like quite a large change * Default SSB Periodicity   + No change to Rel-15/16 (i.e., 20 ms default periodicity is assumed) * Methods to indicate licensed/unlicensed operation   + As we highlighted in Section 2.1.3, for initial access, it needs to be decided how to indicate LBT on/off. In the GTW it was agreed to discuss this in the channel access AI. The reason for the dependency on initial access is that the size of DCI 1\_0 with CRC scrambled by SI-RNTI (i.e., the Type0-PDCCH used to schedule PDSCH carrying SIB1) has a different size depending on shared/non-shared spectrum (see highlighted sentence in below extract from 38.212 Section 7.3.1.2.1. Hence two alternatives for handling this are:  1. the UE does 2 blind decodes assuming the 2 different sizes 2. LBT on/off is indicated in MIB so that the UE can avoid 2 blind decodes   Clearly, if solution (2) is adopted, one bit needs to be found in MIB for indicating LBT on/off in addition to bits for Q.  Some companies have also suggested using a different set of sync raster points (SetA vs. SetB) for indicating LBT on/off. However, we point out that this can double the UE SSB search complexity, which is most likely not desirable from a UE implementation standpoint. Furthermore, this has a strong RAN4 dependence.  --- Extract from 38.212 Section 7.3.1.2.1 ---  The following information is transmitted by means of the DCI format 1\_0 with CRC scrambled by SI-RNTI:  - Frequency domain resource assignment – bits  -  is the size of CORESET 0  - Time domain resource assignment – 4 bits as defined in Clause 5.1.2.1 of [6, TS38.214]  - VRB-to-PRB mapping – 1 bit according to Table 7.3.1.2.2-5  - Modulation and coding scheme – 5 bits as defined in Clause 5.1.3 of [6, TS38.214], using Table 5.1.3.1-1  - Redundancy version – 2 bits as defined in Table 7.3.1.1.1-2  - System information indicator – 1 bit as defined in Table 7.3.1.2.1-2  - Reserved bits – 17 bits for operation in a cell with shared spectrum channel access; otherwise 15 bits  --- End extract --- |

#### **1st Round Discussion Summary:**

Companies are not in agreement on the open issues that were brought up and likely require further discussions.

#### **2nd Round Discussion:**

Looks like companies need to further discussion some of the other open issues that were brought up. Please continues to comment further on issues outlined in 1st round discussion.

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| **Company** | **Comment** |
| Qualcomm | Re-iterating the same comments for 1st round:  For initial access, in cases where the SSB SCS is smaller than other channels’ SCS (e.g., PDCCH/PDSCH), consider WB DMRS or cell-specific TRS for further timing error corrections (for cell-specific TRS, consider studying the FD density needed). |
| LG Electronics | To Qualcomm,  The motivation to change FD density of TRS seems to be valid only when SSB SCS is 120 kHz but SCS of initial BWP is 960 (or 480) kHz. If this is the case, it can be further discussed after we agree such kind of SCS combination.  To Ericsson,  We understand the concern due to DCI size misalignment, if LBT on or off is not indicated before a UE receives SIB1. So, Ericsson’s proposal is to indicate LBT on or off in MIB or prior to MIB. Is that correct understanding? We agree that LBT on or off needs to be signaled in MIB or prior to MIB. However, even though LBT on or off is signaled in SIB1, we think the problem can be figured out by UE assuming 17 bits for all cases in 60 GHz. |

#### **2nd Round Discussion Summary:**

TBD

## 2.2 PRACH Aspects

### 2.2.1 Supported PRACH Numerology

* From [1] Futurwei:
  + For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2.
    - For non-initial access use cases, support 480 and 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.
* From [2] Huawei, HiSilicon:
  + When UE is in RRC\_IDLE or RRC\_INACTIVE state, support only 120 kHz SCS for PRACH preamble and Msg.3 transmission in 52.6GHz to 71GHz spectrum. This includes all following cases:
    - Initial access from RRC\_IDLE,
    - Transition from RRC\_INACTIVE to RRC\_CONNECTED,
    - Request for OSI in RRC\_IDLE or RRC\_INACTIVE state.
    - Note: When UE is in RRC\_IDLE or RRC\_INACTIVE state, RACH configuration is provided in the configuration of initial UL BWP for PCell in SIB1.
  + When UE is in RRC\_CONNECTED state, in addition to 120 kHz SCS, support 480 kHz and 960 kHz SCS for PRACH preamble and Msg.3 transmission in 52.6GHz to 71GHz spectrum.
* From [3] vivo:
  + Support 120KHz, 480KHz and 960KHz as candidate SCS of initial UL BWP.
  + Support 960KHz SCS in addition to 120KHz SCS for PRACH format (A, B, C).
* From [5] Nokia, NSB:
  + Support 480kHz and/or 960 kHz SCS for PRACH in non-initial access use cases.
  + Support 480kHz and/or 960 kHz SCS for PRACH in initial access use case when UE’s SSB search complexity can be mitigated
* From [10] ZTE, Sanechips:
  + Support additional SCSs (480kHz and/or 960kHz) for PRACH and SSB if single subcarrier spacing is supported.
* From [11] Intel:
  + Support 480 kHz and 960 kHz SCS for PRACH in NR extension up to 71 GHz.
    - Note: no need to distinguish whether the PRACH is for initial access or non-initial access, as such distinction does not exist for RAN1 specification.
* From [12] Fujitsu:
  + In addition to 120kHz, support 480kHz and 960kHz for PRACH SCS for all cases.
* From [13] Apple:
  + If 480kHz and 960kHz SCS are used for PRACH transmission, support L=139 only.
* From [18] LGE:
  + If 480 and/or 960 kHz SCS SSB is not supported for the initial access use case, support only the 480 and/or 960 kHz SCS PRACH with the sequence length L=139 for the cases other than initial access (e.g., for SCell).
* From [19] Lenovo, Motorola Mobility:
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, support both the numerologies of 480kHz and 960kHz for PRACH transmission
* From [21] Interdigital:
  + Further study necessity of PRACH for additional SCSs in Rel-17.
* From [25] NTT Docomo:
  + For PRACH SCS, as well as SSB, 480 and 960 kHz SCS should be supported at least for non-initial access cases.

#### Summary of Discussions

* Support 120kHz PRACH in all cases, support 480/960kHz RACH for connected mode
  + Huawei, HiSilicon
* Support 120kHz PRACH in all cases, support 480/960kHz RACH for (at least) non-initial access cases
  + Futurewei, Docomo
* Support 480 and 960kHz PRACH (in addition to 120kHz PRACH)
  + vivo, ZTE, Sanechips, Intel, Fujitsu, Apple (only L=139), LGE (only L=139), Lenovo, Motorola Mobility,
* Moderator understands that most (if not all) companies have similar proposal to support 480/960kHz in RAN1 specification. There are some discussion around limiting use of specific PRACH SCS in different use cases, but from moderator’s understanding such distinction will not be present in RAN1 specification. Moderator suggest further discussion as companies seems to be close to alignment.

#### **1st Round Discussion:**

From modertor’s understanding the physical layer does not distinguish initial access and non-initial access for PRACH as all the random access behaviors is described in RAN2. In order to make further discussion and progress on RACH, moderator suggest to first see we can agree to support which SCS for PRACH, and further discuss how and whether to limit the SCS usage for specific scenarios. This way some further discussion on RO and PRACH sequence and format could be made.

Please comment further on the following proposal.

##### **Proposal 2.1-1)**

* Support 480kHz and 960kHz PRACH in physical layer specifications
  + RAN1 to send LS to RAN2 to inform any specific PRACH SCS are to be excluded from certain modes of operation from RAN1 perspective (if any)
* RAN1 to discuss further on restriction of specific PRACH SCS for specific scenarios

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| **Company** | **Comment** |
| DOCOMO | Support the Proposal 2.1-1. Since 480/960 kHz SCS for SSB are supported at least for non-initial access, 480/960 kHz PRACH should be supported in PHY specifications. Ok with sending LS to RAN2 on use case restrictions and discussing about it further in RAN1. |
| Samsung | We support the proposal.  We have a clarification question regarding the comment in the GTW. In our understanding, initial BWP configured in SIB1 can take a SCS of 480 kHz and 960 kHz, for both downlink and uplink cases, since the agreement of supporting 480 kHz and 960 kHz for data/control/RS didn’t specify its use cases. Then it would be straightforward to allow PRACH to use the same SCS as well. |
| LG | Support the Proposal 2.1-1. Since 480/960 kHz SCS for SSB are supported at least for non-initial access, it is better to send LS to RAN2 in order to make further discussion and progress on RACH. |
| Qualcomm | Fine with proposal |
| Sharp | We support the proposal. |
| ZTE, Sanechips | We are fine with the proposal. |
| Fujitsu | We support the proposal. |
| Nokia | We are OK with the proposal. |
| Xiaomi | Fine with the proposal |

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| Huawei, HiSilicon | We do not see the need for Proposal 2.1-1 and we can’t support it. Please note that we already have the following agreement from **RAN1 104-e**:  Agreement:   * For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2. * For non-initial access use cases,   + if 480kHz and/or 960 kHz SSB SCS is agreed to be supported, support 480 and/or 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.   So, we already have agreement in place that 480 and/or 960 kHz PRACH SCS are supported **for non-initial access use cases.**  We agree with the moderator to “make further discussion and progress on RACH” (let’s call this discussion as *Discussion 1*), but the basis for *Discussion 1* is already provided and we can use the above agreement as a baseline to further enhance the PRACH configuration design of 480/960 kHz PRACH SCS for non-initial access. This is similar to the discussions that we have regarding the possible enhancements in PRACH configuration for 120 kHz SCS.  In parallel to above *Discussion 1*, we can have *Discussion 2*: “Whether or not the application of 480/960 kHz PRACH SCS should be extended to initial access case”. However, the outcome of *Discussion 2* would not affect the possible progress in *Discussion 1* as the enhancements in *Discussion 1* will be applicable for all supported cases (only non-initial access case or both non-initial access case and initial access case if the support for 480/960 kHz PRACH SCS is agreed to be extended to the initial access case in *Discussion 2*). After *Discussion 2* is concluded, we can send an LS to RAN2 and inform them about RAN1 decision. *But, in any case, the decision of whether 480/960 kHz PRACH SCS is only supported for non-initial access case or for both initial access and non-initial access cases must be made in RAN1. RAN2 has no means to make such a decision.*  Finally, in our view, above agreement in RAN1 104-e means that “UE is not expected to be configured with 480/960 kHz SCS PRACH in initial UL BWP of a PCell provided in Type0-PDSCH”. This is clearly a RAN1 specification impact.  As a summary of our views, we suggest the following proposal that is built on the Agreement in RAN1 104-e:  **Proposal:**   * **The agreement in RAN1 104-e on the support for 480 and 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2 for non-initial access use case means that UE is not expected to be configured with 480/960 kHz SCS PRACH in initial UL BWP of a PCell provided in Type0-PDSCH.** * **FFS: Enhancements on PRACH configuration design for 480 and 960 kHz PRACH SCS.** |
| OPPO | Fine with the proposal. |
| Futurewei | We are OK in principle with the proposal i.e. to send an LS to RAN 2. The actual LS needs further discussions. Therefore, we suggest adding “LS to RAN4 text is FFS” |
| Lenovo, Motorola Mobility | Fine with the proposal 2.1-1 |
| Interdigital | We support the proposal. |
| CATT | We support 480kHz and 960kHz PRACH in physical layer specifications. The LS to ran2 can be discussed if there is really a exclusion issue. |
| Intel | Support the proposal |
| vivo | We are fine with the Proposal 2.1-1. |
| Ericsson | Huawei has a point – we have already agreed to support 480/960 kHz PRACH for non-initial access use cases, and clearly this would be specified in RAN1.  We are okay to provide an LS to RAN2 (doesn't need to be this meeting) informing them of potential restrictions on the use cases of 480/960 kHz PRACH once decisions on SSB are stable. |
| Sony | We support the proposal |

#### **1st Round Discussion Summary:**

Huawei has pointed out our previous agreement. Based on the previous agreement, moderator assumes that 480kHz and 960kHz PRACH will be supported in the physical layer specification, and the only issue left is whether or not 480kHz and 960kHz can be applicable for initial access. However, this seems quite dependent on 480/960kHz SSB support for initial access. Therefore moderator assumes discussion on supported PRACH numerology can be skipped for this meeting.

#### **2nd Round Discussion:**

Moderator assumes previous RAN1 agreement means 480/960kHz PRACH will be specified in RAN1 specification, and RAN1 could go ahead with further development of RAN1 specification for 480/960kHz PRACH.

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| Agreement:   * For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2. * For non-initial access use cases,   + if 480kHz and/or 960 kHz SSB SCS is agreed to be supported, support 480 and/or 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively. |

If there are any different understanding, please comment further.

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| **Company** | **Comment** |
| Samsung | We are ok with FL’s assessment.  We would also to note that actually we didn’t have a clear definition of “initial access” and “non-initial access” for PRACH (not as a clear statement as SSB), so even with the agreement, it’s still confusing which exact cases are applicable. |
| Qualcomm | We have the same understanding as FL |
| Ericsson | We are also OK with the FL's assessment.  Regarding clarification of "non-initial" access, we can revisit that later if needed. It shouldn't stop the work on physical layer specification. |

#### **2nd Round Discussion Summary:**

TBD

### 2.2.2 PRACH Sequence and Format

* From [5] Nokia, NSB:
  + Support L=139 for PRACH with 480kHz and 960kHz at above 52.6 GHz.
* From [6] Ericsson:
  + Conclude that for PRACH with 480/960 kHz SCS, only L = 139 is supported, i.e., L = 571 and 1151 are not supported.
* From [7] CATT:
  + Consider supporting increasing symbols in time domain to enhance PRACH coverage.
  + Consider repeating and concatenating the PRACH preamble sequence to enhance PRACH coverage for unlicensed spectrum operation
* From [8] Qualcomm:
  + consider only using PRACH sequence length = 139 for SCS = 480 kHz and 960 kHz
* From [9] OPPO:
  + Sequence length L=571 and 1151 for PRACH when the SCS is 480kHz/960kHz are not needed.
* From [11] Intel:
  + Optional support of PRACH formats A1~A3, B1~B4, C0, C2 for and with SCS 480 kHz and 960 kHz, i.e., .
* From [16] Samsung:
  + Support short PRACH format for all PRACH sequence lengths and all SCSs , and don’t support long PRACH format.
* From [18] LGE:
  + The 120 kHz PRACH SCS with sequence lengths L=571 and L=1151 are not required for the licensed spectrum where the regulatory requirements are not defined on PSD limit.
* From [21] Interdigital:
  + For 52.6 – 71 GHz, the existing PRACH sequences with the existing PRACH sequence lengths 571 and 1151 should be reused.
* From [23] Sharp:
  + Only support L = 139 for PRACH with 480kHz and 960 kHz SSB SCS.
* From [25] NTT Docomo:
  + For PRACH sequence with 480/960 kHz SCS, at least L=139 should be supported.
    - Whether to support additional length (e.g., L=571 and/or 1151) should be discussed after receiving an LS reply from RAN4 on UE EIRP and conducted power in 52.6 – 71 GHz

#### Summary of Discussions

* Supported sequence lengths
  + For 480/960kHz SCS PRACH (if agreed):
    - L=139: Ericsson, LGE, Nokia, NSB, OPPO, Qualcomm, Docomo (other lengths FFS)
    - L=139, 571, 1151: Intel, Samsung, Interdigital
* Supported PRACH formats:
  + For 480/960kHz SCS PRACH (if agreed) support all existing formats, A1~A3, B1 ~B4, C0, C2:
    - Intel
* One company commented that PRACH length decision may need to wait for RAN4 reply LS on EIRP and max conducted power.
* Moderator suggest discussing further based on following proposal (as starting point):
  + For 480/960kHz SCS PRACH (if agreed), only support L=139

#### **1st Round Discussion:**

Moderator suggest discussing on the following:

##### **Proposal 2.2-1)**

* For 480/960kHz SCS PRACH (if agreed), support all existing PRACH formats (A1~A3, B1 ~B4, C0, C2) with sequence length L = 139
  + FFS: support for sequence length L = 571, and 1151

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| **Company** | **Comment** |
| DOCOMO | We support the Proposal 2.2-1. |
| Samsung | We are ok with the proposal. |
| LG | We support the Proposal 2.2-1. |
| Qualcomm | SCS = 480/960 kHz with sequence length = 139 is enough to achieve the desired BW requirement for the maximum EIRP allowed.  We are fine with main bullet and prefer to remove the FFS part |
| Sharp | We are fine with the proposal. |
| Mediatek | We are ok with the proposal |
| ZTE, Sanechips | We are fine with the proposal. |
| Fujitsu | We support the proposal. |
| Nokia | We are OK with the proposal. |
| Xiaomi | Fine with the proposal |

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| Huawei, HiSilicon | We do not support Proposal 2.2-1. As discussed in our views for Proposal 2.1-1), we already have an agreement in RAN1 104-e regarding the support of 480/960kHz PRACH for non-initial access case as follows:  Agreement **(RAN1 104-e):**   * For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2. * For non-initial access use cases,   + if 480kHz and/or 960 kHz SSB SCS is agreed to be supported, support 480 and/or 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.   In our view, proposal 2.2-1) potentially expands the scope of the agreement in RAN1 104-e regarding 480/960kHz PRACH to all cases (initial access and non-initial access case) without through discussion and justification. We believe that all operations during initial access should be carried out on the base numerology of 120 kHz.  If companies would like to expand the support of 480/960 kHz PRACH SCS to initial access cases, we can discuss this issue. However, such an issue should be discussed in RAN1 and the outcome (whether the support of 480/960 kHz PRACH SCS is limited to non-initial access case or is expanded to both initial access and non-initial access cases) should be provided to RAN2 in an LS so it can be reflected in RAN2 specifications. RAN2 has no means to decide whether or not a specific PRACH SCS is applicable only in non-initial access case or both initial and non-initial access cases.  As discussed in our views for Proposal 2.1-1), if necessary, we can further clarify the Agreement in RAN1 104-e using the following proposal:  **Proposal:**   * **The agreement in RAN1 104-e on the support for 480 and 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2 for non-initial access use case means that UE is not expected to be configured with 480/960 kHz SCS PRACH in initial UL BWP of a PCell provided in Type0-PDSCH.** * **FFS: Enhancements on PRACH configuration design for 480 and 960 kHz PRACH SCS.** |
| OPPO | Fine with the proposal. |

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| Futurewei | Please clarify the intention of the proposal with respect to the prior agreement on PRACH format for SCS 480/960 kHz for non-initial channel access as we already agreed the PRACH format for non-initial access case. |
| Lenovo, Motorola Mobility | Fine with the proposal 2.2-1 |
| Interdigital | We support the proposal. |
| CATT | Fine with 2.2-1. |
| Intel | Support the Proposal and fine to study L=571 and 1151.  One point here is the support of fixed wireless access in the US which allows to maximize the Tx power up to 27 dBm for signal bandwidths larger than 100 MHz (for the smaller bandwidths, the highest power level should be reduced from 27 dBm). Therefore, at least for SCS 480 kHz, L=571 should be supported (without contradiction with the agreed minimal system bandwidth) in order to achieve the max Tx power level of 27 dBm for fixed wireless access in the US.  Therefore, we suggest adding “support L=571 for 480kHz PRACH”.  We prefer to keep the FFS, as depending on response from RAN4 on the max EIRP and max conducted power pairs, RAN1 may find other PRACH sequence length necessary. |
| Ericsson | Again, Huawei has a point. We have agreed on support of 480/960 kHz PRACH at least for non-initial access use cases, so it seems we don’t need a re-agreement.  Regarding sequence lengths 571/1151, this translates to 274 / 552 MHz for 480 kHz SCS and 548 / 1105 MHz for 960 kHz. These bandwidth are excessive, and actually lead to degraded link budget. In the US, the conducted power limit of 27 dBm is achieved at 100 MHz, so it is not necessary to go to 274 MHz. In fact, the link budget degrades – no additional power, just additional noise.  Hence L = 571/1151 for 480/960 kHz are not motivated. |
| Sony | We support the proposal. |

#### **1st Round Discussion Summary:**

As Huawei noted, RAN1 has already agreed to support L=139 is supported for 480/960kHz PRACH. The only open question is other values. Most companies think L=139 is sufficient. Intel has commented the support for L=571 for 480kHz, while Ericsson comments that this is not needed.

#### **2nd Round Discussion:**

Moderator assumes previous RAN1 agreement means 480/960kHz PRACH will be specified in RAN1 specification, and RAN1 could go ahead with further development of RAN1 specification for 480/960kHz PRACH.

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| Agreement:   * For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2. * For non-initial access use cases,   + if 480kHz and/or 960 kHz SSB SCS is agreed to be supported, support 480 and/or 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively. |

If there are any different understanding, please comment further.

Also moderator asks companies to further provide comments on the L=571 for 480kHz PRACH.

* Should L=571 for 480kHz PRACH be supported to maximize (conducted) transmit power for US fixed wireless use cases?

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| **Company** | **Comment** |
| Samsung | We are ok with FL’s assessment.  For the additional question, we are ok to support L=571 for 480kHz PRACH. |
| Qualcomm | We have the same understanding as FL.  For the additional question, we do not see a need to support L=571 for 480kHz PRACH |
| Ericsson | We are OK with FL's assessment  Still, we don't think L = 571 is needed for 480 kHz as the PRACH bandwidth is excessive (274 MHz). It far exceeds the bandwidth for which the US conducted power limit maxes out at 27 dBm, i.e., 100 MHz. |

#### **2nd Round Discussion Summary:**

TBD

### 2.2.3 RACH Occasion Resources

* From [1] Huawei, HiSilicon:
  + Support maximum of 40 ms for ra-ResponseWindow for operation with shared spectrum and msgB-ResponseWindow for both operations with and without shared spectrum. Support indicating two LSBs of SFN at which gNB has received msg1 (msgA) in DCI format 1\_0 with CRC scrambled by RA-RNTI (msgB-RNTI).
  + For operations with shared channel access in 52.6GHz to 71GHz spectrum, a gap symbol between consecutive ROs within the PRACH slot should be supported to avoid a LBT failure at the UE due to a PRACH transmission from another UE in the previous RO.
* From [3] vivo:
  + For RO configuration for PRACH with 480/960kHz SCS:
  + Reuse the exiting FR2 RACH configuration table and the location of duration containing PRACH slot pattern within 10ms is same as FR2.
  + How to determine the RACH slot index:
    - Alt.1: Reuse the same reference slot as FR2 and maintain the same number of PRACH slots per reference slot.
    - Alt.2: Reuse the same reference slot as FR2 and increase the number of PRACH slots to more than 2 per reference slot.
    - Alt.3: Define a new reference slot and maintain the same number of PRACH slots per reference slot.
    - Alt.4: Define a new reference slot and increase the number of PRACH slots to more than 2 per reference slot.
    - Alt.5: Define different reference slot for different PRACH SCS and the number of PRACH slots within a reference slot is the same as FR2.
* From [5] Nokia, NSB:
  + Reuse the existing FR2 RACH configuration table and PRACH slot(s) for 480 and 960 kHz are allocated with the following principles where the reference SCS is 60 kHz:
    - If “Number of PRACH slots within a 60 kHz slot” is 1, then there is one PRACH slot with 480 or 960 kHz SCS among the slots defined by the 60 kHz reference slot
    - If “Number of PRACH slots within a 120 kHz slot” is 2, then there are two PRACHs slot with 480 or 960 kHz SCS among the slots defined by the 60 kHz reference slot.
* From [6] Ericsson:
  + For 480/960 kHz PRACH, support PRACH configurations that allow maintaining the same PRACH processing load (operations/unit time) as for 120 kHz PRACH configurations.
    - support configuration of PRACH occasion(s) in only 1 or 2 480/960 kHz slots within a 60 kHz reference slot.
  + For 480/960 kHz PRACH, reuse the current PRACH configuration table in 38.211 for FR2 "as is." Specify rule for which 1 or 2 480/960 kHz slots within a 60 kHz reference slot are used depending on the value in the existing column "Number of PRACH slots within a 60 kHz slot" in the current PRACH configuration table. The rule should be common for all PRACH configurations in the table.
* From [7] CATT:
  + For RO configuration support of 480/960 KHz, 120 KHz configuration can be reused for each 8/16 slots within the 60 KHz slot time.
* From [8] Qualcomm:
  + a maximum of 4 and 2 FD multiplexed ROs for SCS = 120 kHz and sequence length = 571 and 1151, respectively
  + for SCS = 120 kHz, if the maximum number of FD ROs are reduced, consider ways to increase the TD ROs (to maintain the same capacity) with minimal specification impact
  + for higher RACH SCS (480 and 960 kHz), consider including a symbol-level gap between ROs to allow for gNB beam switching delay
  + for higher RACH SCS (480 and 960 kHz), consider ways to support more than 2 RACH slots per RACH reference slot
* From [9] OPPO:
  + Set the reference SCS for RACH slot determination as 120kHz.
  + RAN1 should design a unified RO configuration for both licensed and unlicensed spectrums.
  + On top of RO configuration, a mask can be further added for unlicensed spectrum to switch off certain RO from being selected.
* From [10] ZTE, Sanechips:
  + Support the same RO configuration table as in Rel-15/16 with the same RO density as in PRACH SCS equals to 120KHz.
  + Support 60kHz for reference slot as in FR2 with the less spec effort in beyond 52.6G.
* From [11] Intel:
  + Regarding PRACH RO configurations for SCS 480 kHz and 960 kHz:
  + The numerology for reference slot counting within a system frame remains corresponding to SCS 60 kHz;
  + The max number of starting positions for PRACH slots within a reference slot (which has SCS 60 kHz) is equal to 2;
  + Fix the starting position(s) of PRACH slots within the reference slot by properly setting the values of parameter n\_{slot}^{RA} (TS 38.211, Section 5.3.2).
    - The starting position(s) should be aligned with the SSB slot patterns in order to avoid systematic overlapping between SSBs and ROs.
  + Reuse PRACH RO configurations listed in Table 6.3.3.2-4 from TS 38.211.
  + For PRACH SCS 480 kHz and 960 kHz, introduce optional time gaps between consecutive ROs;
  + Modify equation defining the first OFDM symbol of PRACH RO given Section 5.3.2 from TS 38.211 as follows:
    - ,
    - where is the gap duration (number of OFDM symbols) and for no gap.
* From [12] Fujitsu:
  + Support RO configuration for non-consecutive ROs in time domain.
* From [13] Apple:
  + Maximum 4 PRACH ROs can be configured for 120kHz SCS with L=571.
  + Maximum 2 PRACH ROs can be configured for 120kHz SCS with L=1151.
  + Reuse the existing FR2 PRACH configuration Table to indicate the time-domain PRACH slot location.
  + Support to keep the same PRACH capacity as Rel-16 FR2 for 480kHz and 960kHz SCS to minimize the signaling overhead.
  + The configured PRACH slots should be distributed over the 60kHz reference slot.
* From [16] Samsung:
  + Using the RO pattern for SCS = 120 kHz derived from the PRACH configuration table as the reference for larger SCS cases.
  + For RO configuration, both direction 1 (indication on which one(s) of the 8 eighty-slots or which one(s) of the eight 960 kHz ROs within a 120 kHz RO) and direction 2 (keep 80 slots in total but redesign the RACH period and RACH duration location) can be considered.
  + Support non-consecutive RO configuration to alleviate the RACH LBT failure.
* From [18] LGE:
  + If the reference slot SCS is kept as 60 kHz and the density of PRACH occasion is the same as in 120 kHz in the time-domain (e.g., 2 slots out of 8 slots for 480 kHz), the PRACH slot index for 480 and 960 kHz SCS can be determined based on the selected two values of with the pre-configured rule or based on the configured/indicated value(s) of by the gNB.
  + If the reference slot SCS is kept as 60 kHz and the density of PRACH occasion is increased compared to 120 kHz in the time-domain, the additional PRACH slots for 480 and 960 kHz SCS can be indicated/configured by the parameter X to allocate the consecutive X slots before the last slot ( for 480 and 960 kHz SCS, respectively).
  + When LBT is used to transmit the PRACH preamble, consider to insert CCA gap between adjacent RACH occasions in time domain (e.g. X usec or Y symbol) to avoid inter-UE LBT blocking due to the propagation delay of PRACH transmitted in an earlier RO.
* From [20] Xioami:
  + Inconsecutive RO time domain configuration should be supported.
* From [21] Interdigital:
  + For 52.6 – 71 GHz, supporting non-consecutive RACH occasions is not preferred.
* From [23] Sharp:
  + Regarding PRACH configuration design for 480/960kHz SCS, reuse Table 6.3.3.2-4 (Random access configurations for FR2 and unpaired spectrum) in Rel-16 38.211 as much as possible. 60kHz reference slot should be also inherited.
  + Regarding PRACH configuration design for 480/960kHz SCS, keep the same RO density and the same relative locations as PRACH configuration in Rel-16.
* From [25] NTT Docomo:
  + For RO configuration for PRACH with 480/960 kHz SCS,
    - Support to specify only 480/960 kHz PRACH slot within a 120 kHz referenced slot in addition to the existing RO configuration in FR2.
      * The 120 kHz referenced slot should be determined based on the existing RO configuration specified in FR2
      * Only one 480/960 kHz PRACH slot within the 120 kHz referenced slot is sufficient.
    - No need to enhance RA-RNTI calculation for NR operation in 52.6 – 71 GHz

#### Summary of Discussions

* Companies have provided several detailed proposals. Most of the proposals are suggestions and answers to several sub-issues. Moderator suggest to continue discussion with the following question list, and try to resolve each question during the RAN1 meeting.
  + RA response window size
  + For 120kHz RO, whether (and how) to support gap for LBT (if needed)
  + For 480/960kHz RO (if agreed), whether (and how) to support gap for LBT (if needed)
  + For 480/960kHz RO (if agreed), whether (and how) to support gap for beam switching (if needed)
  + How to determine the RACH slot index for 480/960kHz
  + Supported RO density for 480/960kHz PRACH per reference slot
  + SCS for reference slot for 480/960kHz PRACH RO
  + Any changes/updates to starting symbol positions of PRACH slots within reference slot

#### **1st Round Discussion:**

* Companies are encouraged to provide inputs on the following questions
  + Q1) RA response window size (e.g. 10msec, 20msec, etc)?
  + Q2) For 120kHz RO, whether (and how) to support gap for LBT (if needed)
  + Q3) For 480/960kHz RO (if agreed), whether (and how) to support gap for LBT (if needed)
  + Q4) For 480/960kHz RO (if agreed), whether (and how) to support gap for beam switching (if needed)
  + Q5) How to determine the RACH slot index for 480/960kHz
  + Q6) Supported RO density for 480/960kHz PRACH per reference slot
  + Q7) SCS for reference slot for 480/960kHz PRACH RO
  + Q8) Any changes/updates to starting symbol positions of PRACH slots within reference slot

Moderator will try to formulate proposal based on inputs from the companies.

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| **Company** | **Comment** |
| DOCOMO | Q1) Same as FR2 would be sufficient.  Q2 and Q3) Since Rel-16 NR-U did not introduce gap for LBT, we do not see the necessity for 60 GHz either.  Q4) Depending on RAN4 LS reply.  Q5) It should correspond to 120 kHz PRACH slot determined by FR2 RO configuration/  Q6) It should be the same as the one for 120 kHz PRACH RO per reference slot in FR2.  Q7) either 60 kHz or 120 kHz. Slightly prefer 120 kHz SCS.  Q8) we do not see the necessity to change anything on symbol position within reference slots. |
| Samsung | 1) configured by gNB, the value range can use the one from NRU Rel16 as starting point  2) support, by indicating the RO to be used in one RACH slot, e.g., even or odd RO;  3) and 4). Similar way as Q2;  5) down select from two ways: one is scaling 10ms-120khz PRACH pattern to fit the 2.5ms-480khz/1.25ms-960khz and find which 2.5ms/1.25ms location in 10ms; the other is indicating the 480khz/960khz RO within a 120khz RO;  6). keep it same as 120khz at least, FFS others  7). 120khz  8). FFS. It may be impacted by decision on above questions and we think it may not need discussion from reference slot level, we can discuss from RO with reference SCS. |
| LG | Q1) We prefer to keep the RAR window size as 10ms.  Q2 and Q3) The gap between the consecutive RO should be supported for 120/480/960 kHz SCS to avoid the inter-UE LBT blocking due to the propagation delay of PRACH transmitted in an earlier RO. The gap between the adjacent RACH occasions can be the fixed duration (e.g., X usec or Y symbol).  Q4) It would be better to defer the related discussion until RAN4 respond to RAN1’s LS.  Q5) If the reference slot SCS is kept as 60 kHz and the density of PRACH occasion is the same as in 120 kHz in the time-domain (e.g., 2 slots out of 8 slots for 480 kHz), the PRACH slot index for 480 and 960 kHz SCS can be determined based on the selected two values of with the pre-configured rule or based on the configured/indicated value(s) of by the gNB.  Q6) The density of PRACH occasion can be the same as in 120 kHz (e.g., 2 slots out of 8 slots for 480 kHz) or can be increased compared to 120 kHz.  Q7) Prefer 60 kHz and we would like to ask what is meaning of 120 kHz SCS reference slot to the proponent companies (i.e., what is the differences from 60 kHz SCS reference slot?).  Q8) We do not see the necessity. |
| Qualcomm | Q1) Same as FR2  Q2) No LBT gap needed  Q3) No LBT gap needed  Q4) Depending on RAN4 LS reply, but based on our analysis we see a need for beam switching gap  Q5) Due to gaps and/or coverage enhancement needs, more than 2 RACH slots per RACH reference slots may be needed (this may not necessarily lead to an increase of RACH processing load). We suggest that “determining the RACH slot index for 480/960kHz” be postponed to after the number of slots in a reference slot is finalized which may depends on the gap needs  Q6) This depends on the need to have more repetitions and/or the need for beam switching gaps  Q7) Can be the same as FR2 (60 kHz)  Q8) This depends on the need to have more repetitions and/or the need for beam switching gaps |
| Sharp | Q1) RA response window size (e.g. 10msec, 20msec, etc)?  10msec.  Q2) For 120kHz RO, whether (and how) to support gap for LBT (if needed)  No. The motivation (stronger than in NR-U) should be justified.  Q3) For 480/960kHz RO (if agreed), whether (and how) to support gap for LBT (if needed)  No. The motivation (stronger than in NR-U) should be justified.  Q4) For 480/960kHz RO (if agreed), whether (and how) to support gap for beam switching (if needed)  Come back with RAN4 decision.  Q5) How to determine the RACH slot index for 480/960kHz  Should be discussed after RO density and reference slot SCS are determined.  Q6) Supported RO density for 480/960kHz PRACH per reference slot  Same as 120kHz PRACH in FR2, as the baseline.  Q7) SCS for reference slot for 480/960kHz PRACH RO  60kHz.  Q8) Any changes/updates to starting symbol positions of PRACH slots within reference slot  Currently no. |
| Mediatek | Q1) Same as FR2  Q2) Gap for LBT is not needed  Q3) Gap for LBT is not needed  Q4) This discussion can be deferred until RAN4 respond to RAN1’s LS  Q5) We prefer to reuse the same reference slot as FR2 and see whether the number of PRACH slots is the same as that in FR2 per reference slot. So this question also depends on the RO configuration  Q6) The RO density can be the same as that in 120 kHz  Q7) Prefer same as FR2  Q8)  We don’t see strong need. |
| ZTE, Sanechips | Q1) Same as FR2  Q2) and Q3) No LBT gap needed  Q4) Wait for RAN4’s reply LS  Q5) It depends on the RO density and reference slot.  Q6) The same as 120kHz RO density in FR2  Q7) 60kHz, the same as in FR2, with that we can reuse the FR2 PRACH configuration table as much as possible  Q8) It’s not necessary for any changes |
| Fujitsu | Q1) Same as FR2  Q2) Support. By a configurable or fixed symbol gap, or by disable even/odd ROs.  Q3) Support. By same way as Q2.  Q4) Support. By same way as Q2.  Q5) This may depend on discussion on Q6 and Q7. If more than 2 RACH slots for 480/960kHz per reference slot is supported, it would be preferred to introduce additional indication to determine the RACH slot index for 480/960kHz.  Q6) This may depend on discussion on gaps in Q2-Q4, considering that the ‘RO density per reference slot’ includes two dimensions, one is number of ROs per slot, and the other is the number of RACH slots per reference slot. The baseline could be the maximum number of RO for 120kHz per 60kHz slot for FR2. If the gap is needed, the maximum number of ROs per RACH slot would be reduced, and then more than 2 RACH slots per reference slot should be supported.  Q7) 60 kHz  Q8) This may depend on discussion on gaps in Q2-Q4. |
| Nokia | Q1) For unlicensed operation the NR-U methodology can be a starting point.  Q2)&Q3) We would prefer to define fixed LBT gap time between valid ROs that do not depend on the time domain allocation of the PRACH.  Q4) We don’t see a need for this but would wait for RAN4 feedback.  Q5) Reuse the existing FR2 RACH configuration table and PRACH slot(s). The slot (of 480/960kHz) would be placed to the last slot overlapping with the corresponding 120kHz slot.  Q6) Same as for 120kHz in FR2.  Q7) 60kHz.  Q8) No changes. |
| Xiaomi | Q1) Same as FR2  Q2-4) Support define LBT gap, especially for new SCS by configuration.  Q5-6) Reuse FR2  Q7-8）FFS |

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| Huawei, HiSilicon | Q1) Similar to Rel-16: Support maximum of 40 ms for ra-ResponseWindow for operation with shared spectrum and msgB-ResponseWindow for both operations with and without shared spectrum.  Q2) Yes. 1 symbol gap between consecutive ROs.  Q3) 480/960kHz PRACH is already agreed for non-initial access cases in RAN1 104-e. Yes. Support gap between consecutive ROs for LBT.  Q4) 480/960kHz PRACH is already agreed for non-initial access cases in RAN1 104-e. Yes. Support 1 symbol gap between consecutive ROs for beam switching at least for 960 kHz SCS.  Q5) We think Q6 should be agreed first.  Q6) We support a higher RO density than in 120 kHz. That is, the number of 480/960 kHz SCS PRACH slots in a reference slot should be higher than the number of 120 kHz SCS PRACH slots in the same reference slot.  Q7) Can remain 60 kHz.  Q8) FFS. We may have to if gap for LBT and/or beam switching is required. |
| OPPO | Q1) Same as FR2  Q2) Q3) Q4): Support gap for LBT by RO configuration  Q5) Based on RO configuration in a 120kHz RACH slot  Q6) The configuration of 480/960kHz RO should also based on a 120kHz RACH slot  Q7) 120kHz  Q8) FFS |

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| Futurewei | Q1) Same as FR2  Q2) No LBT gap is needed  Q3) No LBT gap is needed  Q4) Depending on RAN4 reply  Q5) Discuss it later after RO density and reference slot decision.  Q6) Same as for 120 kHz SCS in FR2  Q7) Same as in FR2, 60 kHz  Q8) FFS |
| CATT | Q1) Same as FR2  Q2) No LBT gap is needed  Q3) No LBT gap is needed  Q4) FFS based on RAN4 feedback  Q5) Discuss it after decision about RO density and reference slot.  Q6) The configuration of 480/960kHz can be based on the 120kHz RO.  Q7) 60 kHz  Q8) Do not see the necessity for the change. |
| Intel | Q1) Same as in FR2  Q2) No LBT gap needed  Q3) No LBT gap needed  Q4) Configurable beam switching gap may be needed  Q5) Set properly the values of parameter and reuse RO configurations from Table 6.3.3.2-4 of TS 38.211  Q6) Strive to keep the number of ROs within the reference slot the same as for SCS 120 kHz. However, the number of occupied RACH slot could be larger, e.g., because of gaps introduced between consecutive ROs  Q7) 60 kHz  Q8) The max number of starting positions for PRACH slots within a reference slot is the same as for SCS 120 kHz |
| vivo | Q1) Same as FR2.  Q2) and Q3) For the LBT gap, it should be supported for 120/480/960 kHz to avoid LBT failure due to the utilizing of the previous RO. By defining a fixed gap between the consecutive ROs.  Q4) For the beam switching gap, we should wait for RAN4’s LS reply.  Q5) The RACH slot index for 480/960kHz depends on the reference slot and the number of PRACH slot per reference slot. We can further discuss the details after the two parameters are determined.  Q6) Increase the RO density for 480/960kHz PRACH per reference slot compared to 120 kHz to improve the access rate.  Q7) Same as FR2 (60 kHz).  Q8) FFS. It depends on whether to support non-consecutive ROs for LBT gap and/or beam switching gap and how to configure. |
| Ericsson | Q1) Same as FR2  Q2) We do not see a need for LBT gap. PRACH should fall under short control signal exemption.  Q3) We do not see a need for LBT gap. PRACH should fall under short control signal exemption.  Q4) We do not see a need for beam switching gap. However, we acknowledge that feedback from RAN4 is still pending, hence difficult to make progress here.  Q5) For 480/960 kHz PRACH, reuse the current PRACH configuration table in 38.211 for FR2 (Table 6.3.3.2-4) "as is." Specify rule for which 1 or 2 480/960 kHz slots within a 60 kHz reference slot are used depending on the value in the existing column "Number of PRACH slots within a 60 kHz slot" in the current PRACH configuration table. The rule should be common for all PRACH configurations in the table. For example, for the case of 2 480/960 kHz slots, they could be the last ones within the 1st and 2nd half of the reference 60 kHz slot as shown in this figure. For the case of 1 480/960 kHz slot, it could be just the last one within the 60 kHz reference slot.    Q6) We have a strong preference to support the same RO density as FR2 since we don't think the number of needed RACH opportunities scales with SCS. Furthermore, we prefer not to increase the PRCH processing load at the gNB. Reusing the FR2 PRACH configuration table with only 1 or 2 480/960 slots within a 60 kHz reference slot achieves the goal of maintaining the same RO density as FR2.  Q7) In order to reuse the existing PRACH configuration table for 120/480/960 kHz PRACH, we support maintaining the SCS of the reference slot to be 60 kHz as illustrated above.  Q8) Can reuse existing starting symbol positions as specified in the current PRACH configuration table in 38.211 for FR2 |
| Sony | Q1) Same as in FR2  Q2) No LBT gap is needed  Q3) No LBT gap is needed  Q4) wait for RAN4 replay  Q5) it depends on RO density and reference slot.  Q6) same as FR2  Q7) 60 kHz  Q8 we don’t see the necessity of change. |

#### **1st Round Discussion Summary:**

Summary of responses from companies are provided below.

* Q1) RA response window size (e.g. 10msec, 20msec, etc)?
  + Same as FR2: Docomo, Qualcomm, Mediatek, ZTE, Sanechips, Fujitsu, Xiaomi, OPPO, Futurwei, CATT, Intel, vivo, Ericsson, Sony
  + Same as FR1 NR-U: Nokia, NSB
  + Configured by gNB: Samsung
  + 10msec: LGE, Sharp
  + Max 40msec: Huawei, HiSilicon
* Q2) For 120kHz RO, whether (and how) to support gap for LBT (if needed)
  + No need: Docomo, Qualcomm, Sharp, Mediatek, ZTE, Sanechips, Futurwei, , CATT, Intel, Ericsson, Sony
  + Support: Samsung (even/odd RO indication), LGE, Fujitsu, Nokia, NSB, Xiaomi, Huawei, HiSilicon, OPPO, vivo
* Q3) For 480/960kHz RO (if agreed), whether (and how) to support gap for LBT (if needed)
  + No need: Docomo, Qualcomm, Sharp, Mediatek, ZTE, Sanechips, Futurwei, CATT, Intel, Ericsson, Sony
  + Support: Samsung, LGE, Fujitsu, Nokia, NSB, Xiaomi, Huawei, HiSilicon, OPPO, vivo
* Q4) For 480/960kHz RO (if agreed), whether (and how) to support gap for beam switching (if needed)
  + Wait for RAN4 reply LS: Docomo, LGE, Qualcomm, Sharp, Mediatek, ZTE, Sanechips, Nokia, NSB, Futurwei, CATT, vivo, Ericsson, Sony
  + Support: Samsung, Fujitsu, Xiaomi, Huawei, HiSilicon, OPPO, Intel
* Q5) How to determine the RACH slot index for 480/960kHz
  + Scale 10msec 120kHz PRACH pattern to 2.5msec 480kHz 1.25msec 960kHz PRACH: Samsung
  + Indicate 480/960kHz PRACH RO within 120kHz RO instance: Samsung, LGE, [OPPO], Intel
  + FFS: Qualcomm (depend on RAN4 reply LS), Sharp, Mediatek, ZTE, Sanechips, Fujitsu, Huawei, HiSilicon, Futurwei, CATT, vivo, Sony
* Q6) Supported RO density for 480/960kHz PRACH per reference slot
  + Same as density for 120kHz PRACH RO per reference slot: Docomo, Samsung, LGE, Sharp, Mediatek, ZTE, Sanechips, Nokia, NSB, Xiaomi, OPPO, Futurwei, CATT, Ericsson, Sony
  + Higher density than 120kHz PRACH RO per reference slot: Huawei, HiSilicon
  + FFS: Qualcomm (depend on RAN4 reply LS) , Fujitsu
* Q7) SCS for reference slot for 480/960kHz PRACH RO
  + 120kHz: Docomo, Samsung, OPPO
  + 60kHz: LGE, Qualcomm, Sharp, ZTE, Sanechips, Fujitsu, Nokia, NSB, Huawei, HiSilicon, Futurwei, CATT, Intel, vivo, Ericsson, Sony
  + FFS: Xiaomi
* Q8) Any changes/updates to starting symbol positions of PRACH slots within reference slot
  + No need: Docomo, LGE, Sharp, Mediatek, ZTE, Sanechips, Nokia, NSB, CATT, Ericsson, Sony
  + Needed: Intel (account for beam switching gap)
  + FFS: Samsung, Qualcomm (depend on RAN4 reply LS), Fujitsu, Xiaomi, Huawei, HiSilicon, Futurwei, vivo

#### **2nd Round Discussion – Part 1:**

For RAR window sizes, numerous companies stated same as FR2. In Rel-15/16 NR, the supported RAR window sizes are:

* From Rel-15: 1, 2, 4, 8, 10, 20, 40, 80 slots
* From Rel-16: 60, 160 slots
* The network configures
  + a value lower than or equal to 10 ms when Msg2 is transmitted in licensed spectrum,
  + and a value lower than or equal to 40 ms when Msg2 is transmitted with shared spectrum channel access (see TS 38.321 [3], clause 5.1.4).

Since FR2 does not contain any shared spectrum channel access, this seems to imply that RAR window need to be lower than 10msec. However, it was not clear if all companies had the same understanding. Therefore, moderator would like to ask companies again to clarify their preferences.

##### **Proposal 2.3-1)**

* For NR 52.6 ~ 71 GHz random access, support all Rel-15 and Rel-16 RAR window lengths (i.e. 1, 2, 4, 8, 10, 20, 40, 60, 80, 160 slots),
  + Alt 1) and network configures a value lower than or equal to 10 msec
    - What is available in current FR2
  + Alt 2) and network configures a value lower than or equal to 40 msec
    - What is available in current FR1 NR-U

Please provide further comments on which alternative companies are supportive of. If the preference is something else, please provide information on the preferred values.

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| **Company** | **Comment** |
| Samsung | We support Alt 1 for licensed band, and Alt 2 for unlicensed band. |
| Qualcomm | We support Alt 1 for licensed and unlicensed bands. 40ms was introduce in NR-U to allow some more time for gNB to send RAR, in case gNB has problem accessing channel due to LBT. We don’t believe the issue exists here. |
| Ericsson | We support Alt-1 for both licensed and unlicensed. We don't think extended RAR is as beneficial for the 52.6 – 71 GHz band since LBT failure is very rare. No need to optimize for LBT failure. |

#### **2nd Round Discussion – Part 1:**

Views on regarding RO definition to account for LBT and beam switch gap seem quite split, and require further discussions. On determination of RACH index for 480/960kHz, most companies seem to favor keeping the same density as 120kHz PRACH. Moderator has formulated a proposal based on inputs received.

##### **Proposal 2.3-2)**

* For 480kHz and 960kHz PRACH,
  + RACH slot index corresponds to one of the slots within 120kHz RO instance, and
  + has the same RO density (i.e. number of RO opportunity) for 480/960kHz PRACH per reference slot of 60kHz as 120kHz PRACH per reference slot
    - FFS: higher RO density for 480/960kHz PRACH is additionally supported
  + FFS: starting symbol position, , of PRACH slots within reference slot
  + FFS: whether and how to account for LBT in RO configuration (if needed)
  + FFS: whether and how to account for beam switching gap in RO configuration (if needed)
  + An “example” illustration of RO for 480/960kHz is shown below:



Please comment further on Proposal 2.3-2 and use it as starting point for further discussions.

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| **Company** | **Comment** |
| Samsung | We believe there are some typo on the section index and proposal index. Seems the correct section title should be “Part 2”, and the proposal index should be 2.3-2.  We have some comments on this proposal:   * We have difficulty to understand the first bullet, “one of the slots within 120 kHz RO instance”, what is the “slots within 120 KHz RO instance”? The wording seems need to be improved for clarify. * For the second bullet, is the intention to say that having the same RO density as the PRACH configuration when using 120 khz? * The drawback to use 60 khz as the “reference slot” is that, we will need larger (double) size of the indication signaling, e.g., eight 480khz ROs per one 60khz RO, but only four 480 khz ROs per one 120khz RO. We don’t see any benefits to use 60khz over 120 khz as reference SCS. |
| Qualcomm | We support this proposal |
| Ericsson | We agree with the direction of this proposal, but we think it could benefit from some clarification as pointed out by Samsung.  Maybe the first thing to do is agree that the reference slot duration corresponds to 60 kHz SCS (same as for the PRACH configuration table defined for FR2). Of course this does not mean that PRACH for 52.6 – 71 GHz supports 60 kHz SCS; it is simply a reference slot duration for defining how many PRACH slots occur within this duration. In FR2 for 120 kHz PRACH there can be either 1 or 2 PRACH slots (second half or both halves of the 60 kHz reference slot). Which half or halves of this reference slot are used is specified in 38.211 Section 5.3.2 with the following:  -  is given by  - if kHz, then  - if kHz and either of "Number of PRACH slots within a subframe" in Tables 6.3.3.2-2 to 6.3.3.2-3 or "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then  - otherwise,  The highlighted spec text says that if the "Number of PRACH slots within a 60 kHz slot" is 1, then the second half of the 60 kHz reference slot is used; otherwise if it is 2, then both halves of the 60 kHz reference slot are used.  Samsung raises a concern that this will need larger (double) size of indication signaling, but that is not true. In FR2, the indication signaling for a PRACH configuration is a PRACH configuration index that points to one of the 256 rows in the PRACH configuration table. Once the row is indicated, the number of PRACH slots within a 60 kHz reference slot is fully determined – either 1 or 2 as already mentioned (see the highlighted column in an extract of the PRACH configuration table 6.3.3.2-4 copied at the bottom of this table).  Maybe the 2nd thing we can do is agree to reuse the current FR2 defined table that assumes 60 kHz reference slots. Then there is no need to increase any indication signaling overhead. In fact there is no need to change anything in the table either. All that is needed is to add a rule to the above on which 480/960 kHz slots within the 60 kHz reference slot are used.  e.g., the above spec text for 38.211 Section 5.3.2 could be augmented as follows (corresponds to the example illustration in the proposal)  - if then if "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, and if "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 2.  - if then if "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, and if "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 2.  If it is agreeable to the group to use 60 kHz reference slot (as in FR2), perhaps the proposal could be clarified as follows: **Proposal 2.3-2)**  * For 480kHz and 960kHz PRACH,   + The reference slot duration corresponds to 60 kHz SCS   + A PRACH slot index, , corresponds to one of the 480/960 kHz PRACH slots within the reference slot ~~120kHz RO instance~~, and   + 480/960 kHz PRACH has the same ~~RO~~ density (i.e. number of ~~RO~~ PRACH slots per reference slot ~~opportunity~~) ~~for 480/960kHz PRACH per reference slot of 60kHz~~ as for 120kHz PRACH in FR2 ~~per reference slot~~     - FFS: higher ~~RO~~ density for 480/960kHz PRACH is additionally supported   + FFS: supported values of the PRACH slot index ~~starting symbol position, , of PRACH slots~~ within reference slot   + FFS: whether and how to account for LBT in RO configuration (if needed)   + FFS: whether and how to account for beam switching gap in RO configuration (if needed)   + An “example” illustration of ~~RO~~ PRACH slots for 480/960kHz is shown below: |

#### **2nd Round Discussion Summary:**

TBD

### 2.2.4 RA Preamble ID calculation

* From [3] vivo:
  + For larger PRACH SCS (480KHz/960KHz), the following options can be considered for RA-RNTI calculation:
    - Alt.1: Modify the RA-RNTI formula as following and introduce some contention resolution mechanism to resolve the conflict.
      * RA-RNTI = (1+s\_id+14×t\_id+14×X×f\_id +14×X×8×ul\_carrier\_id) mod A
    - Alt.2: Reuse the current RA-RNTI formula while introducing additional indicator field to indicate the time-frequency resource together with RA-RNTI.
    - Alt.3: Depending on the RO configuration pattern, reuse the RA-RNTI formula and express the slot indexes t\_id based on a new specific subcarrier spacing.
* From [5] Nokia, NSB:
  + Reuse RA-RNTI formula defined for 120 kHz SCS also for the cases PRACH is configured with 480 or 960 kHz SCS where
    - s\_{id} assumes 480/960 kHz SCS
    - t\_{id} assumes 120 kHz SCS
* From [6] Ericsson:
  + For 480/960 kHz PRACH, reuse the RA-RNTI expressions from Rel-15/16, with the additional statement that for 480/960 kHz PRACH, t\_id should be determined based on a subcarrier spacing of 120 kHz.
* From [7] CATT:
  + For supporting Msg1 transmission with 480 KHz/960 KHz SCS, RA-RNTI is divided into two parts. One part of RA-RNTI is carried by DCI, and the remaining 16-bit of RA-RNTI could be used to scramble CRC of the DCI1. Two possible options are:
  + Option A:
    - s\_id is the index of the first OFDM symbol of the PRACH occasion (0 ≤ s\_id < 14)
    - t\_id is the index of the first slot of the PRACH occasion in a system frame (0 ≤ t\_id < 640)
  + Option B:
    - s\_id is the index of the first OFDM symbol of the PRACH occasion (0 ≤ s\_id < 14)
    - t\_id is the index of the first slot of the PRACH occasion in a system frame (0 ≤ t\_id < 640)
* From [10] ZTE, Sanechips:
  + For higher PRACH SCS (480 and/or 960 kHz), consider the following options for RA-RNTI enhancements:
    - Option 1: Modification of t\_id, change the equation of RA-RNTI calculation, without additional signalling overhead
    - Option 3: Multiple RO blocks (segmented RO blocks) with indication. Reuse the same RA-RNTI equation in NR Rel-16, divide the system frame into N segments (each segment is 80 slots using the used SCS), and signal the segment index that transmit the preamble in the DCI.
* From [11] Intel:
  + RA-RNTI computation equation should be adjusted to avoid overflow in case of PRACH SCS 480 kHz and 960 kHz;
  + Support the following modified equation for RA-RNTI computation:
    - RA-RNTI = 1 + s\_id + 14 × floor(t\_id / ) + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id,
    - where t\_id is based on the value of specified in clause 5.3.2 of TS 38.211.
* From [12] Fujitsu:
  + If 480kHz/960kHz PRACH SCS is supported, the following should be considered to uniquely identify a RO:
    - When calculating RA-RNTI, t\_id is determined in a way that more than one slot can have the same t\_id; and
    - DCI scheduling RAR indicates the local index among the slots having the same t\_id.
* From [13] Apple:
  + modifying the existing calculation equation to solve the RA-RNTI overflowing problem:
* From [18] LGE:
  + If the reference slot SCS remains as 60 kHz and the density of PRACH occasion is the same as in 120 kHz in the time-domain (e.g., 2 slots out of 8 slots for 480 kHz), the existing RA-RNTI/MSGB-RNTI equation can be reused for 480 and 960 kHz SCS by reinterpreting the slot indexes t\_id based on a new specific subcarrier spacing as the slot indexes of 120 kHz SCS (e.g., floor(t\_id/n) where n=4 for 480 kHz SCS and n=8 for 960 kHz).
  + If the reference slot SCS remains as 60 kHz and the density of PRACH occasion is increased compared to 120 kHz in the time-domain, to calculate RA-RNTI/MSGB-RNTI associated with the PRACH occasion for 480 and 960 kHz SCS using the existing RA-RNTI equation, the following options can be considered:
    - Option 1: Divide the RAR window into N sub-periods (where each sub-period is 80 slots using the used SCS) + signal the sub-period index using the DCI that schedules the MSG2/MSGB.
    - Option 2: Divide the frequency index or the symbol index into M subset (if M=4, the subset index 0/1/2/3 can be configured to the frequency index {0, 1}, {2, 3}, {4, 5}, {6, 7}, respectively) + signal the subset index using the DCI that schedules the MSG2/MSGB
* From [23] Sharp:
  + Assuming RO density per reference slot is unchanged, without modifying the formula and definition of s\_id. Modify the definition of t\_id as the slot index referring to 120kHz SCS.

#### Summary of Discussions

* In case 480/960 kHz SCS is supported for PRACH, it was identified existing RA-RNTI calculation will have overflow issue. One of more of the following options were considered by companies to resolve this issue.
  + Option 1) Modify the RA-RNTI formula as following and introduce some contention resolution mechanism to resolve the conflict.
    - RA-RNTI = (1+s\_id+14×t\_id+14×X×f\_id +14×X×8×ul\_carrier\_id) mod A
  + Option 2) multiple RO blocks (segmented RO blocks) with indication in RAR
  + Option 3) update how t\_id, s\_id is determined (t\_id computed based on 120kHz, s\_id computed based on 480/960kHz)
  + Option 4) modulous operation on whole RA-RNTI
  + Option 5) modulous operation on t\_id
  + Option 6) scaled and floored operation on t\_id (e.g. floor(t\_id / ))
* Moderator suggest if single solution is not agreeable, then to refine the different options (describe more precisely) and list all options for down-select in the future RAN1 meeting.

#### **1st Round Discussion:**

Moderator would like to ask companies to precisely list the solutions that companies are considering. Moderator will capture them as options for down-select in future RAN1 meeting.

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| **Company** | **Comment** |
| DOCOMO | Support Option 3. |
| LG | We support the Option 3) and Option 6). |
| Qualcomm | This is highly dependent on the RO design (number of RACH slots in a reference slot, reference slot SCS, etc…). Recommend to defer this discussion until the RO design is final |
| Sharp | Generally, since some options are relevant to RO design modification while other options are not, as a result the comparison among options is dependent on RO design modification.  Under the assumption that PRACH number per 120kHz slot is kept the same, we can support Option 3 for the minor specification impact. |
| Mediatek | Prefer option 3, but also agree to defer this discussion until 2.2.3 is determined. |
| ZTE, Sanechips | We prefer Option 2) and Option 5). Also fine to defer this discussion. |
| Fujitsu | We prefer Option 2. And we agree to defer this discussion. |
| Nokia | We would support option 3), but we should probably conclude the afore discussion first. |
| OPPO | Depends on the outcome of section 2.2.3. |

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| Futurewei | Depends on the outcome of section 2.2.3. We prefer to use Rel 16 NR-U values  ra-ResponseWindow-v1610 ENUMERATED {sl60, sl160}  which lead to  RA-RNTI = (1+s\_id+14×t\_id+14×160×f\_id +14×160×8×ul\_carrier\_id)  With additional bits in DCI format 1\_0 to extend it if necessary, as in NR-U. |
| Lenovo, Motorola Mobility | We support Option 3 |
| CATT1 | Prefer to defer this discussion. |
| Intel | Option 6 is our preference. |
| vivo | This depends on RO configuration outcome. Better to defer this discussion. |
| Ericsson | Since we propose to reuse the FR2 PRACH configuration table "as is" and also adopting a rule to only have 1 or 2 480/960 PRACH slots within a 60 kHz reference slot, the only update that is needed to the RA-RNTI formula is that t\_id should be determined based on SCS 120 kHz.  Hence, the closest option for us is Option 3 (note s\_id is 0..14, so is agnostic to SCS since all slots, regardless of SCS have 14 symbols).  Agree with Nokia, we need to conclude the discussion in Section 2.2.3 first. |

#### **1st Round Discussion Summary:**

With the confirmation that 480/960kHz PRACH is supported in RAN1 specification. RAN1 needs to further discuss methods to mitigate RA-RNTI calculation overflow.

The following is a summary of company views.

* + Option 1) Modify the RA-RNTI formula as following and introduce some contention resolution mechanism to resolve the conflict.
    - RA-RNTI = (1+s\_id+14×t\_id+14×X×f\_id +14×X×8×ul\_carrier\_id) mod A
  + Option 2) multiple RO blocks (segmented RO blocks) with indication in RAR
    - ZTE, Sanechips
  + Option 3) update how t\_id, s\_id is determined (t\_id computed based on 120kHz, s\_id computed based on 480/960kHz)
    - Docomo, Mediatek, Sharp, Nokia, NSB, Lenovo, Motorola Mobility, Ericsson, LGE
  + Option 4) modulous operation on whole RA-RNTI
  + Option 5) modulous operation on t\_id
    - ZTE, Sanechips
  + Option 6) scaled and floored operation on t\_id (e.g. floor(t\_id / ))
    - Intel, LGE

Few companies commented that details of the RO configuration may need to be finalized before concluding on the solution for RA-RNTI calculation issue.

#### **2nd Round Discussion:**

Given that RO configuration design may have some impact on the down selection of the RA-RNTI calculation solution, moderator suggest to list the potential solutions.

##### **Proposal 2.4-1)**

* Further study the following solutions to resolve RA-RNTI overflow for 480/960kHz PRACH:
  + Option 1)
  + Option 2)
    - Segment the PRACH into N segments
    - In DCI:
  + Option 3)
    - Segment the PRACH into N segments
    - In DCI:
  + Option 4)
    - is the index of the first 120kHz slot that contains the PRACH occasion in a system frame.
    - is the index of the first OFDM symbol of the PRACH occasion based on the value of specified in clause 5.3.2 of TS 38.211.
  + Option 5)
    - RA-RNTI = 1 + s\_id + 14 × floor(t\_id / ) + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id,
    - t\_id is based on the value of specified in clause 5.3.2 of TS 38.211.

Please comment further if moderator has missed any other solutions, or incorrectly captured the solution suggested by the companies.

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| --- | --- |
| **Company** | **Comment** |
| Samsung | Is the design of RO configuration surely impacting the change to RA-RNTI? If not, we are not ready to spend effort on identifying the changes to RA-RNTI calculation. We believe this issue should be discussed (if needed) after the issues in Section 2.2.3 are settled down, while we appreciated FL and companies’ effort on listing the options. |
| Qualcomm | This is highly dependent on the RO design (number of RACH slots in a reference slot, reference slot SCS, etc…). Recommend to defer this discussion until the RO design is final |
| Ericsson | We also appreciate the effort of the moderator on listing options; however, we agree with Samsung, that it is too early to make progress on RA-RNTI has it is tightly coupled to the PRACH configuration design. If the same design is reused from Rel-15 FR2 with only 1 or 2 PRACH slots per reference slot, then very minimal change is needed to the RA-RNTI calculation. If a more complexity design is adopted, then RA-RNTI calculation would also need more changes.  Question: in the new list of options in this proposal, we wonder where the original Option 3 went?  In fact, if the the same design on PRACH configuration is used from Rel-15 FR2, the only change that is needed to RA-RNTI is that t\_id assumes 120 kHz. Nothing more. |

#### **2nd Round Discussion Summary:**

TBD

### 2.2.5 Other aspects on PRACH

* From [5] Nokia, NSB:
  + Support SCSe for PRACH transmissions and consider how gNB can control use of SCSe for PRACH transmissions so that the maximum limit for the SCSe transmissions can be kept
  + If LBT gaps are needed between ROs, it would be better to define fixed LBT gap time between valid ROs that do not depend on the time domain allocation of the PRACH. In that case the LBT gap length would not depend on the used PRACH format.
* From [11] Intel:
  + Consider applying short control signal exemption to PRACH transmission by the UE.

#### Summary of Discussions

* Companies have provided discussion on considerations for PRACH design. The discussion includes, application of short control signal exemption for PRACH, and enable/disable of LBT for PRACH.

#### **1st Round Discussion:**

Moderator suggest to discuss the application of short control signal exemption in channel access agenda. If there are any other issues related to PRACH that requires discussion, please provide suggestions and inputs below.

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| **Company** | **Comment** |
| Qualcomm | For SCS = 120 kHz, a maximum of 4 and 2 FD multiplexed ROs can be used for sequence length = 571 and 1151, respectively, thus, the maximum number of FD ROs are reduced. Consider ways to increase the TD ROs (to maintain the same capacity) with minimal specification impact |

#### **1st Round Discussion Summary:**

Not to many companies have provided additional issues for discussion.

#### **2nd Round Discussion:**

Suggest continuing discussion and also comment on issue pointed out by Qualcomm.

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| **Company** | **Comment** |
| Qualcomm | To further motivate the issue pointed out in the first round, the following are the straightforward options:   * Option A: Re-use the existing design but use larger association period   + This may slow down initial access and increase UE power consumption * Option B: Explicitly add more reference slots in a configuration period in Table 6.3.3.2-4 in TS 38.211   + Non-trivial spec work/time   Both options have issues and some more specification impact friendly approaches may be needed. In our paper, we have proposed:   * Add more reference slots in a configuration period by:   + Alt 1: adding N additional slots every M reference slot​     - Reuse existing Table 6.3.3.2-4 in TS 38.211​ (minimal spec impact)     - N and M can be specified or indicated​     - Example: PRACH Config. Index 0:​       * Current table: Slot number = 4,9,14,19,24,29,34,39​       * New values (N = 1, M = 2): Slot number = 4,5, 9,14,15,19,24,25, 29,34,35,39​   + Alt 2: adding one or more offseted version(s) (offset = L) of the slot number pattern to the existing one​     - Reuse existing Table 6.3.3.2-4 in TS 38.211​ (minimal spec impact)     - L can be specified or indicated and can be either added or subtracted to the existing slot number​     - Example: PRACH Config. Index 0:​       * Current table: Slot number = 4,9,14,19,24,29,34,39​       * New values (L = 2): Slot number = 2,4,7,9,12,14,17,19,22,24,27,29,32,34,37,39​ |
| Ericsson | We don't think such an approach suggested by Qualcomm is needed. A reduction in frequency domain ROs is a consequence of using longer sequences, but if this is a problem a, shorter sequence can be used. In other words, there are sufficient configurability tools in the spec to trade off RACH capacity/coverage. It is not needed to fundamentally change the PRACH configuration table or significantly alter interpretations of the table (which will lead to very long discussions). |

#### **2nd Round Discussion Summary:**

TBD

# Summary of Agreements/Conclusions in RAN1 #105-e

TBD

# Reference

1. R1-2104210, “Initial access for Beyond 52.6GHz,” FUTUREWEI
2. R1-2104273, “Initial access signals and channels for 52-71GHz spectrum,” Huawei, HiSilicon
3. R1-2104348, “Discussions on initial access aspects for NR operation from 52.6GHz to 71GHz,” vivo
4. R1-2104416, “Discussion on initial access aspects for NR for 60GHz,” Spreadtrum Communications
5. R1-2104452, “Initial access aspects,” Nokia, Nokia Shanghai Bell
6. R1-2104460, “Initial Access Aspects,” Ericsson
7. R1-2104507, “Initial access aspects for up to 71GHz operation,” CATT
8. R1-2104659, “Initial access aspects for NR in 52.6 to 71GHz band,” Qualcomm Incorporated
9. R1-2104765, “Discusson on initial access aspects,” OPPO
10. R1-2104833, “Discussion on the initial access aspects for 52.6 to 71GHz,” ZTE, Sanechips
11. R1-2104894, “Discussion on initial access aspects for extending NR up to 71 GHz,” Intel Corporation
12. R1-2105061, “Considerations on initial access for NR from 52.6GHz to 71 GHz,” Fujitsu
13. R1-2105092, “Discussion on Initial access signals and channels,” Apple
14. R1-2105156, “Considerations on initial access aspects for NR from 52.6 GHz to 71 GHz,” Sony
15. R1-2105260, “Discussion on initial access aspects supporting NR from 52.6 to 71 GHz,” NEC
16. R1-2105297, “Initial access aspects for NR from 52.6 GHz to 71 GHz,” Samsung
17. R1-2105370, “Discussion on initial access of 52.6-71 GHz NR operation,” MediaTek Inc.
18. R1-2105419, “Initial access aspects to support NR above 52.6 GHz,” LG Electronics
19. R1-2105495, “Initial access aspects for NR from 52.6 GHz to 71GHz,” Lenovo, Motorola Mobility
20. R1-2105555, “On initial access aspects for NR from 52.6GHz to 71 GHz,” Xiaomi
21. R1-2105581, “Discussions on initial access aspects,” InterDigital, Inc.
22. R1-2105592, “NR Initial Access from 52.6 GHz to 71 GHz,” Convida Wireless
23. R1-2105630, “Initial access aspects,” Sharp
24. R1-2105660, “On the importance of inter-operator PCI confusion resolution and ANR support in 52.6 GHz and beyond,” AT&T
25. R1-2105688, “Initial access aspects for NR from 52.6 to 71 GHz,” NTT DOCOMO, INC.
26. R1-2105786, “Further details of initial access for NR above 52.6 GHz,” Charter Communications
27. R1-2105868, “Discussion on initial access aspects for NR beyond 52.6GHz,” WILUS Inc.
28. R1-2105988, “On the importance of inter-operator PCI confusion resolution and ANR support in 52.6 GHz and beyond,” AT&T, NTT DOCOMO, INC., T-Mobile USA