**3GPP TSG-RAN WG1 Meeting #105-eR1-210xxxx**

**e-Meeting, May 10th – 27th, 2021**

**Agenda item:** **7.1**

**Source: Moderator (Apple Inc.)**

**Title: Summary of email discussion [105-e-NR-7.1CRs-13] on the correction for HARQ-ACK timing in Rel-16**

**Document for: Discussion and Decision**

# 1 Introduction

This contribution provides the summary for the following email discussion in RAN1#105-e:

**Issue#28**

[R1-2105075](file:///C:\Users\wanshic\OneDrive%20-%20Qualcomm\Documents\Standards\3GPP%20Standards\Meeting%20Documents\TSGR1_105\Docs\R1-2105075.zip) Correction for HARQ-ACK timing in Rel-16 Apple, Ericsson

[105-e-NR-7.1CRs-13] Issue#28: Correction for HARQ-ACK timing in Rel-16 – Sigen (Apple) by May 25

* For Rel-16 only

Section 2 provides the background information. Section 3 captures the detailed email discussions. Section 4 summarizes the outcome of the email discussion.

# 2 Background

For HARQ-ACK, the PUCCH for HARQ-ACK is transmitted in UL slot *n+k*, where *k* is indicated in UL DCI, and *n* is determined based on PDSCH. When UL SCS is larger than DL SCS, two different interpretations existed in the history of RAN1 discussions. The issue was further discussed in RAN1#104b-e [1], and it was concluded that two different interpretations can exist in Rel-15, but it is important to achieve a common understanding for Rel-16.

***Conclusion:***

*For HARQ-ACK timing in Rel-15, in case UL SCS is larger than DL SCS, there are two different interpretations:*

*-       Interpretation 1: k = 0 corresponds to the last UL slot that overlaps with the PDSCH*

*-       Interpretation 2: k = 0 corresponds to the last UL slot that overlaps with the DL slot for the PDSCH*

*Further discuss this issue for Rel-16 in future meetings.*

Assuming an example as shown in Fig. 1 where DL uses 15 kHz SCS and UL uses 30 kHz SCS, with interpretation 1 *k*=0 would correspond to UL slot 6, while with interpretation 2 *k*=0 would correspond to UL slot 7.

Table

Description automatically generated

Figure 1 Example of HARQ-ACK timing

The following point was raised in [2]:

“Purely from HARQ-ACK timing perspective, adopting either interpretation seems to be fine, except that interpretation 2 is aligned with the original agreement.

However, for the pseudo-code for the Type-1 HARQ-ACK codebook construction to work properly, interpretation 2 should be adopted. Basically, the highlighted part below only makes sense if the end of DL slot for PDSCH is used as the reference.”

|  |
| --- |
| **Excerpt from TS 38.213 Clause 9.1.2.1**  Graphical user interface, text, application  Description automatically generated |

Due to the above reason, it was proposed in [2] to adopt interpretation 2 and a corresponding TP was provided.

To better understand the issue for Type 1 HARQ-ACK codebook with interpretation 1, a very simple example is provided in Figure 2.

A screenshot of a computer

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Figure 2 An example of Type-1 HARQ-ACK codebook construction for K1 set = {1}

In this example, it is assumed that the set of K1 values is {1} (i.e. consisting of a single value).

According to interpretation 1,

* for PDSCH1, K1=1 means that the HARQ-ACK should be provided in UL slot 7 (e.g. PUCCH1). For PDSCH2, K1=1 means that the HARQ-ACK should be provided in UL slot 8 (e.g. PUCCH2).
* However, if we follow the pseudo code for Type-1 HARQ-ACK codebook construction, for the HARQ-ACK codebook constructed in UL slot 7, as the highlighted condition is not satisfied (i.e., mod(7-1+1, 2) is not 0), there is not any DL slot that would have HARQ-ACK mapped to UL slot 7.
* On the other hand, for HARQ-ACK codebook constructed in UL slot 8, as the highlighted condition is satisfied, the TDRA entries in DL slot 3 would have HARQ-ACK mapped to UL slot 8, even though PDSCH1 cannot indicate HARQ-ACK in slot 8 with K1=1.

This means that the HARQ-ACK for PDSCH1 is lost in the codebook construction, and the UE would never transmit it to the gNB.

With interpretation 2, such an issue does not exist.

# 3 Email Discussions

## 3.1 First Round of Email Discussion

It is very important for RAN1 to conclude on a single interpretation for the HARQ-ACK timing in Rel-16, in order to support the case when UL SCS is larger than DL SCS. Companies are invited to provide their views on which interpretation should be adopted for Rel-16 and the reasoning behind it (taking into account the issue of Type-1 HARQ-ACK codebook discussed in Section 2).

**Companies please indicate which interpretation you support for Rel-16.**

|  |  |
| --- | --- |
| **Interpretation 1** |  |
| **Interpretation 2** | Qualcomm, OPPO, Nokia, NSB, Huawei, HiSilicon, ZTE, MediaTek, CATT (at least for slot based HARQ-ACK feedback), WILUS, Ericsson, LG, Intel |

**Companies please provide detailed reasons why you support interpretation 1 or 2.**

|  |  |
| --- | --- |
| **Company** | **Comments** |
| Qualcomm | The slot of the PDSCH reception is the reference for k=0, rather than the actual PDSCH symbols due to the reasons we have discussed in the last meeting. At least from Rel-16 spec, we should have a reasonable common interpretation. |
| OPPO | Although we agree in principle with what the draft CR proposed, we are a bit confused by the example given in background section. In this example, because K1={1}, then any nU that is odd number would not meet the condition of mod(nU-K1+1, 2)=0. This failure seems more related to the setup of K1, because if another assumption is made on K1, such as K1={only even number(s)}, any nU that is even number would not meet the condition of mod(nU-K1+1, 2)=0, which means the situation flips between UL slot 7 and UL slot 8. The given example does not seem quite relevant to the justification of either interpretation. |
| Nokia, NSB | Agree with Qualcomm. |
| Huawei, HiSilicon | This issue has been discussed extensively at the last meeting. Even though there are different views for Rel-15, the original intention is clear enough and should be clarified in Rel-16. |
| ZTE | Share the view with Qualcomm. |
| MediaTek | Agree with Qualcomm. |
| CATT | We would like to clarify how to understand interpretation 2 for sub-slot based HARQ-ACK feedback. |
| WILUS | As we discussed in the last RAN1 meeting, interpretation 2 is more aligned to the original intention of the agreements. For the sub-slot based HARQ-ACK feedback, our understanding is that the UL slot is replaced by the UL sub-slot in interpretation 2, i.e, *k = 0 corresponds to the last UL (sub-)slot that overlaps with the DL slot for the PDSCH.* |
| Ericsson | We share the same reasoning as Qualcomm.  With respect to comments from CATT and WILUS, we share the same view and addition by WILUS clarifies the interpretation 2 more precisely.  However, in our view the change is more related on the DL side. The same principle as before for UL is applied in case of slot/sub-slot for UL. |
| LG | We also agree with QC and other companies, and are also fine with the clarification from WILUS. |
| Intel | Support Interpretation 2 for the reasons mentioned above. |

## 3.2 Second Round of Email Discussion

# 4 Outcome of the Email Discussion

# References

1. R1-2104105, Summary of email discussion [104b-e-NR-7.1CRs-04] on the correction for HARQ-ACK timing, Moderator (Apple Inc.), RAN1#104b-e, April 2021.
2. R1-2105075, Correction for HARQ-ACK timing in Rel-15 and Rel-16, Apple, Ericsson, RAN1#105-e, May 2021.