**3GPP TSG RAN WG1 Meeting #103-E R1-200zzzz**

**e-Meeting, October 26th – November 13th, 2020**

**Source: Moderator (Intel Corporation)**

**Title: Summary #5 of RAN WG1 E-mail Discussion [103e-NR-ePos-02] - AI 8.5.2**

**Agenda item: 8.5.2**

**Document for: Discussion and Decision**

# Introduction

In this contribution, we continue discussion on observations captured based on overview of evaluation results provided in contributions submitted for Rel.17 NR Positioning Enhancements WI [1] - [17] and feature lead summary [18] as well as intermediate summary documents [19]-[22] for the RAN WG1 email thread [103e-NR-ePos-02].

We invite companies to provide their views on provided list of observations aiming to converge on evaluation conclusions to be captured in the 3GPP TR on NR Positioning Enhancements.

# Positioning Accuracy Evaluation

## Accuracy Evaluation for Rel.16 NR Positioning Solutions

### Horizontal positioning accuracy in IOO/UMi/UMa

#### Discussion Round #1

1. **(On positioning accuracy in UMa)**
   * **For the case without modeling synchronization and gNB/UE TX/RX timing errors in the UMa scenario**
     + **Based on the results provided by a majority of sources, 10 m level @ 80% of horizontal positioning accuracy is achieved by Rel.16 in UMa scenario**
     + **Results were provided by [2] sources (Ericsson R1-2008764, QC R1-2008618) out of [17] for FR1 band**
       - **For NR positioning evaluations for UMa scenario in FR1 band, the following is observed with respect to horizontal positioning accuracy:**
         1. **Accuracy of ≤** [**10m @ 80%**](mailto:0.2m@90%25) **is achieved in contributions from [2] sources (Ericsson R1-2008764, QC R1-2008618) out of [2] sources**
2. **(On positioning accuracy in UMi)**
   * **For the case without modeling synchronization and gNB/UE TX/RX timing errors in the UMi scenario**
     + **Based on the results provided by a majority of sources, 1 m level @ 80% of horizontal positioning accuracy is achieved by Rel.16 in UMi scenario**
     + **Results were provided by [4] sources (Nokia R1- 2008300, Ericsson R1-2008764, QC R1-2008618, Fraunhofer R1-2009428) out of [17] for FR1 band**
       - **For NR positioning evaluations for UMi scenario in FR1 band, the following is observed with respect to horizontal positioning accuracy:**
         1. **Accuracy of ≤** [**1m @ 80%**](mailto:0.2m@90%25) **is achieved in contributions from [2] sources (Ericsson R1-2008764, QC R1-2008618) and is not achieved from [2] sources (Nokia R1- 2008300, Fraunhofer R1-2009428)**
3. **(On positioning accuracy in IOO)**
   * **For the case without modeling synchronization and gNB/UE TX/RX timing errors in the IOO scenario**
     + **Based on the results provided by a majority of sources, 1 m level @ 80% of horizontal positioning accuracy is achieved by Rel.16 in IOO scenario**
     + **Results were provided by [6] sources (CATT R1-2007859, Nokia R1- 2008300, Sony R1-2008364, Ericsson R1-2008764, QC R1-2008618, vivo R1-2007665) out of [17] for FR1 and [5] sources (CATT R1-2007859, Sony R1-2008364, Ericsson R1-2008764, QC R1-2008618, vivo R1-2007665) out of [17] for FR2 band**
       - **For NR positioning evaluations for IOO scenario in FR1 band, the following is observed with respect to horizontal positioning accuracy:**
         1. **Accuracy of ≤** [**1m @ 80%**](mailto:0.2m@90%25) **is achieved in contributions from [5] sources (CATT R1-2007859, Sony R1-2008364, Ericsson R1-2008764, QC R1-2008618, vivo R1-2007665) and is not achieved from [1] source (Nokia R1- 2008300)**
       - **For NR positioning evaluations for IOO scenario in FR2 band, the following is observed with respect to horizontal positioning accuracy:**
         1. **Accuracy of ≤** [**1m @ 80%**](mailto:0.2m@90%25) **is achieved in contributions from [5] sources (CATT R1-2007859, Sony R1-2008364, Ericsson R1-2008764, QC R1-2008618, vivo R1-2007665)**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| Nokia/NSB | Okay. |
| Qualcomm | Update QC Tdoc to R1-2009361. Shoudnt we clarify that the results above are without the optional absolute timing modelling? |
| ZTE | Okay. |
| vivo | Change ‘1m@80%’ to ‘sub-meter level @ 90%’ for aligning observation.  And for the IOO, the results with absolute time and without absolute time are provided by vivo’s Tdoc. Considering the agreement of the last meeting, maybe need to clarify the scenario for the observation.  Agreement:  For the absolute time of arrival modelling in IOO, UMa, Umi, companies may provide the details of their model, if any |
| LG | Okay |
| Intel | Support. |
| Qualcomm2 | Two comments:   1. For UMI, From QC side, we evaluated both the scenarios of “with Delta tau” and “without Delta tau”. It was also agreed that it is an optional scenario, so we believe it deserves to be captured.    * **For the case without modeling synchronization and gNB/UE TX/RX timing errors in the UMi scenario**      + **Based on the results provided by a majority of sources, 1 m level @ 80% of horizontal positioning accuracy is achieved by Rel.16 in the baseline UMi scenario**      + **Results were provided by [3] sources (Nokia R1- 2008300, Ericsson R1-2008764, QC R1-2008618) out of [17] for FR1 band**        - **For NR positioning evaluations for UMi scenario in FR1 band, the following is observed with respect to horizontal positioning accuracy:**          1. **Accuracy of ≤** [**1m @ 80%**](mailto:0.2m@90%25) **is achieved in contributions from [2] sources (Ericsson R1-2008764, QC R1-2008618) and is not achieved from [1] source (Nokia R1- 2008300) in the scenario without absolute time of arrival modelling**          2. **Accuracy of ≤** [**1m @ 80%**](mailto:0.2m@90%25) **is not achieved from [1] source (QC R1-2008618) in a scenario with absolute time of arrival modelling** 2. For UMA: We think that we need to separate outdoor and indoor UEs as we did in Rel-16, and the 1m target at 80% would still be applicable.    * + - 1. **Accuracy of ≤** [**1~~0~~m @ 80%**](mailto:0.2m@90%25) **is achieved for the outdoor UEs in contributions from [1] source (QC R1-2008618) out of [2] sources**          2. **Accuracy of ≤** [**10m @ 80%**](mailto:0.2m@90%25) **is achieved for the outdoor UEs in contributions from [2] sources (Ericsson R1-2008764, QC R1-2008618) out of [2] sources**          3. **Accuracy of ≤** [**10m @ 80%**](mailto:0.2m@90%25) **is achieved for the indoor UEs in contributions from [1] sources (Ericsson R1-2008764) out of [2] sources** |
| vivo 2 | The same view with QC for another optional case(DH(6.6,2)), we also think it deserves to capture in TR. And draft following observation and hope it can be considered   * + **For the DH case with clutter parameter is {60%, 6m, 2m }**   ○     **Based on the results provided multiple sources, 10m level @ 80% of horizontal positioning accuracy is not achieved in Rel.16 or R17 solution**  ○     **Results were provided by [2] sources (vivo, Futurewei) out of [17] for FR1 band**   * + - * 1. **Accuracy of ≤** [**10m @ 80%**](mailto:0.2m@90%25) **is not achieved in contributions from [2] sources (vivo R1-2007665, Futurewei R1-2007908) out of [2] sources** |
| Fraunhofer | Please note Fraunhofer has an revised Tdoc R1-2009428. This updates the following observation  **Observation 2: (On positioning accuracy in UMi)**   * + **For the case without modeling synchronization and gNB/UE TX/RX timing errors in the UMi scenario**     - **Based on the results provided by a majority of sources, 1 m level @ 80% of horizontal positioning accuracy is achieved by Rel.16 in UMi scenario**     - **Results were provided by [4] sources (Nokia R1- 2008300, Ericsson R1-2008764, QC R1-2008618, Fraunhofer R1-2009428) out of [17] for FR1 band**       * **For NR positioning evaluations for UMi scenario in FR1 band, the following is observed with respect to horizontal positioning accuracy:**         1. **Accuracy of ≤** [**1m @ 80%**](mailto:0.2m@90%25) **is achieved in contributions from [2] sources (Ericsson R1-2008764, QC R1-2008618) and is not achieved from [2] source (Nokia R1- 2008300, Fraunhofer R1-2009428)** |
| CATT | Okay |

#### Discussion Round #2

Based on provided responses, the revised observation for horizontal positioning accuracy are provided below for further comments:

1. **(On positioning accuracy in UMa)**
   * **For the case without modeling synchronization and gNB/UE TX/RX timing errors in the UMa scenario**
     + **Based on the results provided by a majority of sources, 10 m level @ 80% of horizontal positioning accuracy is achieved by Rel.16 in UMa scenario**
     + **Results were provided by [2] sources (Ericsson R1-2008764, QC R1-2008618) out of [17] for FR1 band**
       - **For NR positioning evaluations for UMa scenario in FR1 band, the following is observed with respect to horizontal positioning accuracy:**
         1. **Accuracy of ≤ [1m @ 80%](mailto:0.2m@90%25) is achieved for the outdoor UEs in contributions from [1] source (QC, R1-2008618) out of [2] sources (Ericsson R1-2008764, QC R1-2008618)**
         2. **Accuracy of ≤ [10m @ 80%](mailto:0.2m@90%25) is achieved for the outdoor UEs in contributions from [2] sources (Ericsson R1-2008764, QC R1-2008618) out of [2] sources**
         3. **Accuracy of ≤ [10m @ 80%](mailto:0.2m@90%25) is achieved for the indoor UEs in contributions from [1] source (Ericsson R1-2008764) out of [2] sources**
2. **(On positioning accuracy in UMi)**
   * **For the case without modeling synchronization and gNB/UE TX/RX timing errors in the baseline UMi scenario**
     + **Based on the results provided by a majority of sources, 1 m level @ 80% of horizontal positioning accuracy is achieved by Rel.16 in UMi scenario**
     + **Results were provided by [4] sources (Nokia R1- 2008300, Ericsson R1-2008764, QC R1-2008618, Fraunhofer R1-2009428) out of [17] for FR1 band**
       - **For NR positioning evaluations for UMi scenario in FR1 band, the following is observed with respect to horizontal positioning accuracy:**
         1. **Accuracy of ≤** [**1m @ 80%**](mailto:0.2m@90%25) **is achieved in contributions from [2] sources (Ericsson R1-2008764, QC R1-2008618) and is not achieved from [2] sources (Nokia R1- 2008300, Fraunhofer R1-2009428) in the scenario without absolute time of arrival modelling**
         2. **Accuracy of ≤ [1m @ 80%](mailto:0.2m@90%25) is not achieved from [1] source (QC R1-2008618) in a scenario with absolute time of arrival modelling**
3. **(On positioning accuracy in IOO)**
   * **For the case without modeling synchronization and gNB/UE TX/RX timing errors in the IOO scenario**
     + **Based on the results provided by a majority of sources, 1 m level @ 80% of horizontal positioning accuracy is achieved by Rel.16 in IOO scenario**
     + **Results were provided by [6] sources (CATT R1-2007859, Nokia R1- 2008300, Sony R1-2008364, Ericsson R1-2008764, QC R1-2008618, vivo R1-2007665) out of [17] for FR1 and [5] sources (CATT R1-2007859, Sony R1-2008364, Ericsson R1-2008764, QC R1-2008618, vivo R1-2007665) out of [17] for FR2 band**
       - **For NR positioning evaluations for IOO scenario in FR1 band, the following is observed with respect to horizontal positioning accuracy:**
         1. **Accuracy of ≤** [**1m @ 80%**](mailto:0.2m@90%25) **is achieved in contributions from [5] sources (CATT R1-2007859, Sony R1-2008364, Ericsson R1-2008764, QC R1-2008618, vivo R1-2007665) and is not achieved from [1] source (Nokia R1- 2008300)**
       - **For NR positioning evaluations for IOO scenario in FR2 band, the following is observed with respect to horizontal positioning accuracy:**
         1. **Accuracy of ≤ [1m @ 80%](mailto:0.2m@90%25) is achieved in contributions from [5] sources (CATT R1-2007859, Sony R1-2008364, Ericsson R1-2008764, QC R1-2008618, vivo R1-2007665)**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
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### Impact of synchronization and gNB/UE TX/RX timing errors

#### Discussion Round #1

1. **(On impact of synchronization and gNB/UE TX/RX timing errors)**
   * **Evaluation results (provided by [6] out of [17] sources) have shown that synchronization and gNB/UE TX/RX timing errors have degraded UE positioning accuracy of the Rel.16 NR Positioning timing-based solutions**
   * **If synchronization and gNB/UE TX/RX timing errors are modelled without compensation, the targeted IIoT accuracy requirements with sub-meter level positioning accuracy are not reached by timing-based solutions of the Rel.16 NR Positioning.**
   * **Accurate synchronization and small gNB/UE TX/RX timing errors are essential to achieve precise performance of the NR Positioning timing-based solutions. Further alignment on the X and Y values are needed in the gNB/UE TX/RX timing error model to facilitate the use of common assumptions across different sources**
   * **The values of X and Y beyond certain limit [1.25 ns and 2.5 ns] allow to approach target positioning accuracies, but the feasibility of X and Y values need to be further discussed by RAN WG4**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| **CATT** | * + **For the last bullet, should it be “The values of X and Y within certain limit [1.25 ns and 2.5 ns] allow to approach target positioning accuracies, but the feasibility of X and Y values within the limitation need to be further discussed by RAN WG4** |
| **Huawei/HiSilicon** | **We are not sure how [1.25ns and 2.5ns] is obtained from the evaluation.**  **In addition, whether synchronization error will specified/discussed in RAN4 cannot be decided by RAN1, and we are not sure whether other WGs may be involved, e.g. RAN2 or RAN3, SA groups.**  **Therefore, we suggest the following rewording**  **but the feasibility of X and Y values need to be further discussed** |
| vivo | For the first and second sub-bullet, we think the performance of multi-RTT can meet sub-meter level requirement with synchronization.  Besides, in our evaluation, the sub-meter level requirement can be achieved when timing error small than 2ns, so we wouldn’t say that ” the targeted IIoT accuracy requirements with sub-meter level positioning accuracy are not reached”.   |  |  | | --- | --- | | [Case E72], [SH, perfect sync], [FR1], [DL-TDOA]  [BS timing error 1ns, UE timing error 0.5ns] | 0.42 | | [Case E73], [SH, perfect sync], [FR1], [DL-TDOA]  [BS timing error 2ns, UE timing error 0.5ns] | 0.83 |   So, for the First and second sub-bullet, suggest modifying as below   * + **Evaluation results (provided by [6] out of [17] sources) have shown that ~~synchronization and~~ gNB/UE TX/RX timing errors have degraded UE positioning accuracy of the Rel.16 NR Positioning timing-based solutions**   + **Evaluation results (provided by [6] out of [17] sources) have shown that synchronization ~~and gNB/UE TX/RX timing errors~~ have degraded UE positioning accuracy of the Rel.16 NR Positioning timing-based solutions except for multi-RTT.**   + **~~If synchronization and gNB/UE TX/RX timing errors are modelled without compensation, the targeted IIoT accuracy requirements with sub-meter level positioning accuracy are not reached by timing-based solutions of the Rel.16 NR Positioning.~~**   For the third sub-bullet, suggest modifying as below   * + **Accurate synchronization and small gNB/UE TX/RX timing errors are ~~essential~~ helpful to achieve precise performance of the NR Positioning timing-based solutions. ~~Further alignment on the X and Y values are needed in the gNB/UE TX/RX timing error model to facilitate the use of common assumptions across different sources~~**  |  |  | | --- | --- | | [Case E67], [SH, perfect sync], [FR1], [DL-TDOA]  [BS timing error 0.5ns, UE timing error 0.5ns] | 0.3 | | [Case E76], [DH, perfect sync], [FR1], [DL-TDOA]  [BS timing error 0.5ns, UE timing error 0.5ns] | 0.31 |   For the last sub-bullet, suggest to remove it as target requirement has not been decided. |
| LG | Agree. |
| Intel | Agree with the proposal.  We think that RAN1 can determine X and Y values that do not significantly degrade the positioning performance and check feasibility of determined X and Y values with RAN4.  It will facilitate fair comparison of the evaluation results over different companies.  Given that values are provided in brackets, our understanding that they can be further discussed. |
| Nokia/NSB | There are solutions which do not suffer from synchronization errors, so it is not correct to say they are essential, and it should be highlighted that certain methods are not effected by them. We think the final bullet could be removed as well. |
| Futurewei | Do not agree with the last bullet. It is not RAN1 to set and recommend the values for X and Y. Last bullet should be revised to:   * + **~~The values of X and Y beyond certain limit [1.25 ns and 2.5 ns] allow to approach target positioning accuracies, but~~ the feasibility of X and Y values need to be further discussed by RAN WG4** |
| ZTE | Okay with the proposal in principle. RAN1 can decide X and Y values that will not significantly degrade positioning accuracy according to evaluation results. While other WGs may need to check feasibility of X and Y values. |
| Qualcomm | * + We prefer to remove the last bullet. There is no need to add numbers at this point. |

#### Discussion Round #2

Based on provided responses, the revised observation for gNB/UE Rx/Tx timing errors is provided below for further comments:

1. **(On impact of gNB/UE TX/RX timing errors)**
   * **Evaluation results of gNB/UE TX/RX timing errors are provided by [7] sources (Huawei, ZTE, Qualcomm, Intel, CATT, Ericsson, vivo) out of [17] sources)**
   * **Summary of results is provided in tables below:**

Table 1: Summary of evaluated gNB/UE TX/RX timing error parameters and achieved horizontal positioning accuracy in InF-SH baseline scenario for Rel.16 positioning method.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Company name**  **(Positioning method)** | **FR1 / FR2** | **gNB/UE TX/RX timing error mitigation is on/off** | **Evaluated UE TX/RX timing error values (Y value)** | **Evaluated gNB TX/RX timing error values (X value)** | **Is horizontal positioning accuracy  0.2m @ 90% met?** | **Is horizontal positioning accuracy  0.5m @ 90% met?** |
| Intel  (Multi-RTT) | FR1 | Off at gNB  Off at UE | 10 ns | 5 ns | NO | NO |
| FR1 | Ideal at gNB  On at UE | 0 ns | 5 ns | NO | YES |
| ZTE  (DL-TDOA) | FR1 | Off at gNB | 0 ns | 0.5 ns | NO | NO |
| FR2 | Off at gNB | 0 ns | 0.5 ns | NO | YES |
| Huawei/HiSilicon  (DL/UL-TDOA) | FR1 | Off at gNB | N/A | 1.4ns  (2ns inter-gNB difference) | NO | NO |
| Huawei/HiSilicon  (UL-TDOA/AoA) | FR1 | Off at gNB | N/A | 1.4ns  (2ns inter-gNB difference) | NO | Yes |
| Huawei/HiSilicon  (Multi-RTT) | FR1 | Off at gNB  Off at UE | 5.6ns  (8ns intra-UE Rx - Tx difference) | 1.4ns  (2ns intra-gNB Rx – Tx difference) | NO | NO |
| vivo 1  (DL-TDOA) | FR1 | Off at gNB  Off at UE | 0 ns | 0 ns | Yes (0.094) | Yes (0.094) |
| 0.5ns | 0.5ns | NO (0.30) | Yes (0.30) |
| 1ns | 0.5ns | NO (0.34) | Yes (0.34) |
| 2ns | 0.5ns | NO (0.36) | Yes (0.36) |
| 3ns | 0.5ns | NO (0.35) | Yes (0.35) |
| 5ns | 0.5ns | NO( 0.37) | Yes ( 0.37) |
| 0.5ns | 1ns | NO(0.42) | Yes (0.42) |
| 0.5ns | 2ns | NO (0.83) | NO (0.83) |
| 0.5ns | 3ns | NO (1.07) | NO (1.07) |
| 0.5ns | 5ns | NO (1.87) | NO (1.87) |
| vivo 2  (Multi-RTT) | FR1 | Off at gNB  Off at UE | 0 ns | 0 ns | Yes (0.092) | Yes (0.092) |
| 0.5ns | 0.5ns | NO (0.24） | Yes (0.24） |
| 1ns | 0.5ns | NO (0.23) | Yes (0.23) |
| 2ns | 0.5ns | NO (0.27) | Yes (0.27) |
| 3ns | 0.5ns | NO (0.33) | Yes (0.33) |
| 5ns | 0.5ns | NO (0.44) | Yes (0.44) |
| 0.5ns | 1ns | NO (0.28) | Yes (0.28) |
| 0.5ns | 2ns | NO (0.34) | Yes (0.34) |
| 0.5ns | 3ns | NO (0.76) | NO (0.76) |
| 0.5ns | 5ns | NO (1.26) | NO (1.26) |
| Qualcomm  (DL-TDOA) | FR2 | Off at gNB  Off at UE | 0.0ns | 0.0ns | Yes | Yes |
| 0.1ns | 0.1ns | Yes | Yes |
| 0.2ns | 0.2ns | Yes | Yes |
| 0.5ns | 0.5ns | No | Yes |
| 1.0ns | 1.0ns | No | No |
| 2.0ns | 2.0ns | No | No |
| Ericsson  (DL-TDOA) | FR2 | Off at gNB  Off at UE | N/A | 0ns | YES(0.031218) | YES(0.031218) |
| Off at gNB  Off at UE | N/A | 1ns | NO(0.500084) | YES(0.500084) |
| Off at gNB  Off at UE | N/A | 2ns | NO(0.989034) | NO(0.989034) |
| Off at gNB  Off at UE | N/A | 4ns | NO(1.924776) | NO(1.924776) |
| Off at gNB  Off at UE | N/A | 8ns | NO(3.848105) | NO(3.848105) |
| On at gNB | N/A | 0ns | YES(0.034039) | YES(0.034039) |
| On at gNB | N/A | 8ns | YES(0.02989) | YES(0.02989) |
|  |  |  |  |  |  |  |

Table 2: Summary of evaluated gNB/UE TX/RX timing error parameters and achieved horizontal accuracy in InF-DH baseline scenario for Rel.16 positioning methods.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Company name**  **(Positioning method)** | **FR1 / FR2** | **gNB/UE TX/RX timing error mitigation is on/off** | **Evaluated UE TX/RX timing error values (Y value)** | **Evaluated gNB TX/RX timing error values (X value)** | **Is positioning accuracy  0.2m @ 90% met?** | **Is positioning accuracy  0.5m @ 90% met?** |
| Intel  (Multi-RTT) | FR1 | Off at gNB  Off at UE | 10 ns | 5 ns | NO | NO |
| FR1 | Ideal at gNB  On at UE | 0 ns | 5 ns | NO | NO |
| ZTE  (DL-TDOA) | FR1 | Off at gNB | 0 ns | 0.5 ns | NO | NO |
| FR2 | Off at gNB | 0 ns | 0.5 ns | NO | NO |
| Huawei/HiSilicon  (DL/UL-TDOA) | FR1 | On at gNB | N/A | 1.4ns  (2ns inter-gNB difference) | NO | NO |
| Huawei/HiSilicon  (UL-TDOA/AoA) | FR1 | On at gNB | N/A | 1.4ns  (2ns inter-gNB difference) | NO | NO |
| Huawei/HiSilicon  (Multi-RTT) | FR1 | On at gNB  On at UE | 5.6ns  (8ns intra-UE Rx - Tx difference) | 1.4ns  (2ns intra-gNB Rx – Tx difference) | NO | NO |
| vivo 1  (DL-TDOA) | FR1 | Off at gNB  Off at UE | 0 ns | 0ns | Yes (0.17) | Yes (0.17) |
| 0.5ns | 0.5ns | NO (0.31) | Yes (0.31) |
| 1ns | 0.5ns | NO (0.32) | Yes (0.32) |
| 2ns | 0.5ns | NO (0.32) | Yes (0.32) |
| 3ns | 0.5ns | NO (0.28) | Yes (0.28) |
| 5ns | 0.5ns | NO (0.31) | Yes (0.31) |
| 0.5ns | 1ns | NO(0.40) | Yes (0.40) |
| 0.5ns | 2ns | NO (0.76) | NO (0.76) |
| 0.5ns | 3ns | NO (0.88) | NO (0.88) |
| 0.5ns | 5ns | NO (1.94) | NO (1.94) |
| vivo 2  (Multi-RTT) | FR1 | Off at gNB  Off at UE | 0 ns | 0ns | Yes (0.19) | Yes (0.19) |
| 0.5ns | 0.5ns | NO (0.24） | Yes (0.24） |
| 1ns | 0.5ns | NO (0.24) | Yes (0.23) |
| 2ns | 0.5ns | NO (0.27) | Yes (0.27) |
| 3ns | 0.5ns | NO (0.28) | Yes (0.33) |
| 5ns | 0.5ns | NO (0.46) | Yes (0.44) |
| 0.5ns | 1ns | NO (0.34) | Yes (0.28) |
| 0.5ns | 2ns | NO (0.48) | Yes (0.34) |
| 0.5ns | 3ns | NO (0.87) | NO (0.76) |
| Qualcomm  (DL-TDOA) | FR2 | Off at gNB  Off at UE | 0.0ns | 0.0ns | Yes | Yes |
| 0.1ns | 0.1ns | Yes | Yes |
| 0.2ns | 0.2ns | Yes | Yes |
| 0.5ns | 0.5ns | No | No |
| 1.0ns | 1.0ns | No | No |
| 2.0ns | 2.0ns | No | No |

Table 3: Summary of evaluated gNB/UE TX/RX timing error parameters and achieved horizontal positioning accuracy in IOO scenario for Rel.16 positioning method.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Company name**  **(Positioning method)** | **FR1 / FR2** | **gNB/UE TX/RX timing error mitigation is on/off** | **Evaluated UE TX/RX timing error values (Y value)** | **Evaluated gNB TX/RX timing error values (X value)** | **Is horizontal positioning accuracy  0.2m @ 90% met?** | **Is horizontal positioning accuracy  0.5m @ 90% met?** |
| CATT  (DL-TDOA) | FR1 | Off at gNB  Off at UE | 1.5 ns | 0.5 ns | NO | NO |
| CATT  (UL-TDOA) | FR1 | Off at gNB  Off at UE | 1.5 ns | 0.5 ns | NO | NO |
| CATT  (Multi-RTT) | FR1 | Off at gNB  Off at UE | 1.5 ns | 0.5 ns | NO | NO |
| CATT  (DL-TDOA) | FR2 | Off at gNB  Off at UE | 1.5 ns | 0.5 ns | NO | NO |
| CATT  (UL-TDOA) | FR2 | Off at gNB  Off at UE | 1.5 ns | 0.5 ns | NO | NO |
| CATT  (Multi-RTT) | FR2 | Off at gNB  Off at UE | 1.5 ns | 0.5 ns | NO | NO |

Companies are encouraged to fill out two tables (Table 1 and Table 2) for InF-SH and InF-DH baseline scenarios and one table (Table 3) for IOO scenarios for the positioning method, achieving the best accuracy performance.

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| Huawei/HiSilicon | We assume for TDOA methods, UE error is irrelevant. |
| LG | Agree. To unified format, we think the title of table 2 “Summary of evaluated timing error parameters” need to be changed into “Summary of evaluated gNB/UE TX/RX timing error parameters” like title of table 1. |
| Intel | Support. |
| Nokia/NSB | Okay |
| CATT | We simulated the impact of gNB/UE TX/RX timing error on horizontal positioning accuracy in IOO, which cannot be include Table 1 and 2. So, we added Table 3. |
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* + - 1. Discussion Round #3

Based on provided responses, the revised observation for gNB/UE Rx/Tx timing errors is provided below for further comments:

1. **(On impact of gNB/UE TX/RX timing errors)**
   * **Evaluation results of gNB/UE TX/RX timing errors are provided by [7] sources (Huawei, ZTE, Qualcomm, Intel, CATT, Ericsson, vivo) out of [17] sources)**
   * **Summary of results is provided in tables below:**

Table 1: Summary of evaluated gNB/UE TX/RX timing error parameters and achieved horizontal positioning accuracy in InF-SH baseline scenario for Rel.16 positioning method.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Company name**  **(Positioning method)** | **FR1 / FR2** | **gNB/UE TX/RX timing error mitigation is on/off** | **Evaluated UE TX/RX timing error values (Y value)** | **Evaluated gNB TX/RX timing error values (X value)** | **Is horizontal positioning accuracy  0.2m @ 90% met?** | **Is horizontal positioning accuracy  0.5m @ 90% met?** |
| Intel  (Multi-RTT) | FR1 | Off at gNB  Off at UE | 10 ns | 5 ns | NO | NO |
| FR1 | Ideal at gNB  On at UE | 0 ns | 5 ns | NO | YES |
| ZTE  (DL-TDOA) | FR1 | Off at gNB | 0 ns | 0.5 ns | NO | NO |
| FR2 | Off at gNB | 0 ns | 0.5 ns | NO | YES |
| Huawei/HiSilicon  (DL/UL-TDOA) | FR1 | Off at gNB | N/A | 1.4ns  (2ns inter-gNB difference) | NO | NO |
| Huawei/HiSilicon  (UL-TDOA/AoA) | FR1 | Off at gNB | N/A | 1.4ns  (2ns inter-gNB difference) | NO | YES |
| Huawei/HiSilicon  (Multi-RTT) | FR1 | Off at gNB  Off at UE | 5.6ns  (8ns intra-UE Rx - Tx difference) | 1.4ns  (2ns intra-gNB Rx – Tx difference) | NO | NO |
| vivo 1  (DL-TDOA) | FR1 | Off at gNB  Off at UE | 0 ns | 0 ns | YES (0.094) | YES (0.094) |
| 0.5ns | 0.5ns | NO (0.30) | YES (0.30) |
| 1ns | 0.5ns | NO (0.34) | YES (0.34) |
| 2ns | 0.5ns | NO (0.36) | YES (0.36) |
| 3ns | 0.5ns | NO (0.35) | YES (0.35) |
| 5ns | 0.5ns | NO (0.37) | YES (0.37) |
| 0.5ns | 1ns | NO(0.42) | YES (0.42) |
| 0.5ns | 2ns | NO (0.83) | NO (0.83) |
| 0.5ns | 3ns | NO (1.07) | NO (1.07) |
| 0.5ns | 5ns | NO (1.87) | NO (1.87) |
| vivo 2  (Multi-RTT) | FR1 | Off at gNB  Off at UE | 0 ns | 0 ns | YES (0.092) | YES (0.092) |
| 0.5ns | 0.5ns | NO (0.24） | YES (0.24） |
| 1ns | 0.5ns | NO (0.23) | YES (0.23) |
| 2ns | 0.5ns | NO (0.27) | YES (0.27) |
| 3ns | 0.5ns | NO (0.33) | YES (0.33) |
| 5ns | 0.5ns | NO (0.44) | YES (0.44) |
| 0.5ns | 1ns | NO (0.28) | YES (0.28) |
| 0.5ns | 2ns | NO (0.34) | YES (0.34) |
| 0.5ns | 3ns | NO (0.76) | NO (0.76) |
| 0.5ns | 5ns | NO (1.26) | NO (1.26) |
| Qualcomm  (DL-TDOA) | FR2 | Off at gNB  Off at UE | 0.0ns | 0.0ns | YES | YES |
| 0.1ns | 0.1ns | YES | YES |
| 0.2ns | 0.2ns | YES | YES |
| 0.5ns | 0.5ns | NO | YES |
| 1.0ns | 1.0ns | NO | NO |
| 2.0ns | 2.0ns | NO | NO |
| Ericsson  (DL-TDOA) | FR2 | Off at gNB  Off at UE | N/A | 0ns | YES(0.031218) | YES(0.031218) |
| Off at gNB  Off at UE | N/A | 1ns | NO(0.500084) | YES(0.500084) |
| Off at gNB  Off at UE | N/A | 2ns | NO(0.989034) | NO(0.989034) |
| Off at gNB  Off at UE | N/A | 4ns | NO(1.924776) | NO(1.924776) |
| Off at gNB  Off at UE | N/A | 8ns | NO(3.848105) | NO(3.848105) |
| On at gNB | N/A | 0ns | YES(0.034039) | YES(0.034039) |
| On at gNB | N/A | 8ns | YES(0.02989) | YES(0.02989) |
|  |  |  |  |  |  |  |

Table 2: Summary of evaluated gNB/UE TX/RX timing error parameters and achieved horizontal accuracy in InF-DH baseline scenario for Rel.16 positioning methods.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Company name**  **(Positioning method)** | **FR1 / FR2** | **gNB/UE TX/RX timing error mitigation is on/off** | **Evaluated UE TX/RX timing error values (Y value)** | **Evaluated gNB TX/RX timing error values (X value)** | **Is positioning accuracy  0.2m @ 90% met?** | **Is positioning accuracy  0.5m @ 90% met?** |
| Intel  (Multi-RTT) | FR1 | Off at gNB  Off at UE | 10 ns | 5 ns | NO | NO |
| FR1 | Ideal at gNB  On at UE | 0 ns | 5 ns | NO | NO |
| ZTE  (DL-TDOA) | FR1 | Off at gNB | 0 ns | 0.5 ns | NO | NO |
| FR2 | Off at gNB | 0 ns | 0.5 ns | NO | NO |
| Huawei/HiSilicon  (DL/UL-TDOA) | FR1 | On at gNB | N/A | 1.4ns  (2ns inter-gNB difference) | NO | NO |
| Huawei/HiSilicon  (UL-TDOA/AoA) | FR1 | On at gNB | N/A | 1.4ns  (2ns inter-gNB difference) | NO | NO |
| Huawei/HiSilicon  (Multi-RTT) | FR1 | On at gNB  On at UE | 5.6ns  (8ns intra-UE Rx - Tx difference) | 1.4ns  (2ns intra-gNB Rx – Tx difference) | NO | NO |
| vivo 1  (DL-TDOA) | FR1 | Off at gNB  Off at UE | 0 ns | 0ns | YES (0.17) | YES (0.17) |
| 0.5ns | 0.5ns | NO (0.31) | YES (0.31) |
| 1ns | 0.5ns | NO (0.32) | YES (0.32) |
| 2ns | 0.5ns | NO (0.32) | YES (0.32) |
| 3ns | 0.5ns | NO (0.28) | YES (0.28) |
| 5ns | 0.5ns | NO (0.31) | YES (0.31) |
| 0.5ns | 1ns | NO(0.40) | YES (0.40) |
| 0.5ns | 2ns | NO (0.76) | NO (0.76) |
| 0.5ns | 3ns | NO (0.88) | NO (0.88) |
| 0.5ns | 5ns | NO (1.94) | NO (1.94) |
| vivo 2  (Multi-RTT) | FR1 | Off at gNB  Off at UE | 0 ns | 0ns | YES (0.19) | YES (0.19) |
| 0.5ns | 0.5ns | NO (0.24） | YES (0.24） |
| 1ns | 0.5ns | NO (0.24) | YES (0.23) |
| 2ns | 0.5ns | NO (0.27) | YES (0.27) |
| 3ns | 0.5ns | NO (0.28) | YES (0.33) |
| 5ns | 0.5ns | NO (0.46) | YES (0.44) |
| 0.5ns | 1ns | NO (0.34) | YES (0.28) |
| 0.5ns | 2ns | NO (0.48) | YES (0.34) |
| 0.5ns | 3ns | NO (0.87) | NO (0.76) |
| Qualcomm  (DL-TDOA) | FR2 | Off at gNB  Off at UE | 0.0ns | 0.0ns | YES | YES |
| 0.1ns | 0.1ns | YES | YES |
| 0.2ns | 0.2ns | YES | YES |
| 0.5ns | 0.5ns | No | No |
| 1.0ns | 1.0ns | No | No |
| 2.0ns | 2.0ns | No | No |

Table 3: Summary of evaluated gNB/UE TX/RX timing error parameters and achieved horizontal positioning accuracy in IOO scenario for Rel.16 positioning method.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Company name**  **(Positioning method)** | **FR1 / FR2** | **gNB/UE TX/RX timing error mitigation is on/off** | **Evaluated UE TX/RX timing error values (Y value)** | **Evaluated gNB TX/RX timing error values (X value)** | **Is horizontal positioning accuracy  0.2m @ 90% met?** | **Is horizontal positioning accuracy  0.5m @ 90% met?** |
| CATT  (DL-TDOA) | FR1 | Off at gNB  Off at UE | 1.5 ns | 0.5 ns | NO | NO |
| CATT  (UL-TDOA) | FR1 | Off at gNB  Off at UE | 1.5 ns | 0.5 ns | NO | NO |
| CATT  (Multi-RTT) | FR1 | Off at gNB  Off at UE | 1.5 ns | 0.5 ns | NO | NO |
| CATT  (DL-TDOA) | FR2 | Off at gNB  Off at UE | 1.5 ns | 0.5 ns | NO | NO |
| CATT  (UL-TDOA) | FR2 | Off at gNB  Off at UE | 1.5 ns | 0.5 ns | NO | NO |
| CATT  (Multi-RTT) | FR2 | Off at gNB  Off at UE | 1.5 ns | 0.5 ns | NO | NO |

Table 4: Summary of evaluated gNB/UE TX/RX timing error parameters and achieved horizontal positioning accuracy in UMi scenario for Rel.16 positioning method.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Company name**  **(Positioning method)** | **FR1 / FR2** | **gNB/UE TX/RX timing error mitigation is on/off** | **Evaluated UE TX/RX timing error values (Y value)** | **Evaluated gNB TX/RX timing error values (X value)** | **Is horizontal positioning accuracy  0.2m @ 90% met?** | **Is horizontal positioning accuracy  0.5m @ 90% met?** |
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Companies are encouraged to fill out two tables (Table 1 and Table 2) for InF-SH and InF-DH baseline scenarios and two tables (Table 3 and Table 4) for IOO scenarios and UMi scenarios for the positioning method, achieving the best accuracy performance.

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| **Company Name** | **Comments** |
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## Accuracy Evaluation for NR Positioning Enhancements

### LOS / NLOS Identification and NLOS Mitigation

#### Discussion Round #1

1. **(On LOS/NLOS identification and NLOS mitigation)**
   * **Evaluation results for LOS/NLOS identification and NLOS mitigation in indoor factory scenario were provided by [9] sources out of [17]:**
     + **The [6] sources show that LOS/NLOS identification provides performance gain and reporting of the LOS/NLOS link type need to be considered as NR positioning enhancement relative to Rel.16 solutions.**
     + **The [2] sources compared NR positioning performance of LOS/NLOS detection algorithm(s) and have shown that it has better performance compared to the outlier rejection algorithms.**
     + **The [1] source shows that implementing NLOS mitigation can improve positioning accuracy. In InF-SH scenario, gain from the method of LOS classification is marginal.**
     + **The [2] sources show that the outlier rejection algorithm has better performance than LOS/NLOS detection algorithm.**
   * **LOS/NLOS identification and NLOS mitigation are recommended as a solution to overcome the problem of NLOS excess propagation delay offset for indoor factory scenarios especially in the NLOS-heavy scenarios like InF-DH.**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| **CATT** | **Since the last bullet is an observation, but not a proposal, suggest rewording it to: “LOS/NLOS identification and NLOS mitigation are observed to be a viable solution to…”** |
| Qualcomm | Based on the above evaluations, it is not clear that “LOS/NLOS identification and NLOS mitigation” is recommended. Outlier rejections are implementation-based algorithms that already can be used in NR Rel-16 for “LOS/NLOS identification and mitigation”. There are 4 companies that compare both schemes, and it looks like a tie currently based on the results.  As suggested in previous comments, we suggest to keep just the bullets that summarize the results without drawing further conclusions. |
| **vivo** | **Suggest modifying as below:**   * + **Evaluation results for LOS/NLOS identification and NLOS mitigation in indoor factory scenario were provided by [9] sources out of [17]:**     - **The [6] sources show that LOS/NLOS identification provides performance gain ~~and reporting of the LOS/NLOS link type need to be considered as NR positioning enhancement relative to Rel.16 solutions.~~**     - **The [X] sources show that the outlier rejection algorithm provides performance gain.**     - **The [2] sources compared NR positioning performance of LOS/NLOS detection algorithm(s) and have shown that it has better performance compared to the outlier rejection algorithms.**     - **The [1] source shows that implementing NLOS mitigation can improve positioning accuracy. In InF-SH scenario, gain from the method of LOS classification is marginal.**     - **The [2] sources show that the outlier rejection algorithm has better performance than LOS/NLOS detection algorithm.**     - **The [vivo] source show that the positioning performance of LOS/NLOS detection method degrades as LOS detection error probability increases.**   + **~~LOS/NLOS identification and NLOS mitigation are recommended as a solution to overcome the problem of NLOS excess propagation delay offset for indoor factory scenarios especially in the NLOS-heavy scenarios like InF-DH.~~** |
| LG | Ok with first bullet. But for second bullet, we agree with QC’s comment. |
| Intel | Support in general.  Suggest rephrasing the last bullet as follows:   * + **LOS/NLOS identification is beneficial ~~and NLOS mitigation are recommended as a solution~~ to overcome the problem of NLOS excess propagation delay offset for indoor factory scenarios especially in the NLOS-heavy scenarios like InF-DH.** |
| Apple | Share a similar view with LG and QC |
| Nokia/NSB | Okay with the first bullet. |
| Futurewei | Support Intel’s revised wordings |
| OPPO | Firstly, we suggest update the 3rd sub-bullet in the observation as follows. The NLOS mitigation method out tdoc is UE implementation-based method. The change tries to clarify that.   * + - **The [1] source shows that UE implementation-based NLOS mitigation can improve positioning accuracy. In InF-SH scenario, gain from the method of LOS classification is marginal.**   Secondly, we share the same view as Qualcomm and vivo that the 2nd bullet (conclusion) shall be deleted here. It is good to only make the observation here. |
| ZTE | Agree with changes from Intel. Suggest to revise the first sub-bullet in first bullet as follow,   * + - **The [6] sources show that LOS/NLOS identification provides performance gain and reporting of assistance information for the LOS/NLOS detection need to be considered as NR positioning enhancement relative to Rel.16 solutions.** |

#### Discussion Round #2

Based on provided responses, the revised observation for LOS/NLOS identification and NLOS mitigation is provided below for further comments.

1. **(On LOS/NLOS identification and NLOS mitigation)**
   * **Evaluation results for LOS/NLOS identification outlier rejection, NLOS mitigation based on triangle inequality algorithms in indoor factory scenarios were provided by [11] sources (OPPO, Futurewei, vivo, Intel, Qualcomm, ZTE, Huawei, CeWiT, Nokia, Sony, Fraunhofer) out of [17] sources**
   * **NR positioning utilizing LOS/NLOS identification, outlier rejection, NLOS mitigation based on triangle inequality algorithms improve performance of positioning accuracy with respect to solutions that do not apply these techniques**
   * **Based on results of evaluation**
     + **[9] sources (Futurewei, Intel, ZTE, Huawei, CeWiT, Nokia, Sony, Fraunhofer, Ericsson) evaluated LOS/NLOS identification with additional specification changes relative to Rel.16 solutions**
     + **[1] source (Ericsson) evaluated NLOS detection using reporting enhancements**
     + **[2] sources (vivo, Qualcomm) evaluatedoutlier rejection algorithm (implementation-based algorithm that can be applied for Rel.16 solutions without specification changes)**
     + **[1] source (OPPO) evaluated NLOS mitigation using triangle-based inequality algorithm (implementation-based algorithm that can be applied for Rel.16 solutions without specification changes)**
   * **Comparative analysis of LOS/NLOS identification vs outlier rejection algorithms was done by 5 sources (Intel, Huawei, vivo, Qualcomm, ZTE)**
     + **Three sources (Intel, Huawei, ZTE) observe that NR positioning based on LOS/NLOS identification outperforms NR positioning utilizing outlier rejection**
     + **Two sources (vivo, Qualcomm) observe that NR positioning utilizing outlier rejection outperforms NR positioning utilizing LOS/NLOS identification**
   * **Comparative analysis of NLOS mitigation based on triangle-based inequality vs LOS/NLOS identification was done by 1 source (OPPO). The following was observed:**
     + **Implementing LOS classification method can improve the positioning accuracy, but the errors in LOS classification may decrease performance**
     + **In InF-SH scenario, gain from the method of LOS classification is marginal**

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| **ZTE** | **We actually compare the performance of implementation-based algorithm (similar to RAIM algorithm, shown in case 12 and 17 in our contribution) and NLOS mitigation methods, where NLOS mitigation methods are superior to implementation-based algorithm. So we would like to update the third bullet,**   * + **Comparative analysis of LOS/NLOS identification vs NLOS mitigation based on outlier rejection algorithms was done by 5 sources (Intel, Huawei, vivo, Qualcomm, ZTE)**     - **Three sources (Intel, Huawei, ZTE) observe that NR positioning based on LOS/NLOS identification outperforms NR positioning utilizing NLOS mitigation based on outlier rejection**     - **Two sources (vivo, Qualcomm) observe that NR positioning utilizing NLOS mitigation based on outlier rejection outperforms NR positioning utilizing LOS/NLOS identification** |
| **vivo** | **Thanks FL for the summary of observations.**  **Regarding the 3rd bullet, we feel the discussion of support LOS/NLOS identification or not would be better fit into the scope of 8.5.3, especially when talking “with additional specification changes relative to Rel.16” which are not revealed at all by the evaluation results.**  **Regarding the last bullet, our understanding of OPPO’s comparison is also UE implementation-based algorithm vs. LOS/NLOS identification. But I’ll leave this to OPPO.** |
| **LG** | **Agree.** |
| Intel | Support. |
| Fraunhofer | Ok in principle, please add Fraunhofer to the sources in:   * + **Evaluation results for LOS/NLOS identification and NLOS mitigation based on outlier rejection or triangle inequality algorithms in indoor factory scenarios were provided by [11] sources (OPPO, Futurewei, vivo, Intel, Qualcomm, ZTE, Huawei, CeWiT, Nokia, Sony, Fraunhofer) out of [17] sources**   + **..**   + **Based on results of evaluation**     - **[8] sources (Futurewei, Intel, ZTE, Huawei, CeWiT, Nokia, Sony, Fraunhofer) support LOS/NLOS identification with additional specification changes relative to Rel.16** |
| Futurewei | Support |
| Nokia/NSB | Support |
| CATT | Support |
| Qualcomm | Thanks for the updated proposal   * With regards to the 1st bullet:   + Outlier rejection is not just doing “LOS/NLOS” identification and “NLOS mitigation”. Outlier rejection is about finding outliers; these can even be LOS links that have low SNR, or for some reason resulted in bad TOA estimation; and vice versa: NLOS links that happen to have good TOA estimation; or even a group of NLOS links, which, even though, each one separately has “relatively bad” TOA estimation, the errors in the positioning domain are averaged out, and the resulting collection of links turns out produce a good positioning estimate. Shouldn’t the first bullet be as follows:   **Evaluation results with LOS/NLOS identification, NLOS mitigation, outlier rejection, or triangle inequality …**   * Similar comment to the 2nd bullet:   **NR positioning utilizing LOS/NLOS identification, NLOS mitigation, outlier rejection, or triangle inequality algorithms improves performance of positioning accuracy with respect to solutions that do not apply these techniques**  Then, add the remaining bullets as subbullets of this statement   * With regards to the 3rd bullet:   + The bullet with the “support” or “not support” is also part of 8.5.3 discussion. It is not needed here.   + If the intention is to say that for these 7 companies, LOS/NLOS identification provided better performance, we need to say that it provided better performance over a scenario that is not using “outlier rejection”. Since, in the 4th bullet we say which companies do the comparison of LOS/NLOS vs Outlier rejection. |
| Ericsson | We ran evaluations for Inf DH in LOS detection. Below is the edited observation including our evaluation.   1. **(On LOS/NLOS identification and NLOS mitigation)**    * **Evaluation results for LOS/NLOS identification outlier rejection, NLOS mitigation based on triangle inequality algorithms in indoor factory scenarios were provided by [11] sources (OPPO, Futurewei, vivo, Intel, Qualcomm, ZTE, Huawei, CeWiT, Nokia, Sony, Fraunhofer) out of [17] sources**    * **NR positioning utilizing LOS/NLOS identification, outlier rejection, NLOS mitigation based on triangle inequality algorithms improve performance of positioning accuracy with respect to solutions that do not apply these techniques**    * **Based on results of evaluation**      + **[9] sources (Futurewei, Intel, ZTE, Huawei, CeWiT, Nokia, Sony, Fraunhofer, Ericsson) evaluated LOS/NLOS identification with additional specification changes relative to Rel.16**      + **[2] sources (vivo, Qualcomm) evaluatedoutlier rejection algorithm (implementation-based algorithm that can be applied for Rel.16 solutions without specification changes)**      + **[1] source (OPPO) evaluated NLOS mitigation usinge triangle-based inequality algorithm (implementation-based algorithm that can be applied for Rel.16 solutions without specification changes)**      + **[1] source (Ericsson) evaluated NLOS detection using reporting enhancements**    * **Comparative analysis of LOS/NLOS identification vs outlier rejection algorithms was done by 5 sources (Intel, Huawei, vivo, Qualcomm, ZTE)**      + **Three sources (Intel, Huawei, ZTE) observe that NR positioning based on LOS/NLOS identification outperforms NR positioning utilizing outlier rejection**      + **Two sources (vivo, Qualcomm) observe that NR positioning utilizing outlier rejection outperforms NR positioning utilizing LOS/NLOS identification**    * **Comparative analysis of NLOS mitigation based on triangle-based inequality vs LOS/NLOS identification was done by 1 source (OPPO). The following was observed:**      + **Implementing LOS classification method can improve the positioning accuracy, but the errors in LOS classification may decrease performance**      + **In InF-SH scenario, gain from the method of LOS classification is marginal** |

### Aggregation of Positioning Frequency Layers

#### Discussion Round #1

1. **(On aggregation of NR positioning frequency layers)**
   * **Evaluation results for aggregation of positioning frequency layers were provided by [4] sources out of [17].**
   * **Aggregation of NR positioning frequency layers improves positioning accuracy and achieve the target IIoT positioning accuracy.**
   * **Further work is needed to decide on details of supported configurations for NR positioning frequency layer aggregation, including practical impairments such as: channel spacing, timing offset over frequency layers, frequency offset over frequency layers, phase discontinuity and possible amplitude imbalance.**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| **CATT** | **For 2nd bullet, we may say “Aggregation of NR positioning frequency layers improves positioning accuracy and achieve the target IIoT positioning accuracy, under certain scenarios…** |
| Qualcomm | Similar comment to previous observations. Suggest to summarize what the companies that provided results have demonstrated. E.g., gains are shown under specific scenarios/impairments/configurations. An example of wording:   * + Evaluation results for aggregation of positioning frequency layers were provided by [4] sources out of [17]:     - Aggregation of NR positioning frequency layers improves positioning accuracy and achieve the target IIoT positioning accuracy, under certain scenarios, configurations, and impairments such as: channel spacing, timing offset over frequency layers, frequency offset over frequency layers, phase discontinuity and possible amplitude imbalance. |
| **vivo** | Agree with CATT and QC.  Beside, based on our evaluation results in case E18, the accuracy is 0.23, can't meet [0.2m@90%](mailto:0.2m@90%25), it is too early to say “Aggregation of NR positioning frequency layers achieve the target IIoT positioning accuracy.” And if the bandwidth of two FL is smaller than 50M， it is impossible to meet the requirement too.   |  |  |  |  | | --- | --- | --- | --- | | Simulation case  (Horizontal Error) | Gain vs Rel.16 solution, @[90]%, [m] | Accuracy achieved @[90]% | IIoT horizontal accuracy requirements of [0.2]m @[90]%are met - Yes/No. If no, provide performance gaps | | [Case E103], [SH, perfect sync], [FR1], [50M] |  | 0.31 | 0.11 | | [Case E104], [SH, perfect sync], [FR1], [100M] |  | 0.094 | Yes | | [Case E105], [SH, perfect sync], [FR1], [50M+50M] |  | 0.21 | 0.01 | | [Case E106], [DH, perfect sync], [FR1], [50M] |  | 0.44 | 0.24 | | [Case E107], [DH, perfect sync], [FR1], [100M] |  | 0.17 | Yes | | Case E108], [DH, perfect sync], [FR1], [50M+50M] |  | 0.23 | 0.03 |   So, we prefer the wording as following   * + Evaluation results for aggregation of positioning frequency layers were provided by [4] sources out of [17]:     - Aggregation of NR positioning frequency layers improves positioning accuracy ~~and achieve the target IIoT positioning accuracy~~, under certain scenarios, configurations, and impairments such as: channel spacing, timing offset over frequency layers, frequency offset over frequency layers, phase discontinuity and possible amplitude imbalance.     - FFS whether the performance of aggregation of multiple FLs is better than one FL with the same bandwidth of aggregating |
| LG | We agree with both CATT and QC’s views. |
| Intel | We are OK with the original proposal and additional revised wording from CATT. |
| Nokia/NSB | Suggest to follow the prior observation structure and just describe which sources show improvement for this topic rather than the generic statement in 2nd bullet. |
| OPPO | Regarding the 2nd bullet, suggest to make the following change:   * + **Aggregation of NR positioning frequency layers improves positioning accuracy and achieve the target IIoT positioning accuracy with assumption of time offset <= [x] ns.**   The reason for the suggested change is the time offset in CA could be very large. Even for the intra-band contiguous CA case, the time offset could be 260ns as shown in RAN4 spec. But in the submitted evaluation results, only one source provides the results with time offset value and the time offset value used is some small value as <20ns for InF. All the other sources seem to assume there is time offset. We shall clarify that in the observation to avoid misunderstanding that any time offset value can achieve the IIOT performance requirement.   |  | | --- | | TS 38.104  6.5.3.2 Minimum requirement for *BS type 1-C* and *BS type* 1-H  For MIMO transmission, at each carrier frequency, TAE shall not exceed 65 ns.  For intra-band contiguous *carrier aggregation*, with or without MIMO, TAE shall not exceed 260ns.  For intra-band non-contiguous *carrier aggregation*, with or without MIMO, TAE shall not exceed 3µs.  For inter-band *carrier aggregation*, with or without MIMO, TAE shall not exceed 3µs. |   Furthermore, same comments as Nokia, suggest to only summarize the observation and do not make recommendation. |
| ZTE | Agree with Qualcomm. |
| vivo2 | The update views as below   * + Evaluation results for aggregation of positioning frequency layers were provided by [4] sources out of [17]:     - Aggregation of NR positioning frequency layers improves positioning accuracy ~~and achieve the target IIoT positioning accuracy~~, under certain scenarios, configurations, and impairments such as: channel spacing, timing offset over frequency layers, frequency offset over frequency layers, phase discontinuity and possible amplitude imbalance.     - The performance of Aggregation of NR positioning frequency layers will be worse due to the impact of channel spacing, timing offset, phase offset among CCs for intra-band contiguous/ non-contiguous from [3] sources (Ericsson,vivo, Qualcomm) out of [3] sources |
| Futurewei | Don’t understand the intention of the third bullet e.g. “Further work..”?  Propose to revise to the following:   * + **Further studies/discussions ~~work is needed to decide~~ needed on ~~details of supported~~ the configurations for NR positioning frequency layer aggregation, including practical impairments such as: channel spacing, timing offset over frequency layers, frequency offset over frequency layers, phase discontinuity and possible amplitude imbalance.** |

#### Discussion Round #2

Based on provided responses, the revised observation for aggregation of NR positioning frequency layers is provided below for further comments.

1. **(On aggregation of NR positioning frequency layers)**
   * **Evaluation results for aggregation of positioning frequency layers were provided by [5] sources (Intel, Qualcomm, Huawei, vivo, Ericsson) out of [17].**
   * **Aggregation of NR positioning frequency layers improves positioning accuracy under certain scenarios, configurations, and assumptions on modelled impairments such as: bandwidth and spacing of aggregated layers, timing offset and frequency offset over frequency layers, phase discontinuity and possible amplitude imbalance.**
     + **One source (Huawei) observes that aggregation with phase continuity can help to improve the positioning accuracy, and discontinuous aggregation can approach the performance of contiguous aggregation with the same frequency span**
     + **One source (Intel) has shown that ideal aggregation of frequency layers improves the positioning accuracy for intra-band contiguous configuration and that further study is needed for other cases including impairments**
     + **One source (Ericsson) has observed that ideal PRS aggregation shows potential gains, but these gains are lost when the phase error between CCs becomes too large**
     + **One source (Qualcomm) has analyzed aggregation of 2 and 4 frequency layers for different channel spacings, time and phase offset across frequency layers**
     + **One source (vivo R1-2007666) has analyzed aggregation of 2 frequency layers for different time offset values**
     + **One source (vivo) has observed that:**
       - **For ideal aggregation of multiple DL positioning frequency 50MHz+50MHz, performance target [0.2m @ 90%] cannot be achieved in both InF-SH and InF-DH.**
       - **For ideal aggregation of multiple DL positioning frequency 50MHz+50MHz, the performance is worse than 100MHz but better than 50MHz.**
       - **The performance of aggregation of frequency layers degrades if timing offset is increased**

|  |  |  |  |
| --- | --- | --- | --- |
| **Company Name** | | **Comments** | |
| **ZTE** | | **Okay.** | |
| Huawei/HiSilicon | | OK. | |
| **vivo** | | **The impact of timing offset for CA also be simulated and presented in （vivo R1-2007666）. At least, we hope this evaluation can be captured in observation like this:**   * + - **One source (Qualcomm) has analyzed aggregation of 2 and 4 frequency layers for different channel spacings, time and phase offset across frequenc ~~y~~layers, one source (vivo R1-2007666) has analyzed aggregation of 2 frequency layers for different time offset.**   **In addition, we suggest revealing the impact of “channel spacings, time and phase offset”, ’has analyzed’ did not reveal any of our evaluations.**  **vivo 2**  **Please add the following description ：**   * + - **One source (vivo) has observed that:**       * **For ideal aggregation of multiple DL positioning frequency 50MHz+50MHz, performance target [0.2m @ 90%] cannot be achieved in both InF-SH and InF-DH.**       * **For ideal aggregation of multiple DL positioning frequency 50MHz+50MHz, the performance is worse than 100MHz but better than 50MHz.**       * **The performance of aggregating will degrade with timing offset increasing** | |
| LG | | We are generally fine, but we slightly prefer to remove “and that further study is needed for other cases including impairements” in the second sub-bullet of the second main bullet since it seems not an observation. In addition, there are some typos such as “frequenc ylayers”. | |
| Intel | | Support. | |
| Nokia/NSB | | Okay in principle, we suggest in the second bullet to change ‘and impairments’ to ‘and assumptions on modelled impairments’ | |
| CATT | | Okay in principle. | |
| Qualcomm | | OK | |
| Ericsson | | We have also provided results for PRS aggregation. In our study, we agree with intel that ideal case improves performance, but we also show that even for contiguous aggregation impairements degrades the performance to worse than with 1CC. below is a summary of the performance:   |  |  | | --- | --- | |  | 90% | | Inf DH, FR1, DL TDOA  2xCC, max phase error=pi | 15.00989 | | Inf DH, FR1, DL TDOA  2xCC, no phase error | 13.91966 | | Inf DH, FR1, DL TDOA  1xCC | 15.01508 | | | Inf SH, FR1, DL TDOA  1xCC | 0.259396 | | Inf SH, FR1, DL TDOA  2xCC, no phase error | 0.079559 | | Ericsson E62, Inf SH, FR1, DL TDOA  2xCC, max phase error=0.2\*pi | 0.275798 | | Ericsson E63, Inf SH, FR1, DL TDOA  2xCC, max phase error=pi | 1.447441 |   Below is our proposed revised observation:   * + **Evaluation results for aggregation of positioning frequency layers were provided by [~~45~~] sources (Intel, Qualcomm, Huawei, vivo, Ericsson) out of [17].**   + **<unchanged text deleted>**     - **One source (Ericsson) has observed that ideal PRS aggregation shows potential gains, but these gains are lost when the phase error between CCs becomes too large.** | |
|  | |  | |
|  | |  | |

### On Network Synchronization / gNB/UE TX/RX Timing Errors (Closed)

#### Discussion Round #1

1. **(On Network Synchronization / gNB / UE TX/RX Timing Errors)**
   * **Accurate network synchronization as well as solutions to cope with gNB/UE TX/RX timing errors are needed to achieve precise positioning**
     + **FFS impact on specification**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| **CATT** | **The sub-bullet of “FFS” can be removed here, unless we want to discuss the impact on the specification in the AI.** |
| Qualcomm | Is this Observation really needed in light of the Observation in Section 2.1.4? There will be overlap with the Summary from CATT on Enhancements if we start discussing enhancements here also. |
| **Vivo** | **Agree with QC** |
| LG | We think if we remain FFS in this AI, it may be collide with discussion in the 8.5.3 AI. So, it seems apposite to keep first main bullet only. |
| Intel | Support the proposal.  We are OK to remove the FFS bullet. |
| Nokia/NSB | We don’t agree with this observation. Multi-RTT does not suffer from synchronization errors (or angle based techniques). |
| ZTE | Remove FFS |
| Intel | After revisions made in section 2.1.2.2, it seems this section is redundant. |

#### Discussion Round #2 (Closed)

Based on received responses in discussion round #1 on overlap with the 8.5.3 AI and Section 2.1.2 it is recommended to close this discussion as a part of evaluation enhancements and continue discussion as a part of AI 8.5.3. Therefore, it is proposed to close discussion on this topic.

# NR Positioning Physical Layer Latency Evaluation

## Rel.16 UE-Assisted DL-TDOA/DL-AOD Positioning

### Discussion Round #1

Companies are invited to fill in the table below for achievable physical layer latency of UE-assisted DL-TDOA/DL-AOD positioning

|  |  |  |
| --- | --- | --- |
| Source  Reference to Tdoc # | Physical layer latency for DL-TDOA/DL-AOD, ms | Comments on major assumptions and physical layer latency components |
| Source #1: | FR1:  FR2: | Major assumptions:  Major components: |
| Qualcomm | [57-823] | Major Assumption: Connected state, FR1, (N,T) = (6,8) PRS capability  Major components: Location Request reception, MG request & configuration, PRS/MG Alignment, PRS processing capabilities |
| Huawei/HiSilicon1  R1-2007576 | FR1:  51.5-66ms (1 samp.)  111.5-126.5ms (4 samp. CSSF = 1)  171.5-186ms (4 samp. CSSF = 2) | Major assumptions:  PRS periodicity is 20ms  MG is requested  Major components  PRS measurement |
| Huawei/HiSilicon2  R1-2007576 | FR1:  171.5-178.5ms (1 samp.)  651.5-658.5ms (4 samp. CSSF = 1) | Major assumptions:  PRS periodicity is 160ms  MG is not requested (sharing with existing RRM gap 6ms/40ms)  Major components  PRS measurement |
| ZTE | FR1:106.23 ms  FR2: 667.87 ms | Major assumptions:  RRC Connected;4 samples;CSSF=1;Measurement Gap Repetition Period is 20ms.  Major components:  Measurement gap request procedures  UE positioning measurement |
| vivo  R1-2007665 | FR1:  [64-11556]  FR2：  [728-328996] | Major assumptions and components:  For FR1: DL measurement &process delay=**,** PRS and MG is periodicity   * the minimum value is 22ms for **，**(N,T) = (6,8) * the maximum value is 11514 ms for **，**(N,T) = (6,1280)   For FR2:  **,** ,   * the minimum value is 20\*4\*8+2ms =642ms * the maximum value is (10240+1280-6)=328954ms   MG request and configuration  Location Request and report |
| Lenovo, Motorola Mobility 1 (R1-2007997) | FR1: [38-235.6]  FR2: [35-229.6] | Major Assumptions: Start and End States: RRC\_CONNECTED, MG configuration enabled, MGRP = 20ms-160ms, 1 DL PRS occasion, T=8-160 ms DL PRS processing time.  Major Components: Request Location reception and processing, MG request & configuration, DL PRS Measurement and Processing, Provide Location transmission and processing. |
| Lenovo, Motorola Mobility 2 (R1-2007997) | FR1: [17-5147.8]  FR2: [15.5-5144.8] | Major Assumptions: Start and End States: RRC\_CONNECTED, Without MG configuration, DL PRS periodicity =4-5120ms, 1 DL PRS occasion, T=8ms DL PRS processing time.  Major Components: Request Location reception and processing, DL PRS Measurement and Processing, Provide Location transmission and processing. |
| LG (R1-2008416) | FR1:  For UE capability-1:  73.12+[X]ms ~ 217.12+[X]ms  For UE capability-2:  71.68+ [X]ms ~ 215.26+[X]ms | Major assumptions:  -For PUSCH transmission:   * Uplink switching gap is not configured. * No BWP switching * No overlapping symbols of the PUCCH and the scheduled PUSCH * # of PUSCH symbols = from 4 to 14 for Type A * # of PUSCH symbols = from 1 to 14 for Type B   -For PDSCH transmission:   * No overlapping symbols of the scheduling PDCCH and the scheduled PDSCH * # of PDSCH symbols = from 3 to 14 for Type A * # of PDSCH symbols = from 2 to 14 for Type B   -[X]: Processing delay at gNB in terms of physical layer (Up to gNB capability)  Major components   * RRC processing time for LPP message at both gNB and UE (LPP request location information message, measurement gap request message, LPP provide location information message) * PRS measurement (LCM of PRS resource periodicity and repetition periodicity of the measurement gap)   - If the latency components related with higher layer are excluded, the physical layer latency is described as follows:   * For UE capability-1: 23.12ms ~ 167.12ms (FR1)   For UE capability-2: 21.68ms ~ 165.26ms (FR1) |
| CATT(R1-2007859) | FR1: 51.5ms | -Major Assumptions: Case 1, 15kHz, FR1, DL-TDOA  Source UE/Destination NW  Positioning technique DL-TDOA, type DL, mode UE-assisted,  Initial and Final RRC States CONNECTED.  -Major Components: require measurement gap, measurement gap configuration, the delay between the time when DL PRS is received and the time when measurement gap configuration is received, the time from UE begins to measure PRS until the measurement result is ready to report, measurement reporting. |
| Nokia (R1-2008300) | FR1: [13.07 – 2956.71] ms | Major Assumptions: 15 kHz SCS  Source NW/ Destination NW. UE-assisted. Excluding MG configuration.  Major components:   * DL PRS periodicity * DL PRS processing time * SR related steps |
| OPPO | FR1: 54.125ms for 60KHz  FR2: 52.56ms for 120KHz | Major Assumptions: 60KHz for FR1 and 120KHz for FR2  Major components:   * Process Location Request reception, * MG request & configuration, * PRS measurement and processing * PUSCH carrying measurement report |
| Interdigital  (R1-2008489) | FR1: 33ms | Major assumptions:   * 30kHz SCS * Initial and final state: RRC\_CONNECTED. * The UE is configured with MG of 1.5ms, receives the PRS within the MG to conduct positioning measurement. * The UE uses a configured grant having periodicity of 1ms to report the measurement. * Best case scenario   Major components:   * Decoding the LPP request location by the UE * Decoding the MG request by the gNB * Receiving the MG configuration and apply the configuration. |
| Intel Corporation  R1-2007945 | FR1: 129.07 ms | Major assumptions:   * 30kHz SCS / FDD * Initial and final state: RRC\_CONNECTED. * DL PRS: 18 resources / 4 symbols per resource / 12 Comb-6 symbols per period. Periodicity – 20 ms. UE DL PRS processing capability – N = 0.5 ms (~12 symbols @30kHz), T = 8 ms * Dynamic DL/UL scheduling based on SR – based on URLLC assumptions [3GPP 38.824, v16.0.0] * Measurement gap: MGL = 5.5 ms, MGRP = 20ms * DL PRS processing   + Nsample = 4 (RAN4 core measurements requirements)   + UE is expected to perform measurements on DL PRS resource 4 times (i.e. across 4 periods) * Higher layer latency components (RRC/LPP processing) are included into the physical layer analysis   Major components:   * MG configuration and alignment time * DL PRS processing time and report delay * Multiple DL/UL transactions for location request, assistance information, measurement gap request and configuration and associated UE/gNB higher layer processing delays (RRC/LPP)   Summary: 4.5714 (L1 components) + 36 (L2/L3 components) + 88.5 (DL PRS processing) = 129.07 ms (total) |
|  |  |  |

### Discussion Round #2

1. **(On physical layer latency for Rel.16 DL-TDOA/DL-AOD NR positioning)**
   * **Capture summary table on physical layer latency for Rel.16 DL-TDOA/DL-AOD UE-Assisted NR positioning from discussion round #1 in the TR**
   * **Summary of physical layer latency for Rel.16 DL-TDOA/DL-AOD UE-assisted NR positioning in FR1 was provided by [11] sources**
   * **Summary of physical layer latency for Rel.16 DL-TDOA/DL-AOD UE-assisted NR positioning in FR2 was provided by [4] sources**
   * **For evaluation in FR1,**
     + **results from [11] sources out of [11] sources (Qualcomm, Huawei, ZTE, vivo, Lenovo, LGE, CATT, Nokia, OPPO, Interdigital, Intel) show that minimum estimated physical layer latency for Rel.16 DL-TDOA/DL-AOD UE-assisted NR positioning exceeds 10ms**
     + **results from [2] (ZTE, Intel) sources out of [11] sources (Qualcomm, Huawei, ZTE, vivo, Lenovo, LGE, CATT, Nokia, OPPO, Interdigital, Intel) show that minimum estimated physical layer latency for Rel.16 DL-TDOA/DL-AOD UE-assisted NR positioning exceeds 100ms**
   * **For evaluation in FR2,**
     + **results from [4] sources out of [4] sources (ZTE, vivo, Lenovo, OPPO) show that minimum estimated physical layer latency for Rel.16 DL-TDOA/DL-AOD UE-assisted NR positioning exceeds 10ms**
     + **results from [2] (ZTE, vivo) sources out of [4] sources (ZTE, vivo, Lenovo, OPPO) show that minimum estimated physical layer latency for Rel.16 DL-TDOA/DL-AOD UE-assisted NR positioning exceeds 100ms**
   * **The following list provides the major physical layer latency components for Rel.16 DL TDOA/DL-AOD UE-assisted NR Positioning**
     + **DL PRS alignment, transmission, measurement time and report delay**
     + **Measurement gap request, configuration and alignment time**
     + **UE/gNB higher layer (LPP/RRC) processing times**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| **Lenovo, Motorola Mobility** | Correction for 5th bullet, 2nd Sub-bullet (FR2 evaluation): Our evaluated minimum latency falls within the 100ms phy latency budget, and similar observation may apply also to Oppo. Oppo and our evaluation observations seem to have been swapped with Vivo and ZTE, suggest the following change:   * + - results from [2] (ZTE, vivo) sources out of [4] sources (ZTE, vivo, Lenovo, OPPO) show that minimum estimated physical layer latency for Rel.16 DL-TDOA/DL-AOD UE-assisted NR positioning exceeds 100ms |
| Nokia/NSB | Support. |
| Qualcomm | “DL PRS Alignment” in NR rel-16 should include “MG Alignment” right? Because even if we PRS every often, the smallest MG periodicity is 20 msec. |
| vivo | Share the same view with QC, MG alignment should be included. In addition, the components included in DL PRS alignment time and measurement time should be clarified. |
| Huawei/HiSilicon | Our evaluation results shows that the minimum physical layer latency is less than 100ms.  FR1:  51.5-66ms (1 samp.)  Suggest the following changes   * + **For evaluation in FR1,**     - **results from [11] sources out of [11] sources (Qualcomm, Huawei, ZTE, vivo, Lenovo, LGE, CATT, Nokia, OPPO, Interdigital, Intel) show that minimum estimated physical layer latency for Rel.16 DL-TDOA/DL-AOD UE-assisted NR positioning exceeds 10ms**     - **results from [32] (Huawei, ZTE, Intel) sources out of [11] sources (Qualcomm, Huawei, ZTE, vivo, Lenovo, LGE, CATT, Nokia, OPPO, Interdigital, Intel) show that minimum estimated physical layer latency for Rel.16 DL-TDOA/DL-AOD UE-assisted NR positioning exceeds 100ms** |
| LG | For the last main bullet, If the UE reports positioning measurement based on UL grant from gNB, the UE needs to send scheduling request before, so we would like to suggest to consider the latency of scheduling request as a physical layer latency component. Furthermore, the periodicity and offset for PUCCH can be configured by from 2 OS to 80 slots for FR1 (based on 38.331). In the case of # of slots > 1, the physical layer latency can be larger than our analysis. Similarly, the latency of UL grant is highly different depending on monitoringSlotPeriodicityAndOffset for PDCCH format 0\_0 and 0\_1 that can be from slot #1 to slot #2560. In the last bullet, we prefer to add two components such as scheduling request and UL grant for major physical layer latency components. Lastly, we’ve not analyzed the effect of buffer in this time. The total physical layer latency can be postponed when the information of measurement report cannot be transmitted at once. So, retransmission of measurement report due to buffer status also needs to be considered for major physical layer latency components. |

## Rel.16 UE-Assisted UL-TDOA/UL-AOA Positioning

### Discussion Round #1

Companies are invited to fill in the table below for achievable physical layer latency of UE-assisted UL-TDOA/UL-AOA positioning

|  |  |  |
| --- | --- | --- |
| Source  Reference to Tdoc # | Physical layer latency for UL-TDOA/UL-AOA, ms | Comments on major assumptions and physical layer latency components |
| Source #1: | FR1:  FR2: | Major assumptions:  Major components: |
| Huawei/HiSilicon  R1-2007576 | FR1:  6.5-26ms (1 samp.)  66.5-86.5ms (4 samp) | Major assumptions:  SRS periodicity is 20ms  Major components  SRS measurement |
| vivo 1  R1-2007665 | FR1:  30.5-2570.5  FR2:  650.5-10250.5 | Major assumptions:  FR1:SRS periodicity is {1, 2, 4, 5, 8, 10, 16, 20, 32, 40, 64, 80, 160, 320, 640, 1280, 2560}slots   * + 15kHz 1ms-2560ms   + 30kHz 0.5ms-1280ms   + 60kHz 0.25ms-640ms   + 120kHz 0.125ms-320ms   FR2: Multiple positioning occasion (4) and beam sweeping (8)   * UL measurement equals to the periodicity of SRS   gNB processing delay is assumed as zero；  The minimum periodicity of SRS is 20ms and the same as the DL minimum periodicity.  Major components:  SRS measurement;  NRPPa process time |
| vivo 2  R1-2007665 | FR1:  11-43 | Major assumptions:  SRS is aperiodic and the slot offset of aperiodic is 0-32 slots   * + 15kHz 0ms-32ms   + 30kHz 0ms-16ms   + 60kHz 0ms-8ms   120kHz 0ms-4ms  Major components:  SRS measurement;  NRPPa process time;  Activation; |
| LG (R1-2008416) | FR1:  For UE capability-1:  31.49+[Y] ms ~ 34.42+[Y] ms  For UE capability-2:  30.77+[Y] ms ~ 33.28+[Y] ms | Major assumptions:  -For SRS transmission:   * One shot transmission (2 OS ~ 12 OS)   -For PDSCH transmission:   * No overlapping symbols of the scheduling PDCCH and the scheduled PDSCH * # of PDSCH symbols = from 3 to 14 for Type A * # of PDSCH symbols = from 2 to 14 for Type B   -[Y]: Processing delay at gNB in terms of physical layer (Up to gNB capability)  Major components   * RRC processing time for LPP message at both gNB and UE (SRS configuration, SRS activation message)   -When the latency related with higher layer is excluded, physical layer latency is described as follows:   * For UE capability-1: 1.49ms ~ 4.42ms (FR1)   For UE capability-2: 0.77ms ~ 3.28ms (FR1) |
| CATT(R1-2007859) | FR1: 5ms | -Major Assumptions: Case 2, 15kHz, FR1, UL-TDOA  Source UE/Destination NW  Positioning technique UL-TDOA, type UL, mode UE-assisted,  Initial and Final RRC States CONNECTED  -Major Components: the time to activate the SRS transmission, the delay from effective time of SRS activation until UE begins to transmit SRS, the time from gNB begins to measure SRS until the measurement result is ready. |
| Nokia (R1-2008300) | FR1: [2.35 – 81925] ms | Major Assumptions: 15 kHz SCS  Source NW/ Destination NW. Excluding SRS-Pos RRC configuration  Major Components:   * SRS-Pos periodicity * Processing of SRS-Pos at gNB/RP-only |
| OPPO | FR1: 23.25 ms for 60kHz  FR2: 23.125ms for 120kHz | Major Assumptions: 60KHz for FR1 and 120KHz for FR2.  Major Components:   * gNB process NPPa measurement request * Configure SRS * SRS-Pos periodicity * gNB processing SRS |
| Interdigital  (R1-2008489) | FR1: 12ms | Major assumptions:   * Initial and final state: RRC\_CONNECTED. * SRS transmission resources occur immediately after decoding the SRS configuration. * 30kHz SCS * Best case scenario   Major components:   * Decoding the SRS configuration message. |
| Intel Corporation  R1-2007945 | FR1: 18.77 ms | Major assumptions:   * 30kHz SCS / FDD * Initial and final state: RRC\_CONNECTED. * Dynamic DL/UL scheduling based on SR – see URLLC assumptions [3GPP 38.824, v16.0.0] * PUSCH: Any symbol, subject to slot boundary constraint (i.e. transmission does not cross slot boundary); Duration – 2, 4, 7 symbols (Type B mapping w/ front loaded DMRS) * PUCCH: 7 occasions per slot [1,0,1,0,1,0,1,0,1,0,1,0,1,0] for SR and HARQ feedback, Duration – 1 symbol. * No HARQ – initial transmission is successful * SRS for positioning: Single resource, 1 symbol duration, Periodicity – each slot * Higher layer latency components (RRC/LPP processing) are included into the physical layer latency analysis   Major components:   * SRS for positioning configuration * UE/gNB higher layer processing delays (RRC/LPP processing)   Summary = 2.7678 (L1 components) + 16 (L2/L3 components) = 18.7678 ms (total) |

### Discussion Round #2

1. **(On physical layer latency for Rel.16 UL-TDOA/UL-AOA NR positioning)**
   * **Capture summary table on physical layer latency for Rel.16 UL-TDOA/UL-AOA NR positioning from discussion round #1 in the TR**
   * **Summary of physical layer latency for Rel.16 UL-TDOA/UL-AOA NR positioning in FR1 was provided by [8] sources (Huawei, vivo, LGE, CATT, Nokia, OPPO, Interdigital, Intel)**
   * **Summary of physical layer latency for Rel.16 UL-TDOA/UL-AOA NR positioning in FR2 was provided by [2] sources (vivo, OPPO)**
   * **For evaluation in FR1,**
     + **results from [3] sources (Huawei, CATT, Nokia) out of [8] sources (Huawei, vivo, LGE, CATT, Nokia, OPPO, Interdigital, Intel) show that minimum estimated physical layer latency for Rel.16 UL-TDOA/UL-AOA NR positioning does not exceed 10ms**
     + **results from [8] sources out of [8] sources (Huawei, vivo, LGE, CATT, Nokia, OPPO, Interdigital, Intel) show that minimum estimated physical layer latency for Rel.16 UL-TDOA/UL-AOA NR positioning does not exceed 100ms**
   * **For evaluation in FR2,**
     + **results from [2] sources out of [2] sources (vivo, OPPO) show that minimum estimated physical layer latency for Rel.16 UL-TDOA/UL-AOA NR positioning exceeds 10ms**
     + **results from [1] (OPPO) sources out of [2] sources (vivo, OPPO) show that minimum estimated physical layer latency for Rel.16 UL-TDOA/UL-AOA NR positioning does not exceed 100ms**
   * **The following list provides the major physical layer latency components for Rel.16 UL-TDOA/UL-AOA NR Positioning**
     + **[SRS for positioning configuration time]**
     + **SRS for positioning processing time**
     + **SRS for positioning alignment time (depends on periodic or aperiodic SRS for positioning)**
     + **gNB higher layer processing delays (RRC/ NRPPa processing times)**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| **InterDigital** | **Regarding the following texts, should they be corrected as follows?**   * + **For evaluation in FR1,**     - **results from [3] sources (Huawei, CATT, Nokia) out of [8] sources (Huawei, vivo, LGE, CATT, Nokia, OPPO, Interdigital, Intel) show that minimum estimated physical layer latency for Rel.16 UL-TDOA/UL-AOA UE-assisted NR positioning does not exceed 10ms** |
| **Lenovo, Motorola Mobility** | Correction for 5th bullet, 2nd Sub-bullet (FR2 Evaluation):   * + For evaluation in FR2,     - results from [1] (OPPO) sources out of [2] sources (vivo, OPPO) show that minimum estimated physical layer latency for Rel.16 UL-TDOA/UL-AOA UE-assisted NR positioning does not exceed 100ms |
| **Nokia/NSB** | Same comment as InterDigital. Haven’t checked all companies but at least Nokia results show the latency does not exceed 10 ms. |
| **vivo** | Support in principle, but whether “SRS processing time” includes SRS alignment time for periodic and aperiodic SRS? If not, we suggest adding SRS alignment time. In addition, whether periodic SRS and aperiodic SRS are discussed separately? |
| **Huawei/HiSilicon** | Same view as IDC/Nokia. I guess there should be “does not” for 10ms.  In addition, we suggest revise the wording “UE assisted” UL-TDOA/UL-AoA. Rel-16 does not support UE assisted UL-only positioning method; more precisely, it should be NG-RAN assistend.  Third, we do not think SRS configuration is included in physical layer latency. Can proponents clarify?  Last, we do not think LPP protocol is involved in physical layer latency analysis.  The suggested changes   1. **(On physical layer latency for Rel.16 UL-TDOA/UL-AOA NR positioning)**    * **Capture summary table on physical layer latency for Rel.16 UL-TDOA/UL-AOA NG-RAN-assisted NR positioning from discussion round #1 in the TR**    * **Summary of physical layer latency for Rel.16 UL-TDOA/UL-AOA NG-RAN-assisted NR positioning in FR1 was provided by [8] sources (Huawei, vivo, LGE, CATT, Nokia, OPPO, Interdigital, Intel)**    * **Summary of physical layer latency for Rel.16 UL-TDOA/UL-AOA NG-RAN-assisted NR positioning in FR2 was provided by [2] sources (vivo, OPPO)**    * **For evaluation in FR1,**      + **results from [3] sources (Huawei, CATT, Nokia) out of [8] sources (Huawei, vivo, LGE, CATT, Nokia, OPPO, Interdigital, Intel) show that minimum estimated physical layer latency for Rel.16 UL-TDOA/UL-AOA NG-RAN-assisted NR positioning does not exceed 10ms**      + **results from [8] sources out of [8] sources (Huawei, vivo, LGE, CATT, Nokia, OPPO, Interdigital, Intel) show that minimum estimated physical layer latency for Rel.16 UL-TDOA/UL-AOA NG-RAN-assisted NR positioning does not exceed 100ms**    * **For evaluation in FR2,**      + **results from [2] sources out of [2] sources (vivo, OPPO) show that minimum estimated physical layer latency for Rel.16 UL-TDOA/UL-AOA NG-RAN-assisted NR positioning exceeds 10ms**      + **results from [2] (Lenovo, OPPO) sources out of [2] sources (vivo, OPPO) show that minimum estimated physical layer latency for Rel.16 UL-TDOA/UL-AOA NG-RAN-assisted NR positioning does not exceed 100ms**    * **The following list provides the major physical layer latency components for Rel.16 UL-TDOA/UL-AOA NG-RAN-assisted NR Positioning**      + **SRS processing time**      + **gNB higher layer processing delays (RRC/NRPPa processing times)** |
| **LG** | We are on the same page with InterDigital. In case of our contribution, if the higher layer is considered, the physical layer latency exceeds 10ms, otherwise it does not exceed. In our understating, we think that the first thing to be decided is whether the components related with higher layer should be excluded or not. |

## Rel.16 UE-Assisted Multi-RTT Positioning

### Discussion Round #1

Companies are invited to fill in the table below for achievable physical layer latency of UE-assisted Multi-RTT positioning

|  |  |  |
| --- | --- | --- |
| Source  Reference to Tdoc # | Physical layer latency for Multi-RTT, ms | Comments on major assumptions and physical layer latency components |
| Source #1: | FR1:  FR2: | Major assumptions:  Major components: |
| Qualcomm | [59-823] | Major assumptions: Connected state, FR1, (N,T) = (6,8) PRS capability  Major components: Location Request Reception, MG Request & Configuration, PRS/MG Alignment, PRS processing capabilities |
| Huawei/HiSilicon1  R1-2007576 | FR1:  51.5-66ms (1 samp.)  111.5-126.5ms (4 samp. CSSF = 1)  171.5-186ms (4 samp. CSSF = 2) | Major assumptions:  PRS periodicity is 20ms  MG is requested  Major components  PRS measurement |
| Huawei/HiSilicon2  R1-2007576 | FR1:  171.5-178.5ms (1 samp.)  651.5-658.5ms (4 samp. CSSF = 1) | Major assumptions:  PRS periodicity is 160ms  MG is not requested (sharing with existing RRM gap 6ms/40ms)  Major components  PRS measurement |
| vivo 1  R1-2007665 | FR1:  [94.5-14126.5] + | Major assumptions and components:  For FR1: DL measurement &process delay =**,** PRS and MG is periodicity   * the minimum value is 22ms for **，**(N,T) = (6,8) * the maximum value is 11514 ms for **，**(N,T) = (6,1280)   FR1:SRS periodicity is {1, 2, 4, 5, 8, 10, 16, 20, 32, 40, 64, 80, 160, 320, 640, 1280, 2560}slots   * + 15kHz 1ms-2560ms   + 30kHz 0.5ms-1280ms   + 60kHz 0.25ms-640ms   + 120kHz 0.125ms-320ms   : The alignment delay is the gap between End trigger of DL positioning and Start trigger of UL positioning.  MG request and configuration  Location Request and report |
| LG (R1-2008416) | FR1:  For UE capability-1:  145.34ms+[Z] ~ 293.32+[Z]ms  For UE capability-2:  142.8+[Z]ms ~  289.75+[Z] ms | Major assumptions:  -For PUSCH transmission:   * Uplink switching gap is not configured. * No BWP switching * No overlapping symbols of the PUCCH and the scheduled PUSCH * # of PUSCH symbols = from 4 to 14 for Type A * # of PUSCH symbols = from 1 to 14 for Type B   -For PDSCH transmission:   * No overlapping symbols of the scheduling PDCCH and the scheduled PDSCH * # of PDSCH symbols = from 3 to 14 for Type A * # of PDSCH symbols = from 2 to 14 for Type B   -For SRS transmission:   * One shot transmission (2 OS ~ 12 OS)   -[Z]: Processing delay at gNB in terms of physical layer (Up to gNB capability)  Major components   * RRC processing time for LPP message at both gNB and UE (SRS configuration, SRS activation message, LPP request location information message, measurement gap request message, LPP provide location information message) * PRS measurement (LCM of PRS resource periodicity and repetition periodicity of the measurement gap)   -When the latency related with higher layer is excluded, physical layer latency is described as follows:   * For UE capability-1: 25.34ms ~ 173.32ms (FR1)   For UE capability-2: 22.8ms ~169.75ms (FR1) |
| Interdigital  (R1-2008489) | FR1: 45ms | Major assumptions:   * Initial and final state: RRC\_CONNECTED. * The UE is configured with MG of 1.5ms, receives the PRS within the MG to conduct positioning measurement. * The UE uses a configured grant having periodicity of 1ms to report the measurement. * SRS transmission resources occur immediately after decoding the SRS configuration. * 30kHz SCS * Best case scenario   Major components:   * Decoding the LPP request location by the UE * Decoding the MG request by the gNB * Receiving the MG configuration and apply the configuration. * Receiving PRS in the MG * Decoding the SRS configuration message. |
| Intel Corporation  R1-2007945 | 140.84 ms | Major assumptions:   * 30kHz SCS / FDD * Initial and final state: RRC\_CONNECTED. * DL PRS: 18 resources / 4 symbols per resource / 12 Comb-6 symbols per period. Periodicity – 20 ms. UE DL PRS processing capability – N = 0.5 ms (~12 symbols @30kHz), T = 8 ms * Dynamic DL/UL scheduling based on SR – based on URLLC assumptions [3GPP 38.824, v16.0.0] * Measurement gap: MGL = 5.5 ms, MGRP = 20ms * DL PRS processing   + Nsample = 4 (RAN4 core measurements requirements)   + UE is expected to perform measurements on DL PRS resource 4 times (i.e. across 4 periods) * PUSCH: Any symbol, subject to slot boundary constraint (i.e. transmission does not cross slot boundary); Duration – 2, 4, 7 symbols (Type B mapping w/ front loaded DMRS) * PUCCH: 7 occasions per slot [1,0,1,0,1,0,1,0,1,0,1,0,1,0] for SR and HARQ feedback, Duration – 1 symbol. * No HARQ – initial transmission is successful * SRS for positioning: Single resource, 1 symbol duration, Periodicity – each slot * Higher layer latency components (RRC/LPP processing) are included into the physical layer latency analysis   Major components:   * MG configuration and alignment time * DL PRS processing time and report delay * Multiple DL/UL transactions and associated UE/gNB RRC/LPP processing delays   Summary:  7.3393 (L1 components) + 45 (L2/L3 components) + 88.5 (DL PRS processing) = 140.8393 (total) |
|  |  |  |

### Discussion Round #2

1. **(On physical layer latency for Rel.16 Multi-RTT NR positioning)**
   * **Capture summary table on physical layer latency for Rel.16 Multi-RTT UE-assisted NR positioning from discussion round #1 in the TR**
   * **Summary of physical layer latency for Rel.16 Multi-RTT UE-assisted NR positioning in FR1 was provided by [6] sources (Qualcomm, Huawei, vivo, LGE, Interdigital, Intel)**
   * **Summary of physical layer latency for Rel.16 Multi-RTT UE-assisted NR positioning in FR2 was provided by [0] sources**
   * **For evaluation in FR1,**
     + **results from [6] sources (Qualcomm, Huawei, vivo, LGE, Interdigital, Intel) out of [6] sources (Qualcomm, Huawei, vivo, LGE, Interdigital, Intel) show that minimum estimated physical layer latency for Rel.16 Multi-RTT UE-assisted NR positioning exceeds 10ms**
     + **results from [4] sources (Qualcomm, Huawei, vivo, Interdigital) out of [6] sources (Qualcomm, Huawei, vivo, LGE, Interdigital, Intel) show that minimum estimated physical layer latency for Rel.16 Multi-RTT UE-assisted NR positioning does not exceed 100ms**
   * **The following list provides the major physical layer latency components for Rel.16 Multi-RTT UE-assisted NR positioning**
     + **DL PRS alignment, transmission, measurement time and report delay**
     + **Measurement gap request, configuration, alignment time**
     + **[SRS for positioning configuration time]**
     + **SRS for positioning processing time**
     + **SRS for positioning alignment time (depends on periodic or aperiodic SRS for positioning)UE/gNB higher layer (LPP/RRC/NRPPa) processing times**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| Qualcomm | “DL PRS Alignment” in NR rel-16 should include “MG Alignment” right? Because even if we PRS every often, the smallest MG periodicity is 20 msec. |
| vivo | It is weird for us that the component of SRS latency is “SRS process time”, but PRS is “DL PRS alignment and measurement time”. Further clarification is needed for these components. |
| Huawei/HiSilicon | We do not think SRS configuration is included in physical layer latency. Can proponents clarify? |
| LG | Same view with our comment in the section 3.1.2. |

## Rel.16 UE-Assisted E-CID Positioning

### Discussion Round #1

Companies are invited to fill in the table below for achievable physical layer latency of UE-assisted E-CID positioning

|  |  |  |
| --- | --- | --- |
| Source  Reference to Tdoc # | Physical layer latency for ECID, ms | Comments on major assumptions and physical layer latency components |
| Source #1: | FR1:  FR2: | Major assumptions:  Major components: |
| Huawei/HiSilicon 1  R1-2007576 | FR1  8.5-15ms | Major assumptions:  DL E-CID  RRM measurement available  Major components  Higher layer signaling processing |
| Huawei/HiSilicon 2  R1-2007576 | FR1  6-26ms | Major assumptions:  UL E-CID  RRM measurement available  Major components  Higher layer signaling processing, or  Additional AoA measurement at gNB |
| ZTE | FR1  10.30 ms | Major assumptions:  DL E-CID  RRM measurement is available at UE side.  Major components:  UE interprets and applies the measurement configuration |
| LG (R1-2008416) | FR1:  For UE capability-1:  21.56+[M]ms ~ 23.56+[M] ms  For UE capability-2:  20.84+[M] ms~22.63+[M] ms | Major assumptions:  -For PUSCH transmission:   * Uplink switching gap is not configured. * No BWP switching * No overlapping symbols of the PUCCH and the scheduled PUSCH * # of PUSCH symbols = from 4 to 14 for Type A * # of PUSCH symbols = from 1 to 14 for Type B   -[M]: Processing delay at gNB in terms of physical layer (Up to gNB capability)  Major components   * RRC processing time for LPP message at both gNB and UE (LPP provide location information message)   -When the latency related with higher layer is excluded, physical layer latency is described as follows:   * For UE capability-1: 1.56ms ~ 3.56ms (FR1) * For UE capability-2: 0.84ms~2.63ms (FR1) |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

### Discussion Round #2

1. **(On physical layer latency for Rel.16 E-CID NR positioning)**
   * **Capture summary table on physical layer latency for Rel.16 E-CID NR positioning from discussion round #1 in the TR**
   * **Summary of physical layer latency for Rel.16 E-CID NR positioning in FR1 was provided by [3] sources (Huawei, ZTE, LGE)**
   * **Summary of physical layer latency for Rel.16 E-CID NR positioning in FR2 was provided by [0] sources**
   * **For evaluation in FR1,**
     + **results from [2] sources (ZTE, LGE) out of [3] sources (Huawei, ZTE, LGE) show that minimum estimated physical layer latency for Rel.16 E-CID NR positioning exceeds 10ms**
     + **results from [3] sources (Huawei, ZTE, LGE) out of [3] sources (Huawei, ZTE, LGE) show that minimum estimated physical layer latency for Rel.16 E-CID NR positioning does not exceed 100ms**
   * **The following list provides the major physical layer latency components for Rel.16 E-CID NR positioning**
     + **Higher layer signaling processing**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| **Huawei/HiSilicon** | We do not think that “UE-assisted E-CID” may be appropriate, as we have DL E-CID and UL E-CID as agreed in the previous meeting.  Suggest to change as follows   1. **(On physical layer latency for Rel.16 E-CID NR positioning)**    * **Capture summary table on physical layer latency for Rel.16 E-CID NR positioning from discussion round #1 in the TR**    * **Summary of physical layer latency for Rel.16 E-CID NR positioning in FR1 was provided by [3] sources (Huawei, ZTE, LGE)**    * **Summary of physical layer latency for Rel.16 E-CID NR positioning in FR2 was provided by [0] sources**    * **For evaluation in FR1,**      + **results from [2] sources (ZTE, LGE) out of [3] sources (Huawei, ZTE, LGE) show that minimum estimated physical layer latency for Rel.16 E-CID NR positioning exceeds 10ms**      + **results from [3] sources (Huawei, ZTE, LGE) out of [3] sources (Huawei, ZTE, LGE) show that minimum estimated physical layer latency for Rel.16 E-CID NR positioning does not exceed 100ms**    * **The following list provides the major physical layer latency components for Rel.16 E-CID NR positioning**      + **Higher layer signaling processing** |
| **LG** | Same view with our comment in the section 3.1.2. |

## Rel.16 UE-Based DL Only Positioning

### Discussion Round #1

Companies are invited to fill in the table below for achievable physical layer latency of UE-based DL-only positioning

|  |  |  |
| --- | --- | --- |
| Source  Reference to Tdoc # | Physical layer latency for UE-based DL only positioning, ms | Comments on major assumptions and physical layer latency components |
| Source #1: | FR1:  FR2: | Major assumptions:  Major components: |
| Qualcomm1 | [46-811] | Major assumptions: Start from RRC Connected, FR1, (N,T)=(6,8), External client  Major components: Location Request reception, MG request & configuration, MG/PRS alignment, PRS processing capabilities |
| Qualcomm2 | [8-780] | Major assumptions: Start from RRC Inactive, FR1, (N,T)=(6,8) , Internal client  Major components: PRS alignment time, PRS processing capabilities |
| Huawei/HiSilicon  R1-2007576 | FR1  51-58.5ms (1 samp.) | Major assumptions:  PRS periodicity is 20ms  MG is requested  MO-LR  Major components  PRS measurement |
| vivo 1  R1-2007665 | FR1:  [66-11558]  FR2：  [730-328998] | Major assumptions and components:  For FR1: DL measurement &process delay=, PRS and MG is periodicity  MG request and configuration  Calculation of Location Estimate at the UE  Location Request and report  MT-LR |
| vivo 2  R1-2007665 | FR1:  [55.5-11547.5]  FR2：  [719.5-328987.5] | Major assumptions and components:  For FR1: DL measurement &process delay=, PRS and MG is periodicity  MG request and configuration  Location Request  Calculation of Location Estimate at the UE  MO-LR |
| Lenovo, Motorola Mobility1 (R1-2007997) | FR1: [29-207.8]  FR2: [27.5 -204.8] | Major Assumptions: Start and End States: RRC\_CONNECTED, MGRP = 20ms-160ms, 1 DL PRS occasion, T=8ms-160ms PRS processing time, Request and provide location information messages omitted.  Major Components: MG request & configuration, DL PRS Measurement and Processing. |
| Lenovo, Motorola Mobility2 (R1-2007997) | [8-5120] | Major Assumptions: Start and End States: RRC\_CONNECTED, Without MG configuration, DL PRS periodicity=4-5120ms, 1 DL PRS occasion, T=8ms DL PRS processing time, Request and provide location information messages omitted.  Major Components: DL PRS Measurement and Processing. |
| OPPO | 44ms | Major Assumption:   * Start time: UE sends MG request * End time: UE finish location calculation   Major component:   * MG request and configuration * Measurement gap periodicity * UE calculating location |
| Interdigital  (R1-2008489) | FR1 :  [39-61] ms for Alt. 1,  [50-72] ms for Alt. 2,  [22-44] ms for Alt. 3,  where different alternatives correspond to different starting points for latency evaluation of UE-B positioning | Major assumptions:   * 30kHz SCS * Initial and final state: RRC\_CONNECTED. * The UE is configured with MG of 1.5ms, receives the PRS within the MG to conduct positioning measurement. (for Alt 1 & 2) * The UE uses a configured grant having periodicity of 1ms to report the measurement. (for Alt 1 & 2 & 3) * Best case scenario   Major components:   * Decoding the LPP request location by the UE (for Alt 2) * Decoding the MG request by the gNB (for Alt 1 & 2) * Receiving the MG configuration and apply the configuration. (for Alt 1 & 2) * UE calculating location (for Alt 1 & 2 & 3) |
|  |  |  |
|  |  |  |

### Discussion Round #2

1. **(On physical layer latency for Rel.16 DL-only UE-based NR positioning)**
   * **Capture summary table on physical layer latency for Rel.16 DL-only UE-based NR positioning from discussion round #1 in the TR**
   * **Summary of physical layer latency for Rel.16 DL-only UE-based NR positioning in FR1 was provided by [6] sources (Qualcomm, Huawei, vivo, Lenovo, OPPO, Interdigital)**
   * **Summary of physical layer latency for Rel.16 DL-only UE-based NR positioning in FR2 was provided by [2] sources (vivo, Lenovo)**
   * **For evaluation in FR1,**
     + **results from [4] sources (Huawei, vivo, OPPO, Interdigital) out of [6] sources (Qualcomm, Huawei, vivo, Lenovo, OPPO, Interdigital) show that minimum estimated physical layer latency for Rel.16 DL-only UE-based NR positioning exceeds 10ms**
     + **results from [6] sources out of [6] sources (Qualcomm, Huawei, vivo, Lenovo, OPPO, Interdigital) show that minimum estimated physical layer latency for Rel.16 DL-only UE-based NR positioning does not exceed 100ms**
   * **For evaluation in FR2,**
     + **results from [2] sources out of [2] sources (vivo, Lenovo) show that minimum estimated physical layer latency for Rel.16 DL-only UE-based NR positioning exceeds 10ms**
     + **results from [1] (vivo) sources out of [2] sources (vivo, Lenovo) show that minimum estimated physical layer latency for Rel.16 DL-only UE-based NR positioning exceeds 100ms**
   * **The following list provides the major physical layer latency components for Rel.16 DL-only UE-based NR positioning**
     + **DL PRS alignment and measurement time**
     + **Measurement gap request and configuration**
     + **Higher layer (LPP/RRC) processing times**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| **Lenovo, Motorola Mobility** | Support. Suggest a minor 2nd Column title modification in Table: “Physical layer latency for UE-Based DL only positioning, ms” |
| Qualcomm | For the case of (Start from RRC Inactive, FR1, (N,T)=(6,8) , Internal client) the 10msec goal could be met |
| vivo | Support in principle, but it is more reasonable to separate observation for idle and connected state |

## NR Positioning Enhancements

### Physical Layer Latency of Enhancements (Closed)

#### Discussion Round #1

1. **(On Physical Layer Latency of Enhanced NR Positioning Solutions)**
   * **The following latency reduction enhancements are considered/recommended by companies**
     + **Support of on demand DL PRS transmission**
     + **Support of a-periodic / semi-persistent DL PRS transmission**
     + **Measurement gap enhancements (e.g. gap less operation, pre-configured gaps activated by low layer signaling, etc.)**
     + **Enhanced UE DL PRS processing capabilities**
     + **Low layer signaling (DCI/MAC CE) for NR positioning procedures and procedural enhancements**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| **CATT** | **Okay** |
| **Huawei/HiSilicon** | **As commented, any enhancement on physical layer latency/E2E latency that requires complicated signalling design (i.e. introducing new signalings and procedures) cannot have easy conclusions, as the addition of procedures add another issues.**  **For this particular observation, since we are listing company recommendation here, we suggest to address the potential enhancement on ePos-03.** |
| **vivo** | **Support** |
| **LG** | **This observation is related to the enhancements, so it seems that this issue could be jointly discussed in the second main bullet in 2.3.2.1** |
| **Intel** | **Support the proposal.**  **Suggest rephrasing the main bullet as follows:**   * + **The following latency reduction enhancements were evaluated ~~are considered/recommended~~ by companies and have shown latency reduction:** |
| **Nokia/NSB** | **Suggest a further revision of Intel’s wording to say that the enhancement may have latency reduction. While we did not explicitly evaluate it in our Tdoc we also proposed UE could request the expected measurement report resource from the serving gNB via RRC ignalling to minimize the positioning measurement report delay and think this could be included in the list.** |
| **InterDigital** | **Support** |
| **LG2** | **We mentioned that this needs to be discussed in AI 8.5.3 before. In consideration of the current state, however, there are a lot of issues and proposals needed to be discussed in AI 8.5.3. If we need to discuss the potential enhancement for the latency reduction here, we would like to add an additional sub-bullet for latency reduction. In our view, the following features can be considered to reduce reporting latency.**   * **UE request of MG with reporting resources** * **MG configuration with reporting resource** |

#### Discussion Round #2 (Closed)

Based on received responses in discussion round #1 on overlap with the 8.5.3 AI it is recommended to close this discussion as a part of evaluation enhancements and continue discussion as a part of AI 8.5.3. Therefore, it is proposed to close discussion on this topic.

### NR Positioning In RRC\_INACTIVE State (Closed)

#### Discussion Round #1

1. **(On UE Positioning in RRC\_INACTIVE States)**
   * **Support of UE positioning in RRC\_INACTIVE state provides latency saving due to lack of transition to RRC\_CONNECTED state**

Companies are invited to provide views on above observations in table below

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| **CATT** | **Okay. Maybe change “due to lack of” to “due to no need of”** |
| **Huawei/HiSilicon** | **We are not sure of the baseline that the latency gain is achieved against. For example, if the UE is always in CONNECTED state, we do not see latency reduction compared to IDLE/INACTIVE state.** |
| **vivo** | **Change RRC\_INACTIVE States to RRC\_IDLE / RRC\_INACTIVE States**   1. **(On UE Positioning in RRC\_IDLE /RRC\_INACTIVE States)**    * **Support of UE positioning in RRC\_IDLE /RRC\_INACTIVE state provides latency saving ~~due to lack of~~ due to no need of transition to RRC\_CONNECTED state** |
| **LG** | **Agree with CATT’s comment.** |
| **Intel** | **Agree with comment from CATT.** |
| **Nokia/NSB** | **Agree with comment from CATT.** |
| **OPPO** | **On top of the comment from CATT, suggest to update the wording as follows:**   * + **~~Support of~~ It is observed that UE positioning in RRC\_INACTIVE state provides latency saving due to no need of lack of transition to RRC\_CONNECTED state** |
| **Huawei/HiSilicon** | **We cannot agree because**   * **It is very hard to justify latency gain of INACTIVE state positioning over Rel-16 RRC\_CONNECTED state positioning.** * **Our understanding is that IDLE/INACTIVE state positioning can provide UE efficiency (power consumption gain).** * **We should not create a middle state of “measurement in IDLE/INACTIVE and report in CONNECTED” to claim latency benefit of “measurement in IDLE/INACTIVE and report in IDLE/INACTIVE”, where both of them are not supported in Rel-16.** |

#### Discussion Round #2 (Closed)

The support of NR positioning in RRC\_INACTIVE state was already agreed by RAN WG1. Therefore, it is proposed to close discussion on this topic.

# Network, UE Efficiency Evaluation for NR Positioning

The results for the network and UE efficiency evaluation were provided by 3 out of 17 sources.

In source [[1], Huawei, HiSi], the following observations were made for PRS resource utilization:

* For PRS with 12 symbols, positioning resource utilization: 2.14 %
* For PRS with 4 symbols, positioning resource utilization: 0.714 %
* For PRS with 1 symbol, positioning resource utilization: 0.179 %
* By reducing the PRS symbols from 12 and 4 to 1 for comb-12 and comb-4, respectively, the overhead of PRS transmission is reduced by 11/12 and 3/4, respectively.
* Moreover, by allowing 1-symbol PRS transmission, network may reuse CSI-RS for mobility for positioning, further reducing the PRS overhead.

The following observations were made with respect to UE efficiency (power saving) in the IDLE/INACTIVE state:

* IDLE/INACTIVE state positioning can save about 7%-40% power consumption compared to C-DRX configuration.

In source [[4], CATT], the following observations were made with respect to the Carrier Phase Positioning (CPP) scheme:

* NR positioning enhancements with carrier phase measurements has no impact on UE and network RF resource usage efficiency.

In source [[16], vivo], the following observations were made for PRS resource utilization:

* The network efficiency exceeds 100% and the MGL/MGRP (UE efficiency) exceeds 30% in some FR2 cases. The detailed PRS resource utilization for different PRS periodicities are provided in table 8.3.1.3.2-2
* The network and device efficiency will be reduced by on-demand PRS within the same level latency compared to periodic PRS.
* The network and device efficiency of aperiodic PRS is multiple of the number of activations.

In [[16], vivo], the following observations were made with respect to UE efficiency (power saving) based on different power saving solutions:

* when PRS measurement is impacted by DRX (reception 1 PRS occasion in DRX active time every DRX cycle (160ms)), 34.19% power saving gain is shown, comparing with PRS measurement regardless of DRX(reception 2 PRS occasions every DRX cycle (160ms), 1 PRS occasion within DRX active time, 1 PRS occasion out of DRX active time) .
* by extending the PRS period to 2 times(160ms to 320ms), 22.03% power saving gain is shown ,comparing with the baseline assumption. By extending the PRS period to 4 times(160ms to 640ms), 33.05 % power saving gain is shown ,comparing with the baseline assumption(PRS period of 160ms).
* when configuring concentrated PRS measurement (1 concentrated PRS occasion every 160ms), 18.77% power saving gain is shown, comparing with the distributed PRS measurement (4 distributed PRS occasion every 160ms).
* by adding the PRS measurement window to limit PRS measurement in 2ms (from 4ms to 2ms), 20.48% power saving gain is shown, comparing with PRS measurement without PRS measurement window (the baseline assumption of 4ms duration).
* by reducing the number of TRPs for PRS measurement (from 8 TRPs to 4 TRPs), 8.51% power saving gain is shown ,comparing with the baseline assumption(8 TRPs).
* by increasing the number of frequency layers to 2 (from 1 to 2), 47.61% power consumption gain is shown, comparing with the baseline assumption.
* by reducing the number of frequency layer to 2 (from 4 to 2), 36.91% power saving gain is shown; by reducing number of frequency layer to 1 (from 4 to 1), 57.26% power saving gain is shown.

In source [[16], vivo],the following observations were made with respect to UE efficiency (power saving) in the IDLE/INACTIVE state:

* Under the premise of idle state measurement, positioning report in the idle state can obtain 44.32% power saving gain compared to report in connected state.

Compared to positioning measurement and report all in the connected state, positioning measurement and report in the idle state can obtain at least 48.38% power saving gain.

|  |  |
| --- | --- |
| **Company Name** | **Comments** |
| **vivo** | We also provided R16 PRS resource utilization in our Tdoc, please capture here  In source [[16], vivo], the following observations were made for PRS resource utilization:   * The network efficiency exceeds 100% and the MGL/MGRP (UE efficiency) exceeds 30% in some FR2 cases. The detailed PRS resource utilization for different PRS periodicities are provided in table 8.3.1.3.2-2 * The network and device efficiency will be reduced by on-demand PRS within the same level latency compared to periodic PRS. * The network and device efficiency of aperiodic PRS is multiple of the number of activations.   In addition, our UE efficiency (power saving) evaluation results in source [[16], vivo] is also worthy to be captured as follows:  In source [[16], vivo], the following observations were made with respect to UE efficiency (power saving) based on different power saving solutions:   * when PRS measurement is impacted by DRX (reception 1 PRS occasion in DRX active time every DRX cycle (160ms)), 34.19% power saving gain is shown, comparing with PRS measurement regardless of DRX(reception 2 PRS occasions every DRX cycle (160ms), 1 PRS occasion within DRX active time, 1 PRS occasion out of DRX active time) . * by extending the PRS period to 2 times(160ms to 320ms), 22.03% power saving gain is shown ,comparing with the baseline assumption. By extending the PRS period to 4 times(160ms to 640ms), 33.05 % power saving gain is shown ,comparing with the baseline assumption(PRS period of 160ms). * when configuring concentrated PRS measurement (1 concentrated PRS occasion every 160ms), 18.77% power saving gain is shown, comparing with the distributed PRS measurement (4 distributed PRS occasion every 160ms). * by adding the PRS measurement window to limit PRS measurement in 2ms (from 4ms to 2ms), 20.48% power saving gain is shown, comparing with PRS measurement without PRS measurement window (the baseline assumption of 4ms duration). * by reducing the number of TRPs for PRS measurement (from 8 TRPs to 4 TRPs), 8.51% power saving gain is shown ,comparing with the baseline assumption(8 TRPs). * by increasing the number of frequency layers to 2 (from 1 to 2), 47.61% power consumption gain is shown, comparing with the baseline assumption. * by reducing the number of frequency layer to 2 (from 4 to 2), 36.91% power saving gain is shown; by reducing number of frequency layer to 1 (from 4 to 1), 57.26% power saving gain is shown.   In source [[16], vivo],the following observations were made with respect to UE efficiency (power saving) in the IDLE/INACTIVE state:   * Under the premise of idle state measurement, positioning report in the idle state can obtain 44.32% power saving gain compared to report in connected state. * Compared to positioning measurement and report all in the connected state, positioning measurement and report in the idle state can obtain at least 48.38% power saving gain. |

# Summary

In this contribution, we provide further intermediate updates on observations for NR positioning evaluation results as a part of RAN1 WG email discussion [103e-NR-ePos-02]. It is planned to discuss this document during GTW session #5 and update it further based on comments received for proposed observations.

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