
1 Scope

This specification describes the documents being produced by the 3GPP TSG RAN WG1 and first complete versions expected to be available by end of 1999. This specification describes the characteristics of the Layer 1 multiplexing and channel coding in the FDD mode of UTRA.

The 25.2 series specifies U_m point for the 3G mobile system. This series defines the minimum level of specifications required for basic connections in terms of mutual connectivity and compatibility.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- [1] 3GPP RAN TS 25.201: "Physical layer – General Description"
- [2] 3GPP RAN TS 25.211: "Transport channels and physical channels (FDD)"
- [3] 3GPP RAN TS 25.213: "Spreading and modulation (FDD)"
- [4] 3GPP RAN TS 25.214: "Physical layer procedures (FDD)"
- [5] 3GPP RAN TS 25.215: "Measurements (FDD)"
- [6] 3GPP RAN TS 25.221: "Transport channels and physical channels (TDD)"
- [7] 3GPP RAN TS 25.222: "Multiplexing and channel coding (TDD)"
- [8] 3GPP RAN TS 25.223: "Spreading and modulation (TDD)"
- [9] 3GPP RAN TS 25.224: "Physical layer procedures (TDD)"
- [10] 3GPP RAN TS 25.225: "Measurements (TDD)"
- [11] 3GPP RAN TS 25.302: "Services Provided by the Physical Layer"

4 Definitions, symbols and abbreviations

2.1 Definitions

For the purposes of the present document, the [following] terms and definitions [given in ... and the following] apply.

<defined term>: <definition>.

- TG*: Transmission Gap is consecutive empty slots that have been obtained with a transmission time reduction method. The transmission gap can be contained in one or two consecutive radio frames.
- TGL*: Transmission Gap Length is the number of consecutive empty slots that have been obtained with a transmission time reduction method. $0 \leq TGL \leq 14$
- TrCH number: Transport channel number represents a TrCH ID assigned to L1 by L2. Transport channels are multiplexed to the CCTrCH in the ascending order of these IDs.

FACH	Forward Access Channel
FDD	Frequency Division Duplex
FER	Frame Error Rate
GF	Galois Field
MAC	Medium Access Control
Mcps	Mega Chip Per Second
MS	Mobile Station
OVSF	Orthogonal Variable Spreading Factor (codes)
PCCC	Parallel Concatenated Convolutional Code
PCH	Paging Channel
PRACH	Physical Random Access Channel
PhCH	Physical Channel
QoS	Quality of Service
RACH	Random Access Channel
<u>RSC</u>	<u>Recursive Systematic Convolutional Coder</u>
RX	Receive
SCH	Synchronisation Channel
SF	Spreading Factor
SFN	System Frame Number
SIR	Signal-to-Interference Ratio
SNR	Signal to Noise Ratio
TF	Transport Format
TFC	Transport Format Combination
TFCI	Transport Format Combination Indicator
TPC	Transmit Power Control
TrCH	Transport Channel
TTI	Transmission Time Interval
TX	Transmit
UL	Uplink (Reverse link)

4.2.1 Error detection

Error detection is provided on transport blocks through a Cyclic Redundancy Check. The CRC is 24, 16, 12, 8 or 0 bits and it is signalled from higher layers what CRC length that should be used for each TrCH.

4.2.1.1 CRC Calculation

The entire transport block is used to calculate the CRC parity bits for each transport block. The parity bits are generated by one of the following cyclic generator polynomials:

$$g_{\text{CRC24}}(D) = D^{24} + D^{23} + D^6 + D^5 + D + 1$$

$$g_{\text{CRC16}}(D) = D^{16} + D^{12} + D^5 + 1$$

$$g_{\text{CRC12}}(D) = D^{12} + D^{11} + D^3 + D^2 + D + 1$$

$$g_{\text{CRC8}}(D) = D^8 + D^7 + D^4 + D^3 + D + 1$$

Denote the bits in a transport block delivered to layer 1 by $a_{im1}, a_{im2}, a_{im3}, \dots, a_{imA_i}$, and the parity bits by

$p_{im1}, p_{im2}, p_{im3}, \dots, p_{imL_i}$. A_i is the length of a transport block of TrCH i , m is the transport block number, and L_i is 24, 16, 12, 8, or 0 depending on what is signalled from higher layers.

The encoding is performed in a systematic form, which means that in GF(2), the polynomial

$a_{im1}D^{A_i+23} + a_{im2}D^{A_i+22} + \dots + a_{imA_i}D^{24} + p_{im1}D^{23} + p_{im2}D^{22} + \dots + p_{im23}D^1 + p_{im24}$
yields a remainder equal to 0 when divided by $g_{\text{CRC24}}(D)$, polynomial

$a_{im1}D^{A_i+15} + a_{im2}D^{A_i+14} + \dots + a_{imA_i}D^{16} + p_{im1}D^{15} + p_{im2}D^{14} + \dots + p_{im15}D^1 + p_{im16}$
yields a remainder equal to 0 when divided by $g_{\text{CRC16}}(D)$, polynomial

$a_{im1}D^{A_i+11} + a_{im2}D^{A_i+10} + \dots + a_{imA_i}D^{12} + p_{im1}D^{11} + p_{im2}D^{10} + \dots + p_{im11}D^1 + p_{im12}$
yields a remainder equal to 0 when divided by $g_{\text{CRC12}}(D)$ and polynomial

$a_{im1}D^{A_i+7} + a_{im2}D^{A_i+6} + \dots + a_{imA_i}D^8 + p_{im1}D^7 + p_{im2}D^6 + \dots + p_{im7}D^1 + p_{im8}$
yields a remainder equal to 0 when divided by $g_{\text{CRC8}}(D)$.

4.2.1.2 Relation between input and output of the Cyclic Redundancy Check

The bits after CRC attachment are denoted by $b_{im1}, b_{im2}, b_{im3}, \dots, b_{imB_i}$, where $B_i = A_i + L_i$. The relation between a_{imk} and b_{imk} is:

$$b_{imk} = a_{imk} \quad k = 1, 2, 3, \dots, A_i$$

$$b_{imk} = p_{im(L_i+1-(k-A_i))} \quad k = A_i + 1, A_i + 2, A_i + 3, \dots, A_i + L_i$$

4.2.2 Transport block concatenation and code block segmentation

All transport blocks in a TTI are serially concatenated. If the number of bits in a TTI is larger than Z_c , the maximum size of a code block in question, then code block segmentation is performed after the concatenation of the transport blocks. The maximum size of the code blocks depends on whether convolutional coding, turbo coding or no coding is used for the TrCH.

4.2.3 Channel coding

Code blocks are delivered to the channel coding block. They are denoted by $O_{ir1}, O_{ir2}, O_{ir3}, \dots, O_{irK_i}$, where i is the TrCH number, r is the code block number, and K_i is the number of bits in each code block. The number of code blocks on TrCH i is denoted by C_i . After encoding the bits are denoted by $y_{ir1}, y_{ir2}, y_{ir3}, \dots, y_{irY_i}$. The encoded blocks are serially multiplexed so that the block with lowest index r is output first from the channel coding block. The bits output are denoted by $c_{i1}, c_{i2}, c_{i3}, \dots, c_{iE_i}$, where i is the TrCH number and $E_i = C_i Y_i$. The output bits are defined by the following relations:

$$c_{ik} = y_{i1k} \quad k = 1, 2, \dots, Y_i$$

$$c_{ik} = y_{i,2,(k-Y_i)} \quad k = Y_i + 1, Y_i + 2, \dots, 2Y_i$$

$$c_{ik} = y_{i,3,(k-2Y_i)} \quad k = 2Y_i + 1, 2Y_i + 2, \dots, 3Y_i$$

...

$$c_{ik} = y_{i,C_i,(k-(C_i-1)Y_i)} \quad k = (C_i - 1)Y_i + 1, (C_i - 1)Y_i + 2, \dots, C_i Y_i$$

The relation between O_{irk} and y_{irk} and between K_i and Y_i is dependent on the channel coding scheme.

The following channel coding schemes can be applied to TrCHs:

- Convolutional coding
- Turbo coding
- No channel coding

The values of Y_i in connection with each coding scheme:

- Convolutional coding, 1/2 rate: $Y_i = 2 * K_i + 16$; 1/3 rate: $Y_i = 3 * K_i + 24$
- Turbo coding, 1/3 rate: $Y_i = 3 * K_i + 12$
- No channel coding, $Y_i = K_i$

Table 1: Error Correction Coding Parameters

Transport channel type	Coding scheme	Coding rate
BCH	Convolutional code	1/2
PCH		
FACH		1/3, 1/2 or no coding
RACH		
CPCH		
DCH	Turbo Code	1/3 or no coding
CPCH		
DCH		

<u>Transport channel type</u>	<u>Coding scheme</u>	<u>Coding rate</u>
<u>BCH</u>	<u>Convolutional code</u>	<u>1/2</u>
<u>PCH</u>		
<u>FACH</u>		
<u>RACH</u>		
<u>CPCH, DCH, DSCH</u>		<u>1/3, 1/2</u>
	<u>Turbo Code</u>	<u>1/3</u>
	<u>No coding</u>	

4.2.3.1 Convolutional coding

4.2.3.1.1 Convolutional coder

- Constraint length $K=9$. Coding rate $1/3$ and $1/2$.
- The configuration of the convolutional coder is presented in Figure 3.

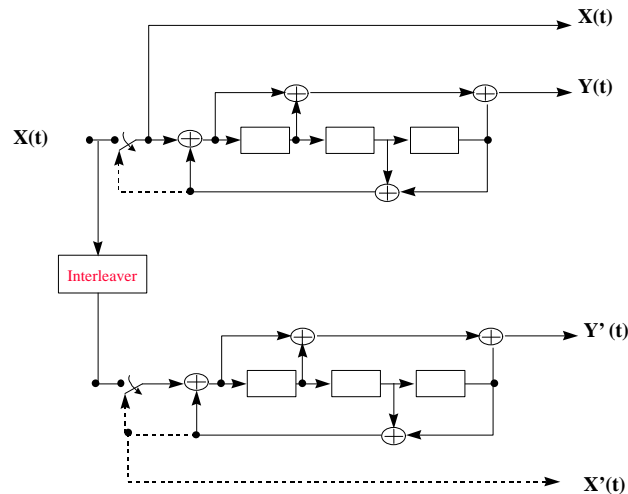


Figure 1: Structure of the 8 state PCCC encoder (dotted lines effective for trellis termination only)

The initial value of the shift registers of the PCCC encoder shall be all zeros.

The output of the PCCC encoder is punctured to produce coded bits corresponding to the desired code rate $1/3$. For rate $1/3$, none of the systematic or parity bits are punctured, and the output sequence is $X(0), Y(0), Y'(0),$

4.2.3.2.2 Trellis termination for Turbo coding

Trellis termination is performed by taking the tail bits from the shift register feedback after all information bits are encoded. Tail bits are added after the encoding of information bits.

The first three tail bits shall be used to terminate the first constituent encoder (upper switch of Figure 1 in lower position) while the second constituent encoder is disabled. The last three tail bits shall be used to terminate the second constituent encoder (lower switch of Figure 1 in lower position) while the first constituent encoder is disabled.

The transmitted bits for trellis termination shall then be

$$X(t) Y(t) X(t+1) Y(t+1) X(t+2) Y(t+2) X'(t) Y'(t) X'(t+1) Y'(t+1) X'(t+2) Y'(t+2).$$

4.2.3.2.3 Turbo code internal interleaver

Figure depicts the overall 8 state PCCC Turbo coding scheme including Turbo code internal interleaver. The Turbo code internal interleaver consists of mother interleaver generation and pruning. For arbitrary given block length K , one mother interleaver is selected from the 134 mother interleavers set. The generation scheme of mother interleaver is described in section 4.2.3.2.3.1. After the mother interleaver generation, l -bits are pruned in order to adjust the mother interleaver to the block length K . Tail bits T_1 and T_2 are added for constituent encoders RSC1 and RSC2, respectively. The definition of l is shown in section 4.2.3.2.3.2.

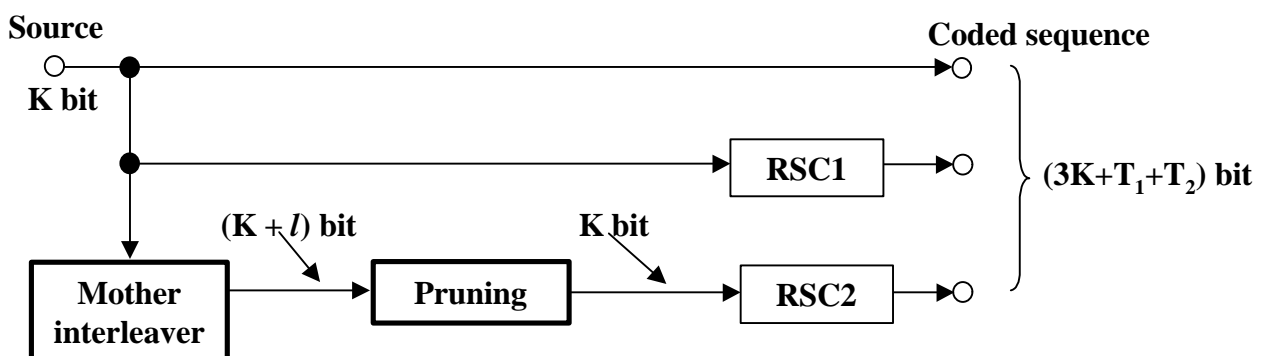


Figure 5: Overall 8 State PCCC Turbo Coding

4.2.3.2.3.1 Mother interleaver generation

The interleaving consists of three stages. In first stage, the input sequence is written into the rectangular matrix row by row. The second stage is intra-row permutation. The third stage is inter-row permutation. The three-stage permutations are described as follows, the input block length is assumed to be K (320 to 5114 bits).

First Stage:

(1) Determine the number of rows~~a row number~~ R such that

$$R=10 \text{ (} K = 481 \text{ to } 530 \text{ bits; Case-1)}$$

$$R=20 \text{ (} K = \text{any other block length except } 481 \text{ to } 530 \text{ bits; Case-2)}$$

(2) Determine the number of columns~~a column number~~ C such that

$$\text{Case-1; } C = p = 53$$

Case-2;

(i) find minimum prime p such that,

$$0 < (p+1) - K/R,$$

(ii) if $(0 < p - K/R)$ then go to (iii),

$$\text{else } C = p+1.$$

(iii) if $(0 < p-1 - K/R)$ then $C=p-1$,

$$\text{else } C = p.$$

(3) The input sequence of the interleaver is written into the $R \times C$ rectangular matrix row by row starting from row 0.

Second Stage:

A. If $C = p$

(A-1) Select a primitive root g_0 from table 2.

(A-2) Construct the base sequence $c(i)$ for intra-row permutation as:

$$c(i) = [g_0 \times c(i-1)] \bmod p, \quad i = 1, 2, \dots, (p-2), \quad c(0) = 1.$$

(A-3) Select the minimum prime integer set $\{q_j\}$ ($j=1, 2, \dots, R-1$) such that

$$\text{g.c.d}\{q_j, p-1\} = 1$$

$$q_j > 6$$

$$q_j > q_{(j-1)}$$

where g.c.d. is greatest common divider. And $q_0 = 1$.

(A-4) The set $\{q_j\}$ is permuted to make a new set $\{p_j\}$ such that

$$p_{P(j)} = q_j, \quad j = 0, 1, \dots, R-1,$$

where $P(j)$ is the inter-row permutation pattern defined in the third stage.

(A-5) Perform the j -th ($j = 0, 1, 2, \dots, R-1$) intra-row permutation as:

$$c_j(i) = c([i \times p_j] \bmod (p-1)), \quad i = 0, 1, 2, \dots, (p-2), \quad \text{and } c_j(p-1) = 0,$$

where $c_j(i)$ is the input bit position of i -th output after the permutation of j -th row.

B. If $C = p+1$

(B-1) Same as case A-1.

(B-2) Same as case A-2.

(B-3) Same as case A-3.

(B-4) Same as case A-4.

(B-5) Perform the j -th ($j = 0, 1, 2, \dots, R-1$) intra-row permutation as:

$$c_j(i) = c([i \times p_j] \bmod (p-1)), \quad i = 0, 1, 2, \dots, (p-2), \quad c_j(p-1) = 0, \text{ and } c_j(p) = p,$$

(B-6) If $(K = C \times R)$ then exchange $c_{R-1}(p)$ with $c_{R-1}(0)$.

where $c_j(i)$ is the input bit position of i -th output after the permutation of j -th row.

C. If $C = p-1$

(C-1) Same as case A-1.

(C-2) Same as case A-2.

(C-3) Same as case A-3.

(C-4) Same as case A-4.

(C-5) Perform the j -th ($j = 0, 1, 2, \dots, R-1$) intra-row permutation as:

$$c_j(i) = c([i \times p_j] \bmod (p-1)) - 1, \quad i = 0, 1, 2, \dots, (p-2),$$

where $c_j(i)$ is the input bit position of i -th output after the permutation of j -th row.

Third Stage:

(1) Perform the inter-row permutation based on the following $P(j)$ ($j=0, 1, \dots, R-1$) patterns, where $P(j)$ is the original row position of the j -th permuted row.

P_A : {19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 10, 8, 13, 17, 3, 1, 16, 6, 15, 11} for $R=20$

P_B : {19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 16, 13, 17, 15, 3, 1, 6, 11, 8, 10} for $R=20$

P_C : {9, 8, 7, 6, 5, 4, 3, 2, 1, 0} for $R=10$

The usage of these patterns is as follows:

Block length K : $P(j)$

320 to 480-bit: P_A

481 to 530-bit: P_C

531 to 2280-bit: P_A

2281 to 2480-bit: P_B

2481 to 3160-bit: P_A

3161 to 3210-bit: P_B

3211 to 5114-bit: P_A

(2) The output of the mother interleaver is the sequence read out column by column from the permuted $R \times C$ matrix starting from column 0.

Table 1: Table of prime p and associated primitive root

p	g _o	pP	g _o	p	g _o	pP	g _o	p	g _o
17	3	59	2	103	5	157	5	211	2
19	2	61	2	107	2	163	2	223	3
23	5	67	2	109	6	167	5	227	2
29	2	71	7	113	3	173	2	229	6
31	3	73	5	127	3	179	2	233	3
37	2	79	3	131	2	181	2	239	7
41	6	83	2	137	3	191	19	241	7
43	3	89	3	139	2	193	5	251	6
47	5	97	5	149	2	197	2	257	3
53	2	101	2	151	6	199	3		

4.2.3.2.3.2 Definition of number of pruning bits

The output of the mother interleaver is pruned by deleting the l -bits in order to adjust the mother interleaver to the block length K , where the deleted bits are non-existent bits in the input sequence. The pruning bits number l is defined as:

$$l = R \times C - K,$$

where R is the row number and C is the column number defined in section 4.1.3.2.3.1.

4.2.4 Radio frame size equalisation

Radio frame size equalisation is padding the input bit sequence in order to ensure that the output can be segmented in F_i data segments of same size as described in section 4.1.6. Radio frame size equalisation is only performed in the UL (DL rate matching output block length is always an integer multiple of F_i)

The input bit sequence to the radio frame size equalisation is denoted by $c_{i1}, c_{i2}, c_{i3}, \dots, c_{iE_i}$, where i is TrCH number and E_i the number of bits. The output bit sequence is denoted by $t_{i1}, t_{i2}, t_{i3}, \dots, t_{iT_i}$, where T_i is the number of bits. The output bit sequence is derived as follows:

$$t_{ik} = c_{ik}, \text{ for } k = 1 \dots E_i \text{ and}$$

$$t_{ik} = \{0 | 1\} \text{ for } k = E_i + 1 \dots T_i, \text{ if } E_i < T_i$$

where

$$T_i = F_i * N_i \text{ and}$$

$$N_i = \lfloor (E_i - 1) / F_i \rfloor + 1 \text{ is the number of bits per segment after size equalisation.}$$

4.2.5 1st interleaving

The 1st interleaving is a block interleaver with inter-column permutations. The input bit sequence to the 1st interleaver is denoted by $x_{i1}, x_{i2}, x_{i3}, \dots, x_{iX_i}$, where i is TrCH number and X_i the number of bits (at this stage X_i is assumed and guaranteed to be an integer multiple of TTI). The output bit sequence is derived as follows:

- (1) Select the number of columns C_i from table 3.
- (2) Determine the number of rows R_i defined as

$$R_i = X_i / C_i$$

- (3) Write the input bit sequence into the $R_l \times C_l$ rectangular matrix row by row starting with bit $x_{i,1}$ in the first column of the first row and ending with bit $x_{i,(R_l C_l)}$ in column C_l of row R_l :

$$\begin{bmatrix} x_{i1} & x_{i2} & x_{i3} & \cdots & x_{iC_l} \\ x_{i,(C_l+1)} & x_{i,(C_l+2)} & x_{i,(C_l+3)} & \cdots & x_{i,(2C_l)} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ x_{i,((R_l-1)C_l+1)} & x_{i,((R_l-1)C_l+2)} & x_{i,((R_l-1)C_l+3)} & \cdots & x_{i,(R_l C_l)} \end{bmatrix}$$

- (4) Perform the inter-column permutation based on the pattern $\{P_1(j)\}$ ($j=0,1, \dots, C-1$) shown in table 3, where $P_1(j)$ is the original column position of the j -th permuted column. After permutation of the columns, the bits are denoted by y_{ik} :

$$\begin{bmatrix} y_{i1} & y_{i,(R_l+1)} & y_{i,(2R_l+1)} & \cdots & y_{i,((C_l-1)R_l+1)} \\ y_{i2} & y_{i,(R_l+2)} & y_{i,(2R_l+2)} & \cdots & y_{i,((C_l-1)R_l+2)} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y_{iR_l} & y_{i,(2R_l)} & y_{i,(3R_l)} & \cdots & y_{i,(C_l R_l)} \end{bmatrix}$$

- (5) Read the output bit sequence $y_{i1}, y_{i2}, y_{i3}, \dots, y_{i,(C_l R_l)}$ of the 1st interleaving column by column from the inter-column permuted $R_l \times C_l$ matrix. Bit $y_{i,1}$ corresponds to the first row of the first column and bit $y_{i,(R_l C_l)}$ corresponds to row R_l of column C_l .

Table 3

TTI	Number of columns C_l	Inter-column permutation patterns
10 ms	1	{0}
20 ms	2	{0,1}
40 ms	4	{0,2,1,3}
80 ms	8	{0,4,2,6,1,5,3,7}

4.2.5.1 Relation between input and output of 1st interleaving in uplink

The bits input to the 1st interleaving are denoted by $t_{i1}, t_{i2}, t_{i3}, \dots, t_{iT_i}$, where i is the TrCH number and T_i the number of bits. Hence, $x_{ik} = t_{ik}$ and $X_i = T_i$.

The bits output from the 1st interleaving are denoted by $d_{i1}, d_{i2}, d_{i3}, \dots, d_{iT_i}$, and $d_{ik} = y_{ik}$.

4.2.5.2 Relation between input and output of 1st interleaving in downlink

If fixed positions of the TrCHs in a radio frame is used then the bits input to the 1st interleaving are denoted by $h_{i1}, h_{i2}, h_{i3}, \dots, h_{i(F_i H_i)}$, where i is the TrCH number. Hence, $x_{ik} = h_{ik}$ and $X_i = F_i H_i$.

If flexible positions of the TrCHs in a radio frame is used then the bits input to the 1st interleaving are denoted by $g_{i1}, g_{i2}, g_{i3}, \dots, g_{iG_i}$, where i is the TrCH number. Hence, $x_{ik} = g_{ik}$ and $X_i = G_i$.

The bits output from the 1st interleaving are denoted by $q_{i1}, q_{i2}, q_{i3}, \dots, q_{iQ_i}$, where i is the TrCH number and Q_i is the number of bits. Hence, $q_{ik} = y_{ik}$, $Q_i = F_i H_i$ if fixed positions are used, and $Q_i = G_i$ if flexible positions are used.

4.2.6 Radio frame segmentation

When the transmission time interval is longer than 10 ms, the input bit sequence is segmented and mapped onto consecutive radio frames. Following rate matching in the DL and radio frame size equalisation in the UL the input bit sequence length is guaranteed to be an integer multiple of F_i .

The input bit sequence is denoted by $x_{i1}, x_{i2}, x_{i3}, \dots, x_{iX_i}$ where i is the TrCH number and X_i is the number bits. The F_i output bit sequences per TTI are denoted by $y_{i,n_1}, y_{i,n_2}, y_{i,n_3}, \dots, y_{i,n_{Y_i}}$ where n_i is the radio frame number in current TTI and Y_i is the number of bits per radio frame for TrCH i . The output sequences are defined as follows:

$$y_{i,n,k} = x_{i,((n-1)Y_i)+k}, n_i = 1 \dots F_i, \underline{j}k = 1 \dots Y_i$$

where

$Y_i = (X_i / F_i)$ is the number of bits per segment,

x_{ik} is the k^{th} bit of the input bit sequence and

$y_{i,n,k}$ is the k^{th} bit of the output bit sequence corresponding to the n^{th} radio frame

The n_i -th segment is mapped to the n_i -th radio frame of the transmission time interval.

4.2.6.1 Relation between input and output of the radio frame segmentation block in uplink

The input bit sequence to the radio frame segmentation is denoted by $d_{i1}, d_{i2}, d_{i3}, \dots, d_{iT_i}$, where i is the TrCH number and T_i the number of bits. Hence, $x_{ik} = d_{ik}$ and $X_i = T_i$.

The output bit sequence corresponding radio frame n_i is denoted by $e_{i1}, e_{i2}, e_{i3}, \dots, e_{iN_i}$, where i is the TrCH number and N_i is the number of bits. Hence, $e_{i,k} = y_{i,n,k}$ and $N_i = Y_i$.

4.2.6.2 Relation between input and output of the radio frame segmentation block in downlink

The bits input to the radio frame segmentation are denoted by $q_{i1}, q_{i2}, q_{i3}, \dots, q_{iQ_i}$, where i is the TrCH number and Q_i the number of bits. Hence, $x_{ik} = q_{ik}$ and $X_i = Q_i$.

The output bit sequence corresponding to radio frame n_i is denoted by $f_{i1}, f_{i2}, f_{i3}, \dots, f_{iV_i}$, where i is the TrCH number and V_i is the number of bits. Hence, $f_{i,k} = y_{i,n,k}$ and $V_i = Y_i$.

4.2.7 Rate matching

Rate matching means that bits on a transport channel are repeated or punctured. Higher layers assign a rate-matching attribute for each transport channel. This attribute is semi-static and can only be changed through higher layer signalling. The rate-matching attribute is used when the number of bits to be repeated or punctured is calculated.

The number of bits on a transport channel can vary between different transmission time intervals. In the downlink the transmission is interrupted if the number of bits is lower than maximum. When the number of bits between different transmission time intervals in uplink is changed, bits are repeated or punctured to ensure that the total bit rate after second multiplexing is identical to the total channel bit rate of the allocated dedicated physical channels.

Notation used in section 4.2.7 and subsections:

multiplexing are denoted by $s_1, s_2, s_3, \dots, s_S$, where S is the number of bits, i.e. $S = \sum_i V_i$. The TrCH multiplexing is defined by the following relations:

$$s_k = f_{1k} \quad k = 1, 2, \dots, V_1$$

$$s_k = f_{2,(k-V_1)} \quad k = V_1+1, V_1+2, \dots, V_1+V_2$$

$$s_k = f_{3,(k-(V_1+V_2))} \quad k = (V_1+V_2)+1, (V_1+V_2)+2, \dots, (V_1+V_2)+V_3$$

...

$$s_k = f_{I,(k-(V_1+V_2+\dots+V_{I-1}))} \quad k = (V_1+V_2+\dots+V_{I-1})+1, (V_1+V_2+\dots+V_{I-1})+2, \dots, (V_1+V_2+\dots+V_{I-1})+V_I$$

4.2.9 Insertion of discontinuous transmission (DTX) indication bits

In the downlink, DTX is used to fill up the radio frame with bits. The insertion point of DTX indication bits depends on whether fixed or flexible positions of the TrCHs in the radio frame are used. It is up to the UTRAN to decide for each CCTrCH whether fixed or flexible positions are used during the connection. DTX indication bits only indicate when the transmission should be turned off, they are not transmitted.

4.2.9.1 Insertion of DTX indication bits with fixed positions

This step of inserting DTX indication bits is used only if the positions of the TrCHs in the radio frame are fixed. With fixed position scheme a fixed number of bits is reserved for each TrCH in the radio frame.

The bits from rate matching are denoted by $g_{i1}, g_{i2}, g_{i3}, \dots, g_{iG_i}$, where G_i is the number of bits in one TTI of TrCH i . Denote the number of bits reserved for one radio frame of TrCH i by H_i , i.e. the maximum number of bits in a radio frame for any transport format of TrCH i . The number of radio frames in a TTI of TrCH i is denoted by F_i . The bits output from the DTX insertion are denoted by $h_{i1}, h_{i2}, h_{i3}, \dots, h_{i(F_i H_i)}$. Note that these bits are three valued. They are defined by the following relations:

$$h_{ik} = g_{ik} \quad k = 1, 2, 3, \dots, G_i$$

$$h_{ik} = \mathbf{d} \quad k = G_i+1, G_i+2, G_i+3, \dots, F_i H_i$$

where DTX indication bits are denoted by \mathbf{d} . Here $g_{ik} \in \{0, 1\}$ and $\mathbf{d} \notin \{0, 1\}$.

4.2.9.2 Insertion of DTX indication bits with flexible positions

~~NOTE: Below, it is assumed that all physical channels belonging to the same CCTrCH use the same SF. Hence, $U_p = U = \text{constant}$.~~

This step of inserting DTX indication bits is used only if the positions of the TrCHs in the radio frame are flexible. The DTX indication bits shall be placed at the end of the radio frame. Note that the DTX will be distributed over all slots after 2nd interleaving.

The bits input to the DTX insertion block are denoted by $s_1, s_2, s_3, \dots, s_S$, where S is the number of bits from TrCH multiplexing. The number of PhCHs is denoted by P and the number of bits in one radio frame, including DTX indication bits, for each PhCH by U .

The bits output from the DTX insertion block are denoted by $w_1, w_2, w_3, \dots, w_{(PU)}$. Note that these bits are threevalued. They are defined by the following relations:

$$w_k = s_k \quad k = 1, 2, 3, \dots, S$$

$$w_k = \mathbf{d} \quad k = S+1, S+2, S+3, \dots, PU$$

where DTX indication bits are denoted by \mathbf{d} . Here $s_k \in \{0,1\}$ and $\mathbf{d} \notin \{0,1\}$.

4.2.10 Physical channel segmentation

~~NOTE: Below, it is assumed that all physical channels belonging to the same CCTrCH use the same SF. Hence, $U_p = U = \text{constant}$.~~

When more than one PhCH is used, physical channel segmentation divides the bits among the different PhCHs. The bits input to the physical channel segmentation are denoted by $x_1, x_2, x_3, \dots, x_Y$, where Y is the number of bits input to the physical channel segmentation block. The number of PhCHs is denoted by P .

The bits after physical channel segmentation are denoted $u_{p1}, u_{p2}, u_{p3}, \dots, u_{pU}$, where p is PhCH number and U is

the number of bits in one radio frame for each PhCH, i.e. $U = \frac{Y}{P}$. The relation between x_k and u_{pk} is given below.

Bits on first PhCH after physical channel segmentation:

$$u_{1k} = x_k \quad k = 1, 2, \dots, U$$

Bits on second PhCH after physical channel segmentation:

$$u_{2k} = x_{(k+U)} \quad k = 1, 2, \dots, U$$

...

Bits on the P^{th} PhCH after physical channel segmentation:

$$u_{Pk} = x_{(k+(P-1)U)} \quad k = 1, 2, \dots, U$$

4.2.10.1 Relation between input and output of the physical segmentation block in uplink

The bits input to the physical segmentation are denoted by $s_1, s_2, s_3, \dots, s_S$. Hence, $x_k = s_k$ and $Y = S$.

4.2.10.2 Relation between input and output of the physical segmentation block in downlink

If fixed positions of the TrCHs in a radio frame are used then the bits input to the physical segmentation are denoted by $s_1, s_2, s_3, \dots, s_S$. Hence, $x_k = s_k$ and $Y = S$.

If flexible positions of the TrCHs in a radio frame are used then the bits input to the physical segmentation are denoted by $w_1, w_2, w_3, \dots, w_{(PU)}$. Hence, $x_k = w_k$ and $Y = PU$.

4.2.11 2nd interleaving

The 2nd interleaving is a block interleaver with inter-column permutations. The bits input to the 2nd interleaver are denoted $u_{p1}, u_{p2}, u_{p3}, \dots, u_{pU}$, where p is PhCH number and U is the number of bits in one radio frame for one PhCH.

(1) Set the number of columns $C_2 = 30$. The columns are numbered 0, 1, 2, ..., C_2-1 from left to right.