Agenda Item:

Source: **Nokia**

Title: **Text proposal for uplink long scrambling codes (2 Gold Codes)**

Document for: **Discussion**

4.3.2.2   Long scrambling code

The long scrambling codes are formed as described in section 4.3.2, where c_1 and c_2 are constructed as the position wise modulo 2 sum of 40960 chip segments of two binary m-sequences generated by means of two generator polynomials of degree 25. The resulting sequences thus constitute segments of a set of Gold sequences. The code c_1 is used in generating the in phase component of the complex spreading code and the code c_2 is used in generating the quadrature component.The uplink scrambling code word has a period of one radio frame of 10 ms.

Let A be an m-sequence generated by the polynomial $X^{25} + X^3 + 1$ and let B be that one by $X^{25} + X^3 + X^2 + X + 1$ over GF(2) with the same initial conditions: $A(0) = B(0) = 1$ and $A(i) = B(i) = 0$ for $i = 1, 2, ... , 24$. Then the sequences A and B satisfy the following recurrence relations:

$A(i + 25) = A(i + 3) + A(i)$ modulo 2, $i = 0, 1, 2, ... , 2^{25} – 27$ and
$B(i + 25) = B(i + 3) + B(i + 2) + B(i + 1) + B(i)$ modulo 2, $i = 0, 1, 2, ... , 2^{25} – 27$.

The long scrambling code parametrization is one dimensional, denoted by m, the parameter m runs thru pairs of Gold codes and takes integral values from 0 to $2^{24} – 2 = 16\ 777\ 214$. The in phase component, $c_{1, m}$, and the quadrature component, $c_{2, m}$, for the *m:th* long scrambling code word are given by

$c_{1, m}(k) = A(k + 2*m) \oplus B(k + 11184803)$ and
$c_{2, m}(k) = A(k + 1 + 2*m) \oplus B(k + 11184803)$,

where k is a chip index, $k = 0, 1, 2, ... , 40960 – 1$, and the symbol $\oplus$ stands for modulo 2 addition. The lowest chip index corresponds to the chip scrambled first in each radio frame. These binary code words are converted to real valued sequences by the transformation '0' -> '+1', '1' -> '-1'.

<Editor's note: this parametrization works for all chip rates, however, the value 40960 is based on assumption of a 4.096Mcps chip rate.>
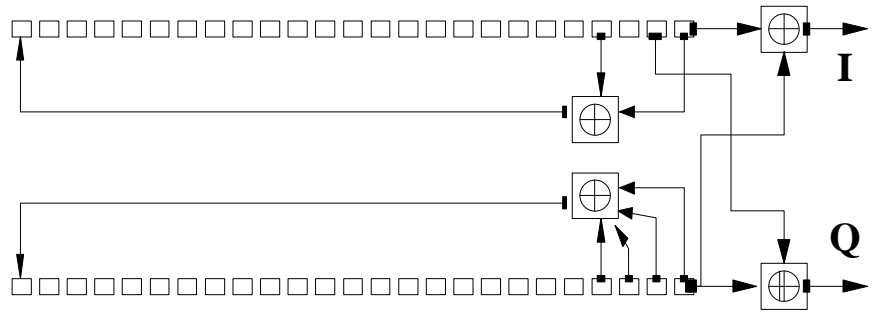
Figure 1.   Configuration of uplink scrambling code generator (This is only an example, there are other possibilities as well.)