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Title: Variable Step Size for Power Over-Shot Protection Based on Sequential Analysis of Power Control Bits

Source: Nortel Networks[1]

Document for: Discussion

0.0 Summary

In this contribution, we present the variable step size power control algorithm in UE and or BTS to protect the transmit power over-shoot caused by current power control rule. To reduce the power over-shoot will result in a reduced power control error standard deviation of a particular connection, hence to improve the performance of this specific link, it will also reduce the over all cell interference cause by all the other users.

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0.1 Introduction.

In the current 3GPP system, closed loop power control mechanisms is employed to equalize the power of UE signals (transmitted at different distances from BTS) at BTS input and to compensate fast power deviations from the nominal level caused by the impact of Rayleigh fading. Especially the fast closed loop power control can be very effective for the slow fading environment.

However, due to the fixed power control step size and power control command transmission delay, an transmit power over-shooting during the deep fade is experienced. This phenomenon, described in section 0.2 corresponds to an un-necessary increase of power over shoot at the end of deep fades period, which increases the interference to other users and adversely impact the overall capacity of the system. In section 0.3, we introduce an enhancement of the presently described power control algorithm, which allows the transmitter side selects the power control step size based on a sequential analysis of the power control commands received. Such algorithm can be applied at the UE and at the BTS. Section 0.4 provides a performance evaluation of the proposed scheme, in terms of standard deviation of difference between the target SIR and the experienced one.

0.2 Power Over-Shooting Phenomenon of 3GPP Power Control

Due the fixed power control step size and fixed power control command transmission delay, when UE experiences of deep fades, the BTS sends consecutive power increasing commands to UE and UE increases the transmit power continuously in order the compensate the deep fading. However, once the deep fade period is finish, due to the delay of power control command and the closed loop feedback power control mechanism, the UE continues to increase the transmit power, and this will cause the power over shot after the deep fade (see Figure 1). Such an power over-shooting has two negative impacts to the uplink/downlink power control performance:

- it will increase the standard deviation of power control error for the particular UE;
- it will increase the over all interference of the cell.

It can be observed that the power over-shooting can be as high as 4 dB. Furthermore, such a power over-shooting occurs at all fading frequencies. The aim of this proposal is to develop a certain rule to reduce or eliminate the un-necessary power over shooting caused by the current 3GPP power control algorithm.

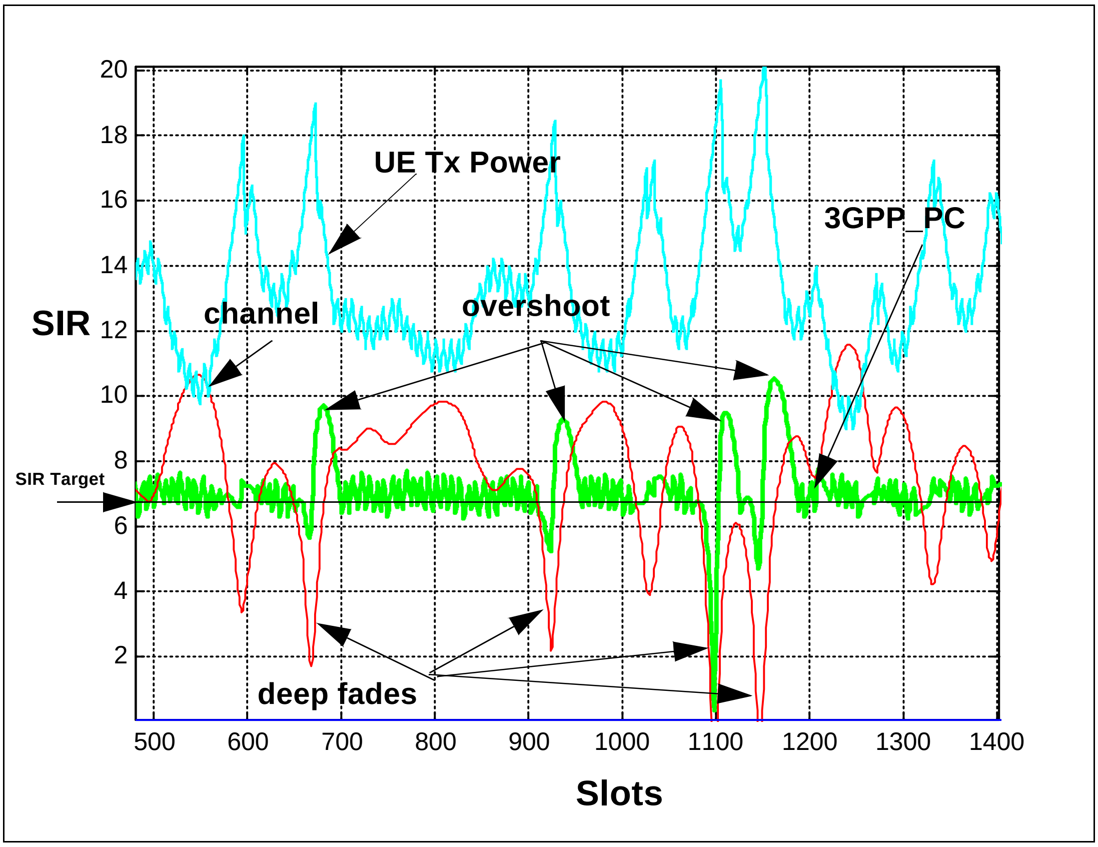
0.3 PCB Sequential Analysis and Variable Step Size Power Control

0.3.1 Description of the Scheme

The current 3GPP power control algorithm is essentially a one-bit memoryless power control. We propose to apply addition rule on the power control bit stream pattern, i.e. to perform the sequential statistical analysis on the power control bits at UE. When the power control bit stream matches a certain pattern, we use different power control rule and step size. *In general, this concept can be also applied to meet other specific power control requirements*. In this proposal, we focus to use this concept to reduce the power overshooting at UE.

The proposed power control algorithm only modifies the power step size determination block in the transmitter side. Figure 2 illustrates the case of the uplink power control, where the transmitter is the UE and the receiver the BTS.

FIGURE 1. .3GPP Closed Loop Power Control Algorithm



0.3.2 Detailed Algorithm

The sequential analysis of power control bits and the variable power control step size rule are as follows:

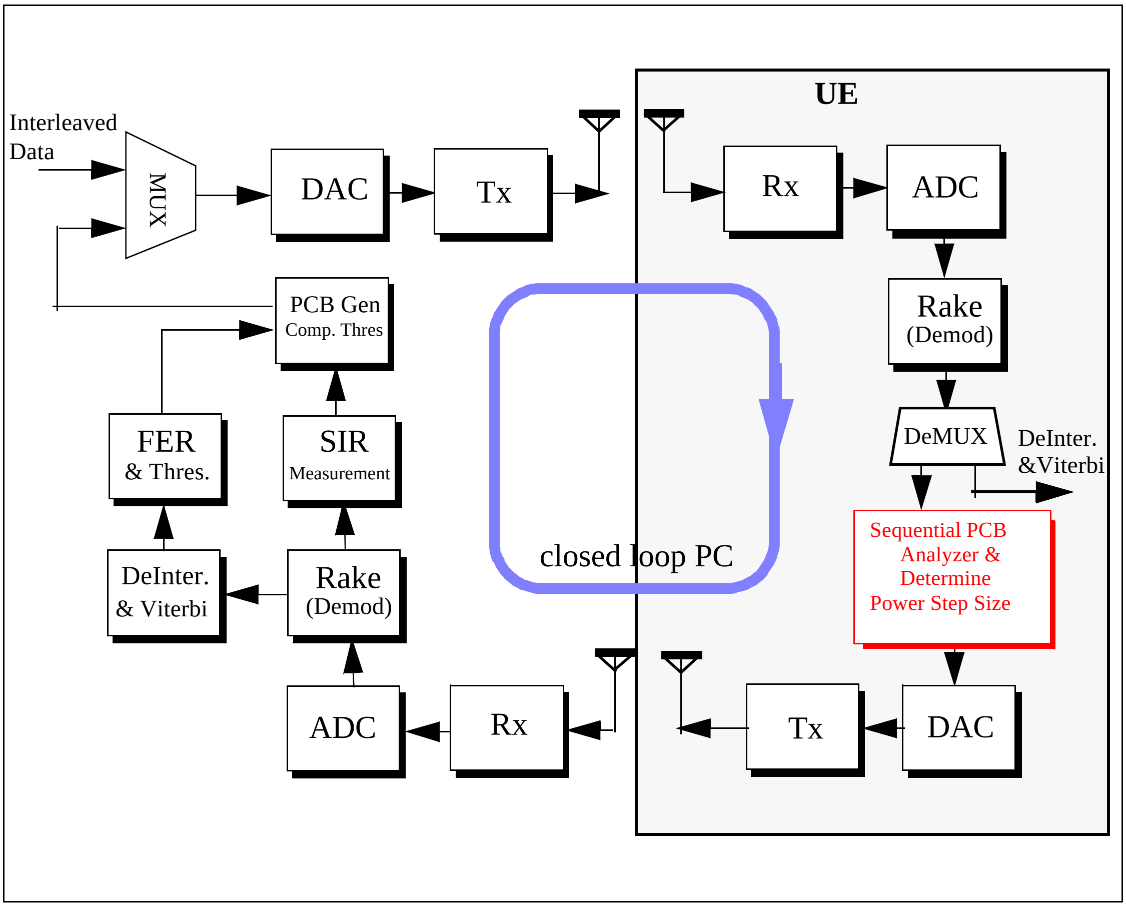
1. Unless otherwise stated, the transmitter applies the normal power control step $\Delta 1$ such that when it receives a TPC=0, then the power is decreased by $\Delta 1$ and when it receives a TPC=1 then the power is increase by $\Delta 1$. This is the presently described algorithm in 25.214.
2. In addition, the transmitter considers the last X received TPC commands.

If Y TPC commands among these X commands, including the last received one (not yet applied), correspond to TPC=1, then

The power step size is change to $\Delta 2$

3. If a transition between TPC=1 and TPC=0 is detected then the power is decreased by the power control step $\Delta 3$ in the next consecutive Z slots, irrespective to the power control command received.
4. Rest the control step to $\Delta 1$ again and resume the normal power control operation in Step 1.

FIGURE 2. Proposed Variable Step Size Closed Loop Power Control Algorithm



0.3.3 Example of Parameters for the Proposed Scheme and Rationale

A particular example of the parameters set, which we used in the simulation, is the following:

$\Delta 1 = 1dB$, $\Delta 2 = 1dB$, $\Delta 3 = 2dB$, X=10, Y=9, Z=1.

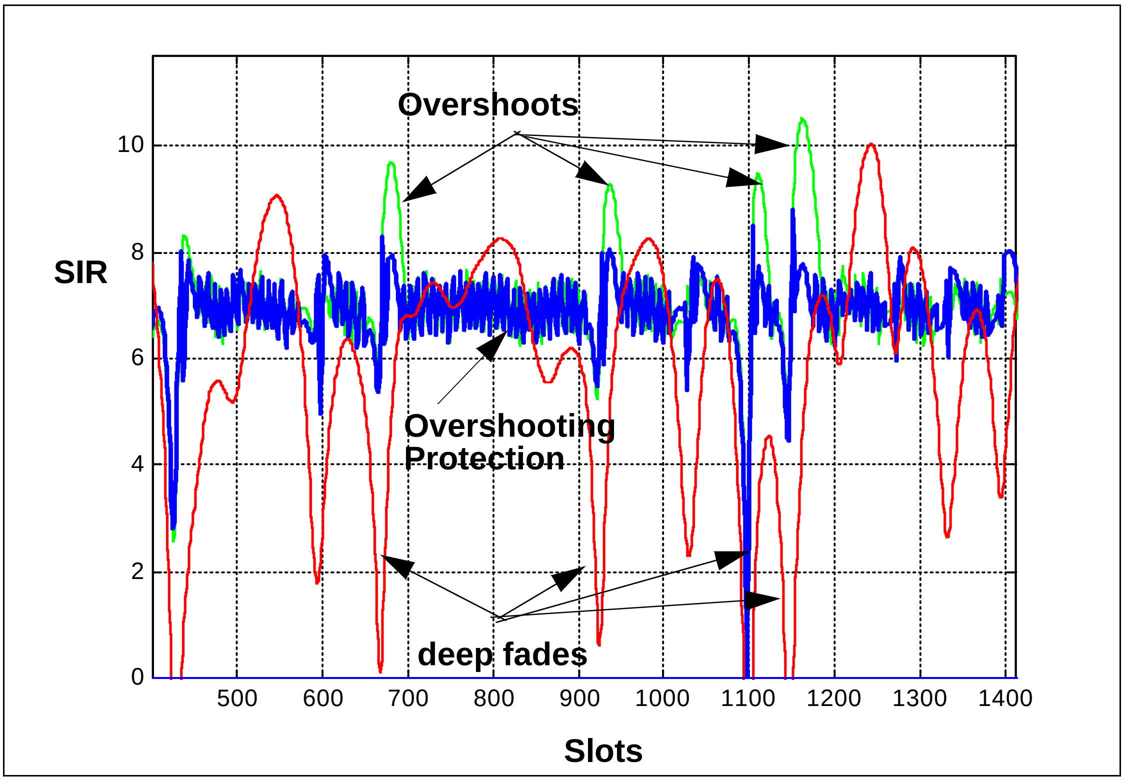
The objective with those parameters and the scheme is as follows

- When the transmitter observes consecutive commands asking for a power increase, then it is highly probably that a deep fade is experienced. In such a case, larger power control step size for a short period of time should track the fast power change.
- Then as soon as there is an inversion of the command (request to decrease the power) this indicates that the deep fade finished. However due to the power control delay, it means that the deep fade finished one (a few) slot periods ago, in which case the power should be decreased by an even larger step.
- The “majority” vote (the analysis of Y out of X command) is used to take into account TPC errors.

0.3.4 Illustrative Behaviour of the Proposed Power Control Algorithm and Gain

The effectiveness of the proposed power control algorithm to reduce the power overshooting is depicted is Figure 3.

FIGURE 3. Closed Loop PC with PCB Analyser and Variable Step Size



It can be seen that the by using the sliding window detection of the consecutive power increase command stream, we can use a variable step size to suppress the power overshooting, after the deep fades period even in the presence of TPC command error. Such a power over shooting protection can be extended to other cases where the disrupt power changes occur at the receiver input.

0.3.5 Impact on the Proposed Scheme

The proposed scheme can be applied for the uplink and the downlink.

The application of the scheme for the downlink power control is left to the manufacturer since the reaction of the BTS to uplink TPC commands is outside the scope of the specifications. It does not have any impact on the UE since it impact only the transmitter.

The application of the scheme for the uplink should be made mandatory. The set of power control steps to apply in each of the phases $\Delta 1$, $\Delta 2$, $\Delta 3$ are parametrizable by the BTS, and can be provided to the UE at call set-up or together with outer loop power control parameters. The additional complexity to the UE is very small, since it only requires an additional memory of X-1 command bits.

0.4 Performance Evaluation of Proposed Power Control Algorithm

0.4.1 Simulation Assumptions

- Output of the Simulator

Our simulation investigates the Standard deviation of the SIR error, where the SIR error is the difference between the target SIR as set by the outer loop power control and the experienced SIR.

- Power control delay

One slot power control delay was taken into account in the assimilations.

- Propagation model

A one-path Rayleigh fading was considered as a first case to look at.

- Power control algorithms simulated

Three cases: (1) 3GPP power control (2) Proposed power control with 1 slot TPC delay.

- Power control Parameters

For our proposed scheme the parameters are as follows:

$\Delta 1 = 1dB$, $\Delta 2 = 1dB$, $\Delta 3 = 2dB$, X=10, Y=9, Z=1.

For the 3GPP algorithm, 1 dB power control step is used.

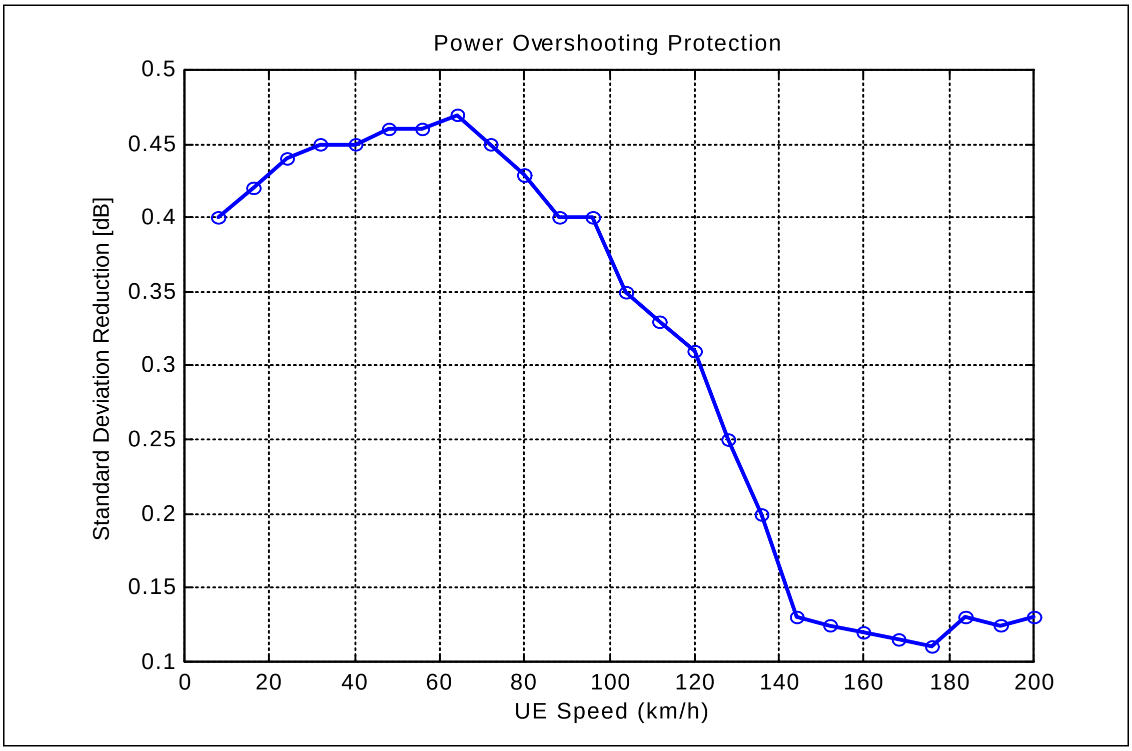
- TPC errors modelling

Uniform 4% TPC error rate.

0.4.2 Simulation Results

The gain of the proposed power control algorithm and the 3GPP power control in terms of the standard deviation of power control error is shown in Figure 4.

FIGURE 4. Power Control Error Reduction for 3GPP and Proposed Power Control



As we can see the for a wide range of the UE speed, the proposed power control can achieve about 0.4 dB gain in the power control error standard deviation. Such a gain can also be translated into the overall cell interference reduction. Additionally the application of the scheme on the uplink leads to a UE transmit power reduction thus the result in battery saving. Note that to implement such UE power over-shooting reduction does not need any modification of the BTS operation.

0.5 Conclusions

We present a power control algorithm, which exploit the sequential analysis of TPC commands stream and using a variable control steps to overcome the power over-shooting for the 3GPP closed loop power control. The proposed algorithm can be implemented in both downlink and uplink, to reduce the overall cell interference and improve link performance. In particular, in the uplink the overshooting suppression can save the UE battery. The impact of the proposed scheme is minimum. No additional signalling is required.