TSG-RAN Working Group1 meeting #4
Yokohama 19-20, April 1999

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Agenda Item	**:**	Adhoc 3 /RACH
Source	**:**	Nokia
Title	**:**	UTRA/FDD RACH timing proposal
Document for	**:**	Discussion / decision

Summary:

In this document, a new timing is proposed for RACH transmission.

1. INTRODUCTION

In the last TSG RAN WG1 meeting the RACH timing was discussed in Adhoc 3, but not any exact values were yet decided for timing requirements.

If the time from the beginning of the preamble to the beginning of the message is defined to be 2 access slots, it means that the total processing time to be divided between BS and UE is only 0.5 ms – 2* T_p, where T_p is the propagation delay. Our opinion is that this is a too tight requirement, especially if we want to do channel estimation from PCCPCH at the UE for decoding AICH.

For that reason we propose that the timing requirement is relaxed somewhat to get more processing time for both BS and UE.

2. RACH TIMING PROPOSAL

Figure 1 shows the proposal of RACH timing. It proposes that downlink frame timing is delayed by 0.5 ms compared to uplink frame timing. Thus T_o=0.5 ms.

It is further proposed that BS transmits AICH at the beginning of the next access slot in downlink, which means that the processing time for BS will be T_{BS} = 0.75 ms – T_p, where T_p is the propagation delay. Likewise, it is proposed that UE transmits the message (or the next preamble) at the beginning of the next access slot in uplink, which means that the processing time for UE will be T_{UE} = 1 ms - T_p, where T_p is again the propagation delay. Also, it is proposed the downlink access slots are synchronised with PCCPCH time slots, in order to make sure that the channel estimation using PCCPCH pilots for decoding AICH is optimised.

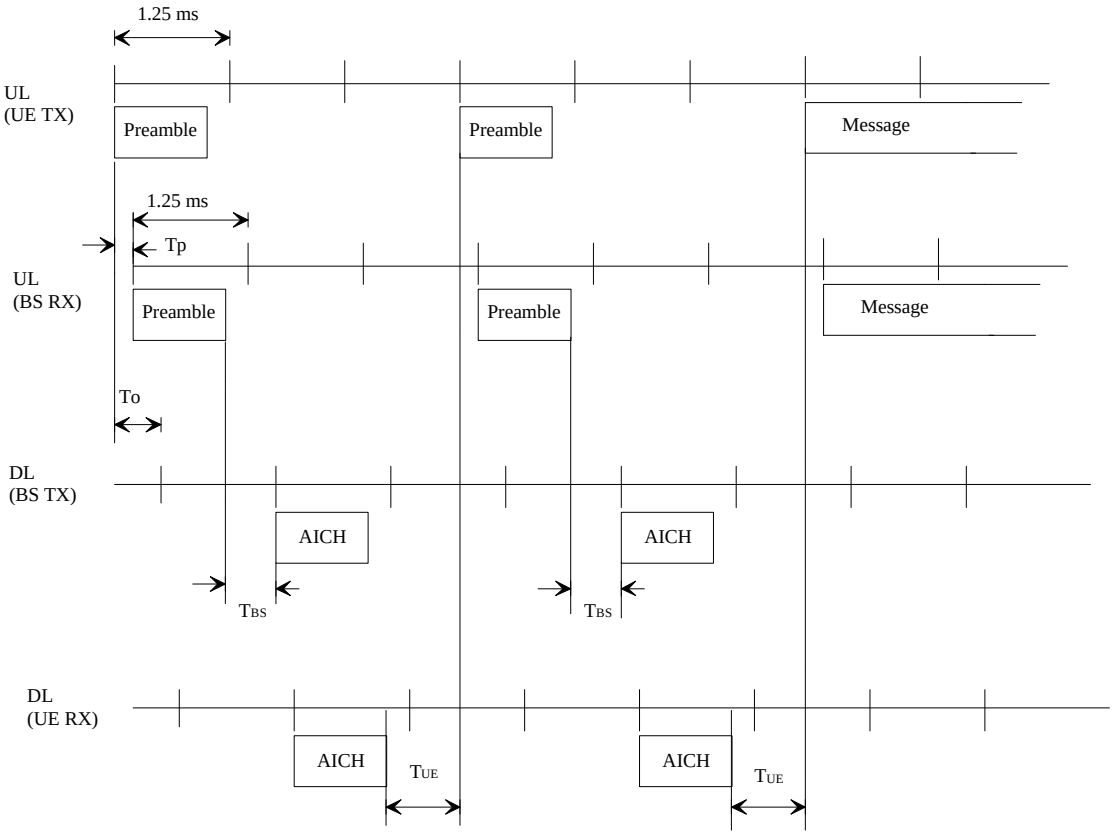

Figure 1. RACH timing proposal.

3. CONCLUSION

We propose that the new RACH timing as described above is adopted for the UTRA/FDD random-access scheme. With this kind of scheme the idle period between preamble and message is still such a small value, 2.75 ms, that it should allow the fast power ramping process to work efficiciently. And what is very important, it allows enough processing time for both BS and UE.

Together with the scheme it is proposed that downlink access slots are synchronised with PCCPCH time slots, in order to make sure that the channel estimation using PCCPCH pilots for decoding AICH is optimised.