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Yokohama 22-25, February 1999

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Agenda Item: 4

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Title: Hardware Complexity Evaluation of Turbo-MIL

Document for:

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1. Introduction

We proposed Multi-stage Interleaver (MIL) for Turbo code in ARIB and ETSI [1]. MIL general description for 8-state (K = 4) Turbo code and DSP implementation complexity were described in ETSI document [2]. In this document, the hardware complexity of Turbo-MIL is evaluated from the power-consumption point of view and the power-consumption of Turbo-MIL is shown as the relative values to the power-consumption of whole Turbo-decoder. In Turbo-interleaver selection, it is important that such hardware complexity evaluation is done to take the ratio of Turbo-interleaver complexity to whole Turbo-decoder complexity or terminal complexity into account and it is important to take the flexibility of Turbo-interleaver into account as well.

2. Power consumption evaluation

(1) Lower complexity Turbo-MIL and its power consumption

In order to reduce the hardware complexity and power consumption, the following variety schemes (*a*) and (*b*) could be adopted for Turbo-MIL without performance degradation:

(*a*) Repetition and puncturing scheme is introduced by small number l (l < 8 bits) as shown in Fig. 1. The required bits for Turbo-interleaver are then set to only $K + l = 0$ (mod 8). The pruning process, which is done just before output of interleaver patterns, according to a result of comparing with "Total_bit"[3] could be deleted from the original Turbo-MIL [2].

(*b*) The pruning process, which is done after an addition for two RAM outputs, according to a result of comparing with "M1"[3] is deleted from the original Turbo-MIL [2] and the inserting process using a decrement counter instead of the pruning process. Here, from this variation, required maximum clock frequency could be reduced to be approximately the half.

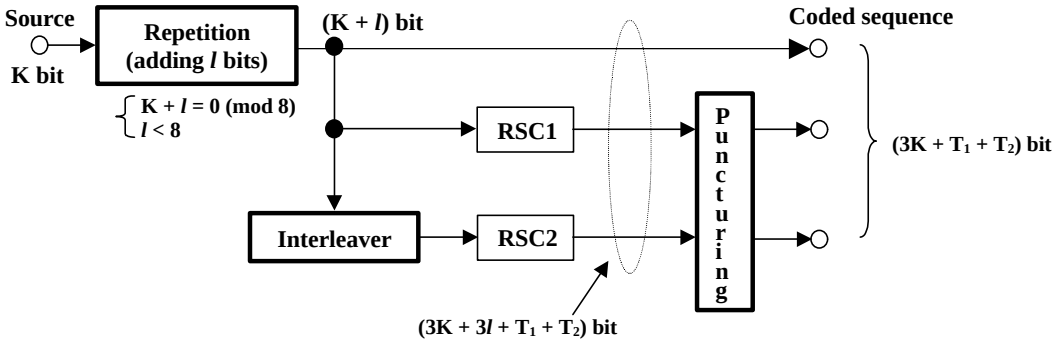


Fig. 1 Flexible Turbo-coder with bit repetition and puncturing

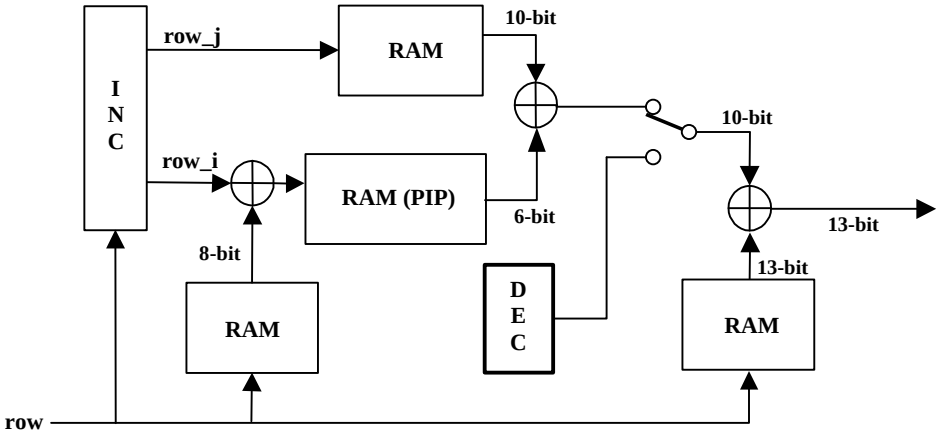


Fig. 2 Low complexity Turbo-MIL without pruning process

Table 1 shows the estimation results of relative power consumption for original Turbo-MIL and the low complexity Turbo-MIL (Fig. 2) i.e. adopted the above variations: (*a*) and (*b*). From these results, when the low complexity Turbo-MIL is applied, it need about 10 % (3 %) power consumption compared to that of total Turbo-decoder in case of the 640-bit (5120-bit) inteleaver length. Furthermore, these percentages are reduced when the power consumption of the interleaver is compared to the total power consumption of the mobile terminal. It power consumption can be estimated less than a few percentage of the total power consumption of the mobile terminal.

Table 1 Relative power consumption of MIL (for 8-state Turbo-code)

	Turbo decoder without interleaver	Original Turbo-MIL (MIL)		Low complexity Turbo-MIL (MIL2)	
		640 bit	5120 bit	640 bit	5120 bit
Relative power consumption	1.00	0.23	0.06	0.12	0.03

(2) Hamming weight asymptote and BER performance

Channel coding of IMT2000 is required a flexibility to the size of frame which should be changed according to the service. The minimum range of frame size is 320 to 8192 bits (there is possibility of enlarging the range of frame size). So, in such frame size range, turbo-interleaver is also required to provide good performance or low error-floor capability. Therefore, we evaluated the error-floor performance for the low complexity Turbo-MIL by using "Hamming Weight Asymptote"(HWA).

Fig. 3 shows HWA comparisons of Turbo codes using original Turbo-MIL (MIL) and the low complexity Turbo-MIL (MIL2). It can been seen that HWA of MIL2 was less than HWA of MIL on the average throughout the whole bit size range. For further performance investigation of MIL2, the simulated BER and FER performance are shown in Fig. 4. It can be found that MIL2 has the good performance as the original MIL.

3. Conclusion

In this document, power consumption of MIL was evaluated and it was estimated to be less than a few percentage of the total power consumption of the mobile terminal. In addition to this, MIL has a high flexibility to the frame size variation, i.e., it has a good performance for any interleaver sizes larger than 256 bits.

References

[1] "Multi-stage interleaving (MIL) method for Turbo codes", NTT DoCoMo, Tdoc SMG2 UMTS-L1 273/98
[2] "Description of Multi-stage InterLeaver (MIL) for 8-state turbo codes", NTT DoCoMo, Tdoc SMG2 UMTS L1 027/99
[3] "Hardware implementation and performance of MIL for Turbo-code", NTT DoCoMo, Tdoc SMG2 UMTS-L1 028/99
[4] "A Study on Turbo-inteleaver Flexibility", NTT DoCoMo, TSGR1#2(99)xxx

(Documents[1]-[3] are ETSI input documents and also these documents have been distributed to 3GPP_TSG_RAN_WG1 reflector for reference.)

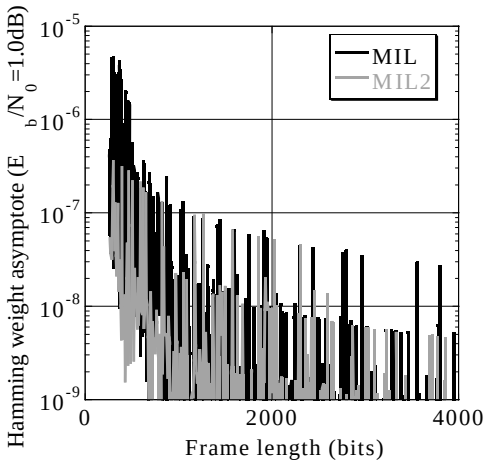
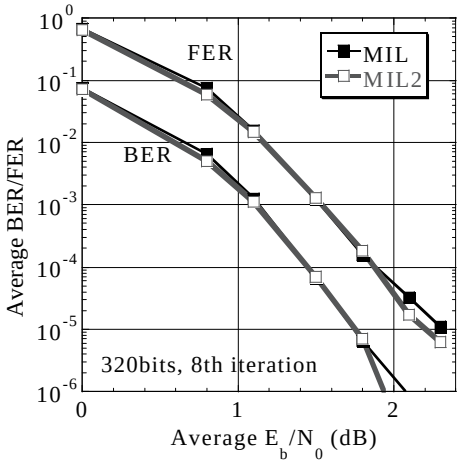
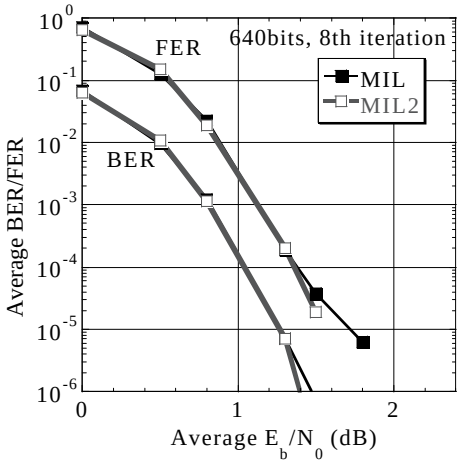


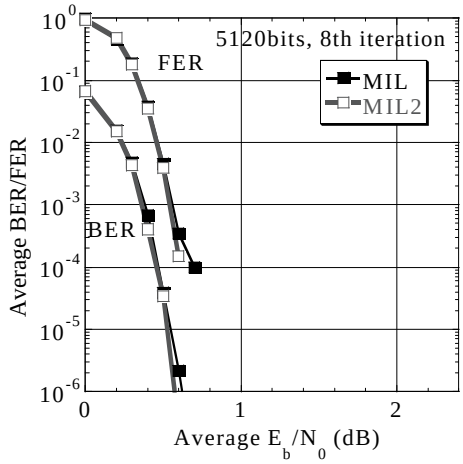
Fig. 3 The Hamming weight asymptote comparison of MIL and MIL2.



(a) BER/FER with 320-bit/8-iteration



(b) BER/FER with 640-bit/8-iteration



(c) BER/FER with 5120-bit/8-iteration

Fig. 4 The BER/FER performance comparison of MIL and MIL2 under AWGN.