TSG-RAN meeting #24 RP-040162
Seoul, Korea, 2-4 June 2004

Status Report for SI to TSG

Study Item Name: Feasibility Study for the analysis of higher chip rates for UTRA TDD evolution

SOURCE: Rapporteur (Martin Beale, IPWireless) **TSG:** RAN **WG:** 1

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Ref. to SI sheet: RAN_Study_Items.doc

Progress Report since the last TSG (for all involved WGs):

RAN1#37: Eight documents that were postponed from RAN1#36 were covered in the meeting. One of the documents covered link level simulation results for uplink Release-99 type channels, the other seven documents covered aspects of the feasibility of higher chip rate TDD systems (complexity aspects of dual mode TDD UEs, impact on other working groups, impact on specifications, signalling impact, impact on antenna systems and feasibility of higher chip rates than 7.68Mcps).

RAN4#31: Three documents were submitted and treated in RAN4#31. The topics covered were coexistence with 1.28cps TDD, a link budget analysis and a document containing minor corrections to RAN4 aspects of the TR. All open RAN4 issues have now been covered and completed for this study item.

List of Completed elements (for complex work items):

- Higher chip rate reference configuration.
- Simulation assumptions
- Link level simulation results for Release 5 type bearers
- System level simulation results for Release 5 type bearers
- Link level results for Release 99 type bearers
- Backwards compatibility and mobility sections of feasibility study
- Complexity analysis
- Coexistence of higher chip rate TDD with HCR-TDD, LCR-TDD and FDD
- Feasibility analysis (except application to 3GPP system and services)

List of open issues:

- Release 99-type system level simulations
- Application to 3GPP system and services section of feasibility analysis
- Conclusion

Estimates of the level of completion (when possible):

90%

SI completion date review resulting from the discussion at the working group:

RAN#25 (Sept 2004)

References to WG's internal documentation and/or TRs:

R1-040656 “TR25.895 v1.3.3 : Analysis of higher chip rates for UTRA TDD evolution”