TSG-RAN meeting #23 RP-040022
Phoenix, USA, 10-12 March 2004

Status Report for SI to TSG

Study Item Name: Feasibility Study for the analysis of higher chip rates for UTRA TDD evolution

SOURCE: Rapporteur (Martin Beale, IPWireless) **TSG:** RAN **WG:** 1

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Ref. to SI sheet: RAN_Study_Items.doc

Progress Report since the last TSG (for all involved WGs):

RAN1#36: Eight documents were submitted to RAN1#36. A minor document concerning minor editorial corrections to the TR was treated. There was thus unfortunately little progress in RAN1. The untreated documents covered the following topics:

- R1-040240 : uplink link level results.
- R1-040241 : dual mode UE complexity aspects.
- R1-040242 : Impact on other WGs.
- R1-040243 : Impact on specifications.
- R1-040244 : Signalling impact.
- R1-040245 : Antenna systems.
- R1-040246 : Higher chip rates than 7.68Mcps.

The untreated documents are to be discussed on the RAN1 reflector. This would allow proponents to modify documents before RAN1#37 with a view to completion of the SI by June 2004.

RAN4#30: Six documents were submitted to and treated in RAN4#30. The topics treated covered the following aspects: UE radio complexity, higher chip rate TDD / FDD coexistence, link budget considerations, use in diverse spectrum allocations and coexistence with 1.28Mcps TDD. It was proposed that coexistence with 1.28Mcps TDD could be considered at a potential WI phase, but RAN4 concluded that there was sufficient time before the completion of the SI for an analysis of coexistence with 1.28Mcps TDD to be considered in RAN4#31.

List of Completed elements (for complex work items):

- Higher chip rate reference configuration.
- Simulation assumptions
- Link level simulation results for Release 5 type bearers
- System level simulation results for Release 5 type bearers
- Downlink link level results for Release 99 type bearers
- Backwards compatibility and mobility sections of feasibility study
- Complexity analysis
- Coexistence of higher chip rate TDD with HCR-TDD
- Coexistence of higher chip rate TDD with FDD

List of open issues:

- Uplink link level performance for Release 99 type bearers (documents have been submitted, but were not treated in RAN1#36)
- Feasibility analysis (documents were submitted, but were not treated in RAN1#36)
- Release 99-type system level simulations
- Coexistence of higher chip rate TDD with 1.28Mcps TDD
- Conclusion

Estimates of the level of completion (when possible):

80%

SI completion date review resulting from the discussion at the working group:

RAN#24 (June 2004)

References to WG's internal documentation and/or TRs:

R1-040389 “TR25.895 v1.3.2 : Analysis of higher chip rates for UTRA TDD evolution”