TSG-RAN Meeting #22 Maui, Hawaii, USA, 9 - 12 December 2003

RP-030648

Title: Independent Release 5 CRs to TS 25.213

Source: TSG-RAN WG1

Agenda item: 7.2.5

TS 25.213 (RP-030648)

RP tdoc#	WG tdoc#	Spec	CR	R	Subject	Ph	Cat	Curre nt	New	WI	Remarks
RP-030648	R1-031270	25.213	064	I	Correction of figure in combining of downlink physical channels	Rel-5	F	5.4.0	5.5.0	TEI5	
RP-030648	R1-031271	25.213	065		Correction of reference to calculation of HS- DPCCH gain factor	Rel-5	F	5.4.0		HSDPA- Phys	

3GPP TSG- RAN WG1 Meeting #35 Lisbon, Portugal, 17-21 November, 2003

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How to create CRs using this form:

Comprehensive information and tips about how to create CRs can be found at http://www.3gpp.org/specs/CR.htm. Below is a brief summary:

- 1) Fill out the above form. The symbols above marked # contain pop-up help information about the field that they are closest to.
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- downloaded from the 3GPP server under ftp://ftp.3gpp.org/specs/ For the latest version, look for the directory name with the latest date e.g. 2001-03 contains the specifications resulting from the March 2001 TSG meetings.
- 3) With "track changes" disabled, paste the entire CR form (use CTRL-A to select it) into the specification just in front of the clause containing the first piece of changed text. Delete those parts of the specification which are not relevant to the change request.

5.1 Spreading

Figure 8 illustrates the spreading operation for the physical channel except SCH. The behaviour of the modulation mapper is different between QPSK and 16QAM. The downlink physical channels using QPSK are P-CCPCH, S-CCPCH, CPICH, AICH, AP-AICH, CSICH, CD/CA-ICH, PICH, PDSCH, HS-SCCH and downlink DPCH. The downlink physical channel using either QPSK or 16 QAM is HS-PDSCH. The non-spread downlink physical channels, except SCH, AICH, AP-ICH and CD/CA-ICH, consist of a sequence of 3-valued digits taking the values 0, 1 and "DTX". Note that "DTX" is only applicable to those downlink physical channels that support DTX transmission. In case of QPSK, these digits are mapped to real-valued symbols as follows: the binary value "0" is mapped to the real value +1, the binary value "1" is mapped to the real value –1 and "DTX" is mapped to the real value 0. For the indicator channels using signatures (AICH, AP-AICH and CD/CA-ICH), the real-valued symbols depend on the exact combination of the indicators to be transmitted, compare [2] sections 5.3.3.7, 5.3.3.8 and 5.3.3.9.

In case of QPSK, each pair of two consecutive real-valued symbols is first serial-to-parallel converted and mapped to an I and Q branch. The definition of the modulation mapper is such that even and odd numbered symbols are mapped to the I and Q branch respectively. In case of QPSK, for all channels except the indicator channels using signatures, symbol number zero is defined as the first symbol in each frame. For the indicator channels using signatures, symbol number zero is defined as the first symbol in each access slot. The I and Q branches are then both spread to the chip rate by the same real-valued channelisation code $C_{ch,SF,m}$. The channelisation code sequence shall be aligned in time with the symbol boundary. The sequences of real-valued chips on the I and Q branch are then treated as a single complex-valued sequence of chips. This sequence of chips is scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$. In case of P-CCPCH, the scrambling code is applied aligned with the P-CCPCH frame boundary, i.e. the first complex chip of the spread P-CCPCH frame is multiplied with chip number zero of the scrambling code. In case of other downlink channels, the scrambling code is applied aligned with the scrambling code applied to the P-CCPCH. In this case, the scrambling code is thus not necessarily applied aligned with the frame boundary of the physical channel to be scrambled.

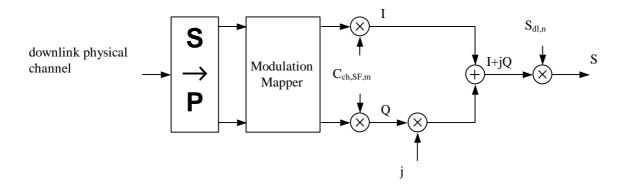


Figure 8: Spreading for all downlink physical channels except SCH

In case of 16QAM, a set of four consecutive binary symbols n_k , n_{k+1} , n_{k+2} , n_{k+3} (with $k \mod 4 = 0$) is serial-to-parallel converted to two consecutive binary symbols ($i_1 = n_k$, $i_2 = n_{k+2}$) on the I branch and two consecutive binary symbols ($q_1 = n_{k+1}$, $q_2 = n_{k+3}$) on the Q branch and then mapped to 16QAM by the modulation mapper as defined in table 3A. The I and Q branches are then both spread to the chip rate by the same real-valued channelisation code $C_{ch,16,m}$. The channelisation code sequence shall be aligned in time with the symbol boundary. The sequences of real-valued chips on the I and Q branch are then treated as a single complex-valued sequence of chips. This sequence of chips from all multi-codes is summed and then scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$. The scrambling code is applied aligned with the scrambling code applied to the P-CCPCH.

Table 3A: 16 QAM modulation mapping

i ₁ q ₁ i ₂ q ₂	I branch	Q branch
0000	0.4472	0.4472
0001	0.4472	1.3416
0010	1.3416	0.4472
0011	1.3416	1.3416
0100	0.4472	-0.4472
0101	0.4472	-1.3416
0110	1.3416	-0.4472
0111	1.3416	-1.3416
1000	-0.4472	0.4472
1001	-0.4472	1.3416
1010	-1.3416	0.4472
1011	-1.3416	1.3416
1100	-0.4472	-0.4472
1101	-0.4472	-1.3416
1110	-1.3416	-0.4472
1111	-1.3416	-1.3416

Figure 9 illustrates how different downlink channels are combined. Each complex-valued spread channel, corresponding to point S in Figure 8, is separately weighted by a weight factor G_i . The complex-valued P-SCH and S-SCH, as described in [2], section 5.3.3.5, are separately weighted by weight factors G_p and G_s . All downlink physical channels are then combined using complex addition.

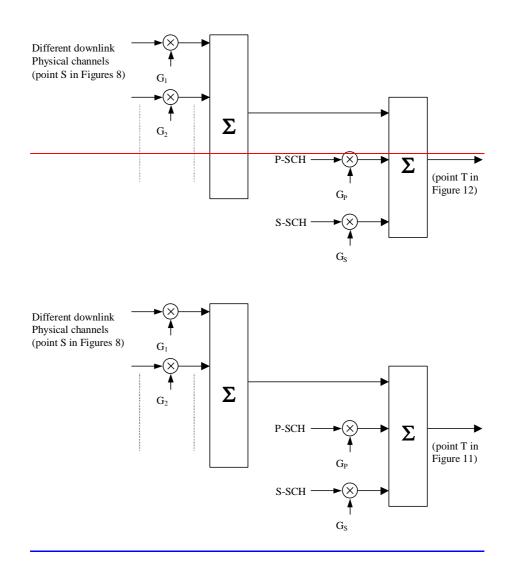


Figure 9: Combining of downlink physical channels

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4.2.1 DPCCH/DPDCH/HS-DPCCH

Figure 1 illustrates the principle of the uplink spreading of DPCCH, DPDCHs and HS-DPCCH. The binary DPCCH, DPDCHs and HS-DPCCH to be spread are represented by real-valued sequences, i.e. the binary value "0" is mapped to the real value +1, the binary value "1" is mapped to the real value -1, and the value "DTX" (HS-DPCCH only) is mapped to the real value 0. The DPCCH is spread to the chip rate by the channelisation code c_c . The n:th DPDCH called DPDCH $_n$ is spread to the chip rate by the channelisation code $c_{d,n}$. The HS-DPCCH is spread to the chip rate by the channelisation code c_{hs} . One DPCCH, up to six parallel DPDCHs, and one HS-DPCCH can be transmitted simultaneously, i.e. $1 \le n \le 6$.

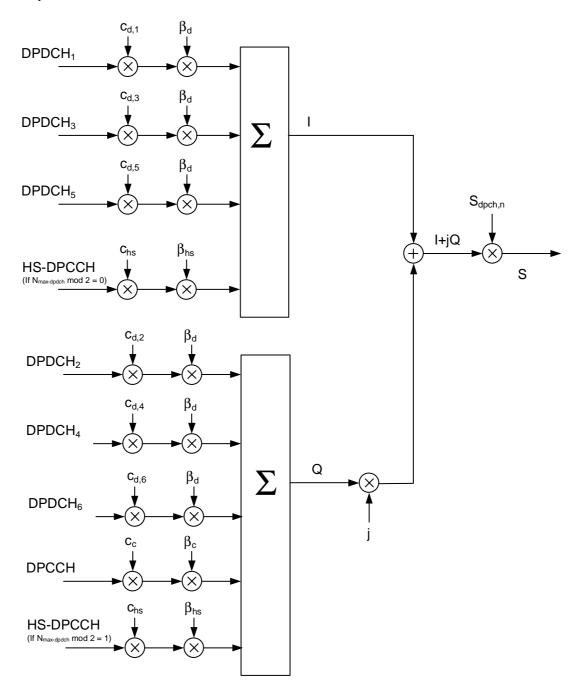


Figure 1: Spreading for uplink DPCCH, DPDCHs and HS-DPCCH

After channelisation, the real-valued spread signals are weighted by gain factors, β_c for DPCCH, β_d for all DPDCHs and β_{hs} for HS-DPCCH (if one is active).

The β_c and β_d values are signalled by higher layers or calculated as described in [6] 5.1.2.5. At every instant in time, at least one of the values β_c and β_d has the amplitude 1.0. The β_c and β_d values are quantized into 4 bit words. The quantization steps are given in table 1.

Table 1: The quantization of the gain parameters

Signalling values for β _c and β _d	Quantized amplitude ratios β _c and β _d
15	1.0
14	14/15
13	13/15
12	12/15
11	11/15
10	10/15
9	9/15
8	8/15
7	7/15
6	6/15
5	5/15
4	4/15
3	3/15
2	2/15
1	1/15
0	Switch off

The β_{hs} value is derived from the power offset Δ_{ACK} , Δ_{NACK} and Δ_{CQI} , which are signalled by higher layers as described in [6] $\frac{5.1.2.6}{5.1.2.5A}$.

The relative power offsets Δ_{ACK} , Δ_{NACK} and Δ_{CQI} are quantized into amplitude ratios as shown in Table 1A.

Table 1A: The quantization of the power offset

Signalling values for	Quantized amplitude ratios for
Δ_{ACK} , Δ_{NACK} and Δ_{CQI}	$\left(rac{\Delta_{HS-DPCCH}}{} ight)$
	10 20
8	30/15
7	24/15
6	19/15
5	15/15
4	12/15
3	9/15
2	8/15
1	6/15
0	5/15

After the weighting, the stream of real-valued chips on the I- and Q-branches are then summed and treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code $S_{dpch,n}$. The scrambling code is applied aligned with the radio frames, i.e. the first scrambling chip corresponds to the beginning of a radio frame. HS-DPCCH is mapped to the I branch in case that the maximum number of DPDCH over all the TFCs in the TFCS (defined as $N_{max-dpdch}$) is even, and mapped to the Q branch otherwise. The I/Q mapping of HS-DPCCH is not changed due to frame-by-frame TFCI change or temporary TFC restrictions.