TSG-RAN meeting #22 RP-030578
Maui, Hawaii, USA, 9-12 December 2003

Status Report for SI to TSG

Study Item Name: Feasibility Study for the analysis of higher chip rates for UTRA TDD evolution

SOURCE: Rapporteur (Martin Beale, IPWireless) **TSG:** RAN **WG:** 1

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Ref. to SI sheet: RAN_Study_Items.doc

Progress Report since the last TSG (for all involved WGs):

- RAN1#34: Two documents were presented and approved covering the following aspects :
  - HSDPA system level results
  - Link level results for Release 99 channels (this document included instantaneous downlink performance results)

- RAN1#35: Two documents (with associated text proposals) were presented. These documents covered the following aspects:
  - UE complexity analysis
  - UTRAN complexity analysis

- RAN4#29: A document covering TDD/TDD coexistence was presented and approved. RAN4 expects that there will be a future contribution regarding the coexistence of a higher chip rate TDD with FDD.

List of Completed elements (for complex work items):

- Higher chip rate reference configuration.
- Simulation assumptions
- Link level simulation results for Release 5 type bearers
- System level simulation results for Release 5 type bearers
- Downlink link level results for Release 99 type bearers
- Backwards compatibility and mobility sections of feasibility study
- Complexity analysis
- Coexistence of higher chip rate TDD with HCR-TDD

List of open issues:

- Uplink link level performance for Release 99 type bearers
- Feasibility analysis.
- Release 99-type system level simulations
- Coexistence of higher chip rate TDD with FDD

Estimates of the level of completion (when possible):

75%

SI completion date review resulting from the discussion at the working group:

RAN#24 (June 2004)

References to WG's internal documentation and/or TRs:

R1-031345 “TR25.895 v1.3.0 : Analysis of higher chip rates for UTRA TDD evolution”

A draft version of TR25.895 including the TDD / TDD coexistence text proposal has been circulated to the RAN1 and RAN4 reflectors.