**3GPP TSG RAN #18** **Tdoc RP-020823**

**New Orleans, USA, 3rd – 6th December, 2002**

**Agenda Item:** 7.1.5

**Source:** Philips

**Title:** Performance of HS-DPCCH

**Document for:** Information

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## 1. Introduction

RAN WG1 has for some time been studying the performance of the UL HS-DPCCH for the HARQ signalling for HSDPA. Based on discussion in RAN WG2, the performance targets for ACK/NACK reliability in order to satisfy protocol and efficiency considerations are as follows:

- The probability of the Node B decoding an ACK when a transport block has been correctly received by the UE on HS-DSCH:- > 0.99
- The probability of the Node B decoding an ACK when the CRC has failed for a transport block on the HS-DSCH:- < 0.0001 (0.001 for difficult radio conditions)
- The probability of the Node B decoding an ACK when the HS-SCCH is not detected by the UE:- < 0.01 (0.1 for difficult radio conditions)

The last requirement applies under the assumption that the probability of the UE failing to detect the HS-SCCH is less than 0.01.

Several companies' simulation results have shown that meeting these requirements with the current Rel5 specifications, even under typical radio conditions (e.g. Soft Handover, particularly with unfavourable radio link imbalance) cannot be achieved without raising the DPCCH power (which would reduce uplink capacity and range using R99 channels) and/or using ACK/NACK repetitions (limiting the peak bit rate and reducing the throughput achievable with HSDPA for UE categories with minimum inter TTI interval equal to one). Some results indicating the extent of this problem are shown in Section 2.

RAN WG1 has therefore considered proposals to improve the reliability of ACK/NACK signalling. One of these proposals (POST/PRE scheme) has been shown to give a worthwhile improvement in performance [1,2].

The POST/PRE proposal operates by means of some additional physical layer signals (transmitted on the HS-DPCCH) which aid the Node B in decoding the HS-DPCCH HARQ signalling reliably. RAN WG2 has confirmed [in RP-020683] that these physical layer signals will not have any impact on higher layers, but would be entirely processed within the physical layer.

CRs for this scheme have been endorsed as technically correct by RAN WG1, and are presented separately to RAN for a final decision on acceptance [3].

Some simulation results for the scheme are presented in Section 3.

## 2. Performance problems with current specifications

This section considers the measures already available in the Rel 5 specifications for improving HS-DPCCH performance.

(1) Choosing a high power offset for HS-DPCCH relative to the DPCCH can improve reliability. It was considered necessary to set a maximum power offset of 6dB.
(2) Repetition of ACK/NACK transmission is effective in reducing error rates. However, the available peak bit rate is reduced in proportion to the number repetitions. This would reduce the attractiveness of the 7 classes of higher-end UE's.

(3) It is possible to improve ACK/NACK reliability by raising the DPCCH power. This can be done by adjusting the SIR target for the closed loop power control. However, the performance and efficiency for R'99 channels will be affected.

Since the performance issues are particularly serious in Soft Handover we focus our attention mainly on that scenario (although there are also problems when not in soft handover).

Figure 1 shows the power offset required for the HS-DPCCH relative to the DPCCH in order to meet the "relaxed performance requirements" when the UE is in SHO with balanced links.

The maximum possible offset is also shown; RAN WG1 has fixed this at 6dB as a result of interference and peak-to-average ratio considerations.

Figure 1 also shows the effect of raising the SIR target of the normal UL DPCCH in order to try to improve the UL channel estimation for the HS-DPCCH, and to enable a higher HS-DPCCH power to be used without requiring a larger offset than 6dB from the normal DPCCH.

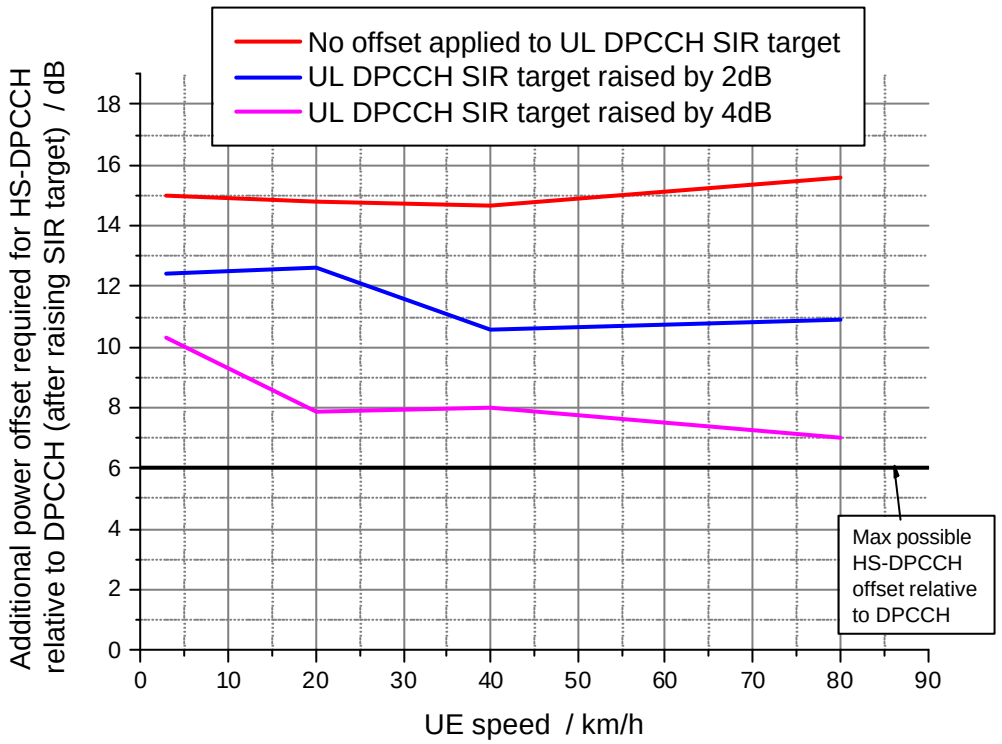


**Figure 1: Relaxed error rate requirements: SHO (2 Node Bs), balanced links, N_acknack_transmit = 1**

It can be seen from Figure 1 that even after applying a 4dB power offset to the DPCCH, a further offset of over 10dB would be required for the HS-DPCCH, just to meet the relaxed requirements.

Increasing the DPCCH power also has other undesirable side-effects, such as increasing the interference generated by the UL dedicated channels. It is likely that the gain factors ($ß_c$ and $ß_d$) would also have to be adjusted.

Figure 2 shows the effect of using repetitions of the ACK/NACK messages on the HS-DPCCH. Even with N_acknack_transmit = 2, the relaxed error rate requirements cannot be met at low speeds in SHO, even with balanced links.

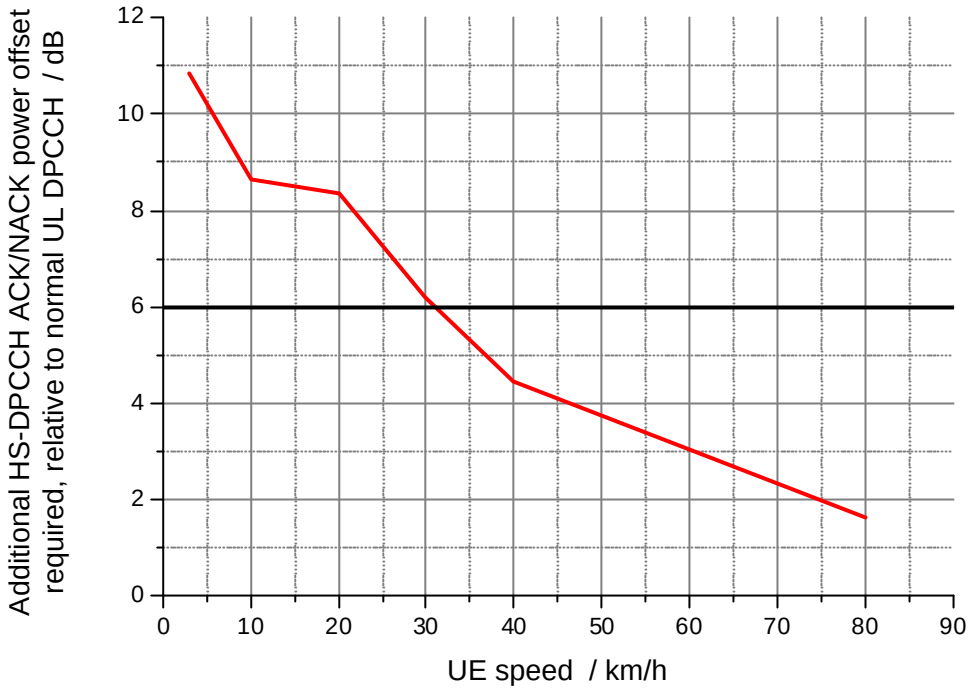


**Figure 2: Relaxed error rate requirements: SHO, balanced links, N_acknack_transmit = 2**

In Figure 3, it can be seen that the situation gets even worse when the links are unbalanced in SHO. With a link imbalance of only 3dB, an increase of 4dB in the SIR target, combined with the use of repetitions, would still require a further HS-DPCCH power offset of 9-10dB in order to meet the relaxed error rate requirements.

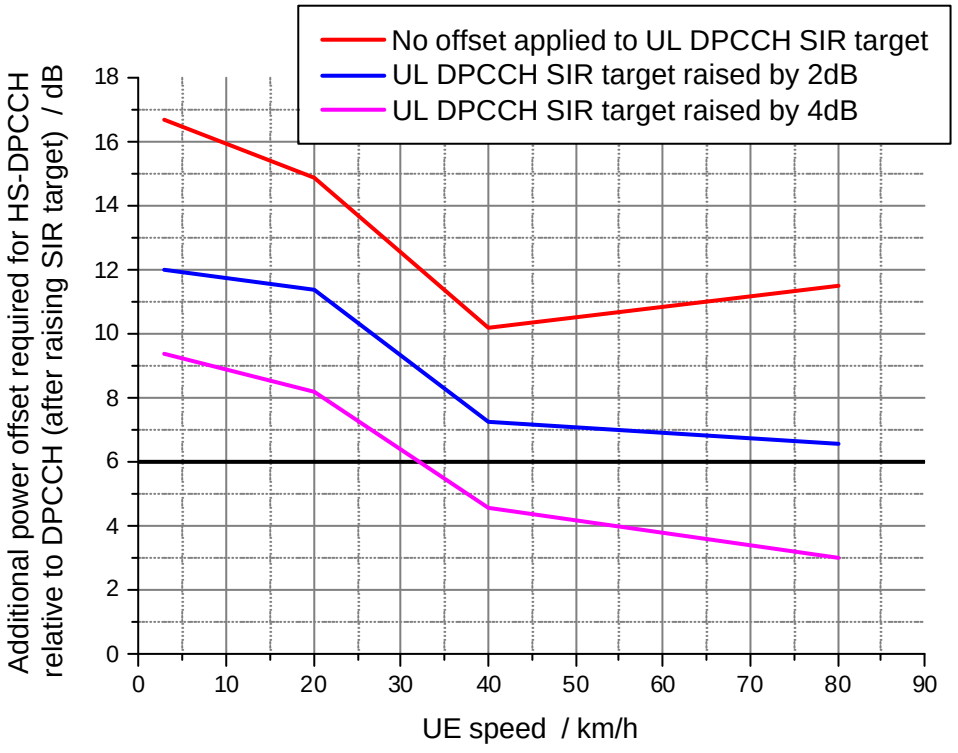


**Figure 3: Relaxed error rate requirements: SHO (2 Node Bs), 3dB link imbalance, N_acknack_transmit = 2**

Further simulation results are given in Annex A for the original performance requirements in SHO.

## 3. Performance of the PRE/POST Scheme

**Error! Reference source not found.** shows an example of the performance of the proposed POST/PRE scheme. It can be seen that the POST/PRE scheme can fully satisfy the relaxed performance requirements at all speeds in SHO, without needing any power offset on the DPCCH or needing more than 6dB offset on the HS-DPCCH.

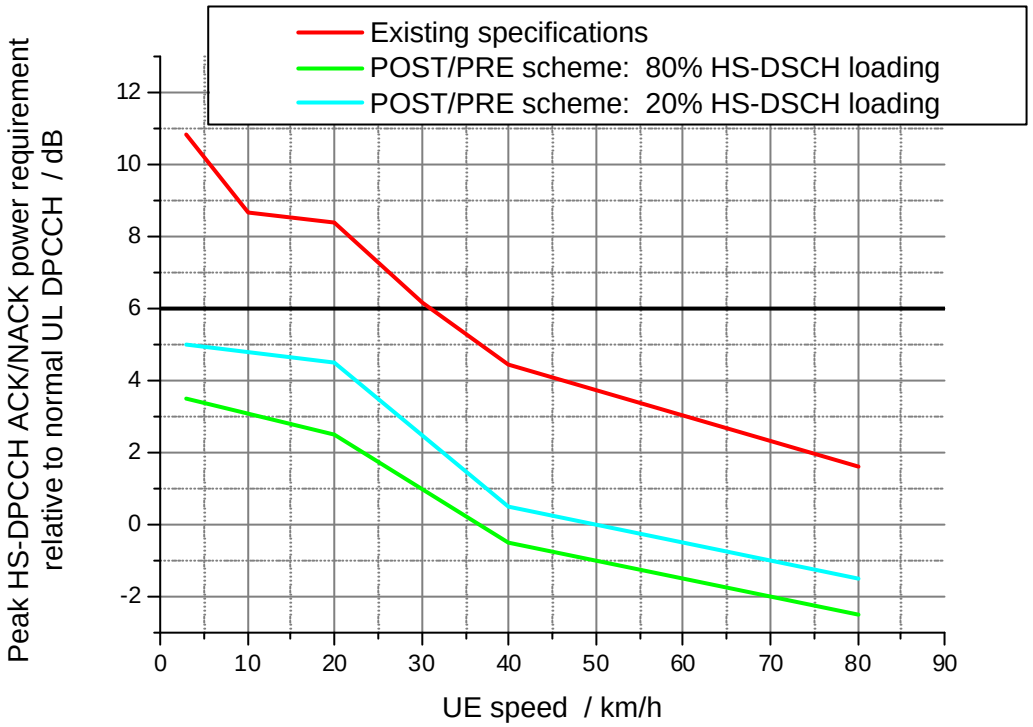


**Figure 4: Performance of POST/PRE scheme for relaxed error rate requirements in SHO (N_acknack_transmit = 2)**

Further simulation results for the POST/PRE scheme, both in SHO and not in SHO, are given in Annex B.

## 4. Conclusions

The results presented here have emphasised the problem in meeting HS-DPCCH performance requirements, particularly at low speeds in soft handover.

Further results have been presented showing the effectiveness of the PRE/POST scheme.

## 5. References


[1] R1-02-1334, "Scheme for meeting HS-DPCCH performance requirements for Rel-5", Philips

[2] R1-02-1335, “Simulation results on scheme for meeting HS-DPCCH performance requirements for Rel-5”, Philips

[3] RP-020850, “HS-DPCCH in SHO”, Philips, Nokia

## Annex A: Additional simulation results for existing specifications

### A.1 Original requirements in SHO

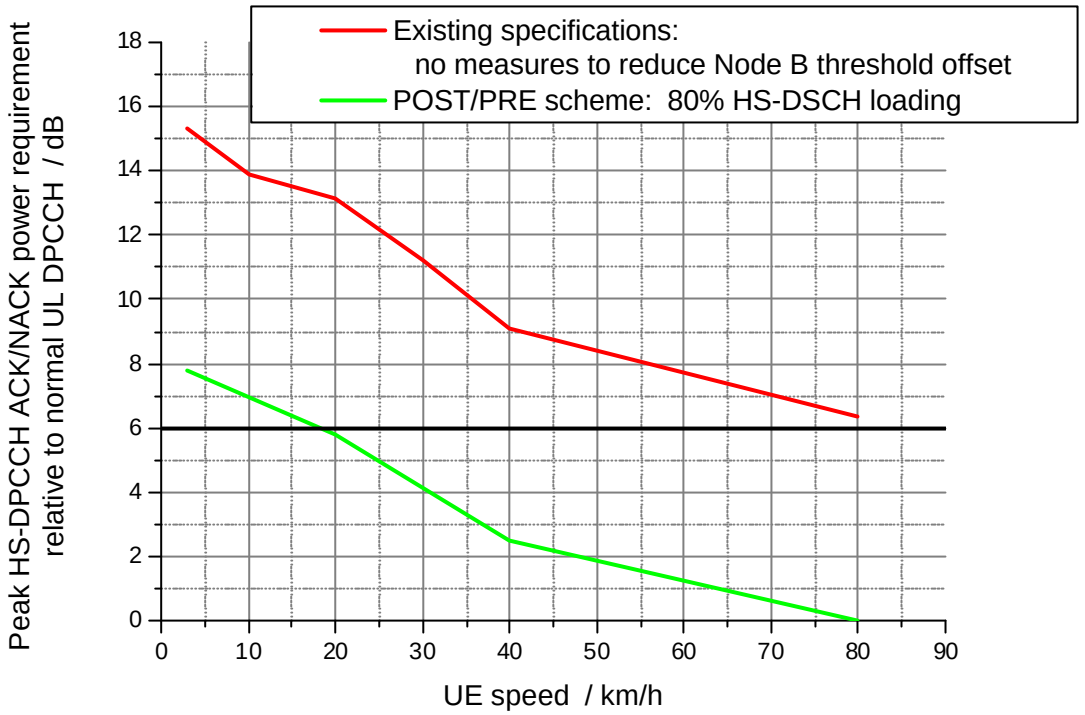


**Figure 5: Original error rate requirements: SHO, balanced links, N_acknack_transmit = 2**

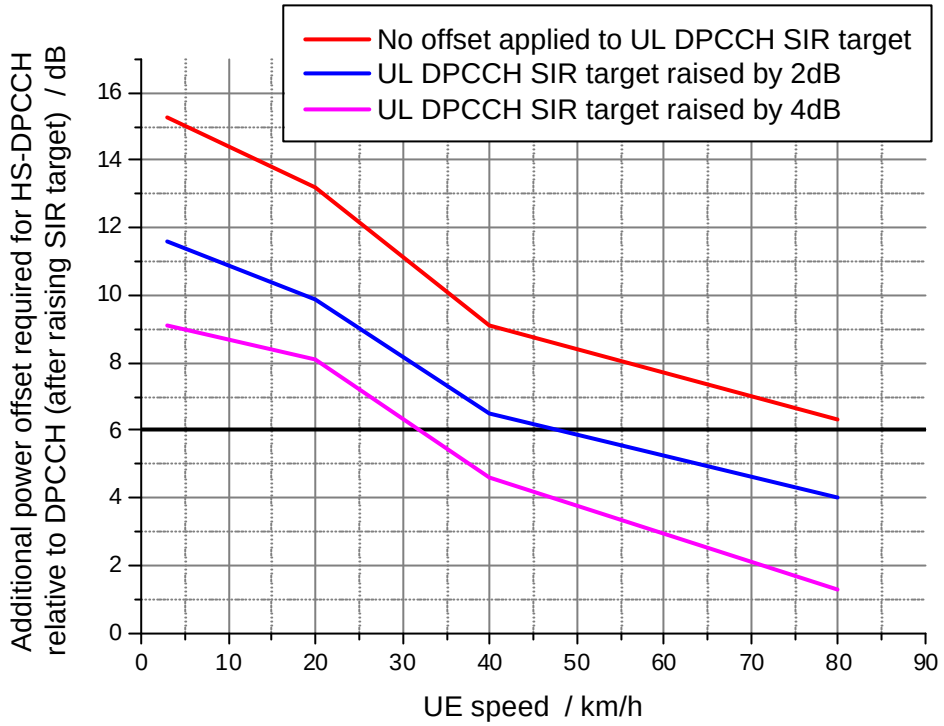


**Figure 6: Original error rate requirements: SHO, balanced links, N_acknack_transmit = 2**

## A.2 Non-SHO

**Error! Reference source not found.** shows the power offset required to meet the original performance requirements for the case when N_acknack_transmit = 1. In these conditions, the original performance requirements cannot be met for any speed greater than 20km/h. Clearly 20km/h cannot be considered a “high” speed, as required for the relaxed requirements to be applicable.

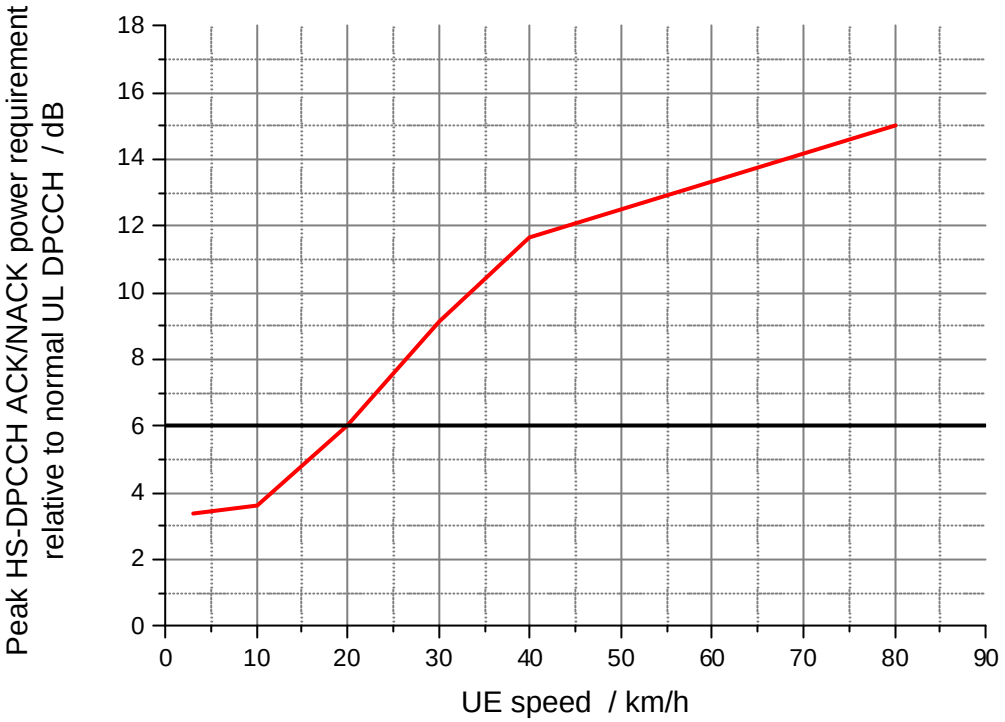


**Figure 7: Non-SHO: Original error rate requirements, N_acknack_transmit = 1**

**Error! Reference source not found.** shows the power requirements for the relaxed requirements. It can be seen that even the relaxed requirements cannot be met with the current specifications at any speed higher than about 35km/h, without using higher values of N_acknack_transmit which reduces peak throughput by at least 50%.

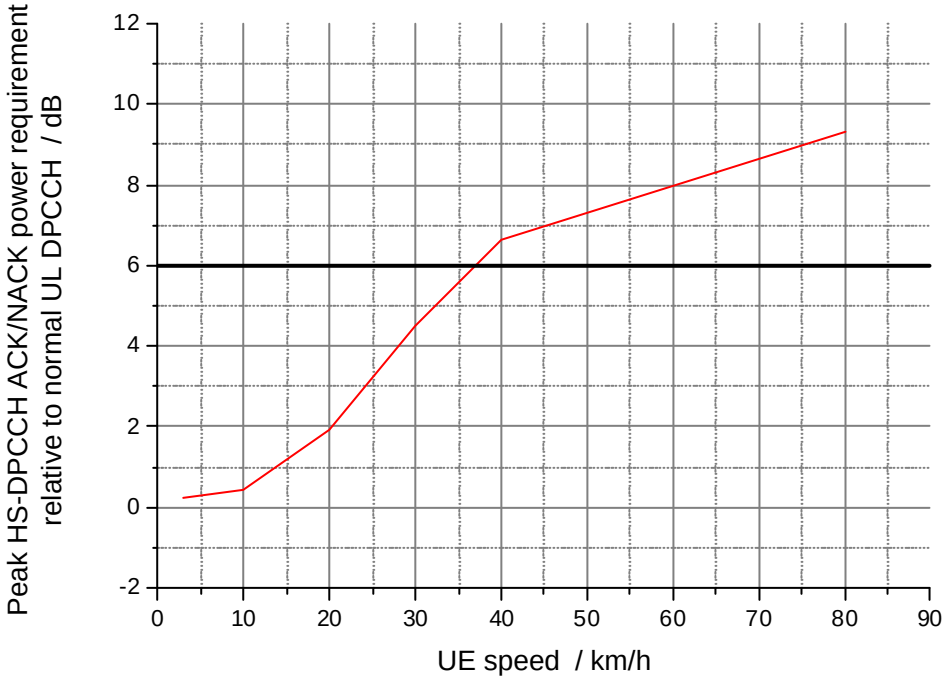


**Figure 8: Non-SHO: Relaxed error rate requirements, N_acknack_transmit = 1**

## Annex B: Additional simulation results for POST/PRE scheme

### B.1 SHO

**Error! Reference source not found.** shows that in addition to meeting the relaxed error rate requirements at all speeds in SHO, the proposed scheme is also able to meet the original performance requirements at most speeds in SHO.

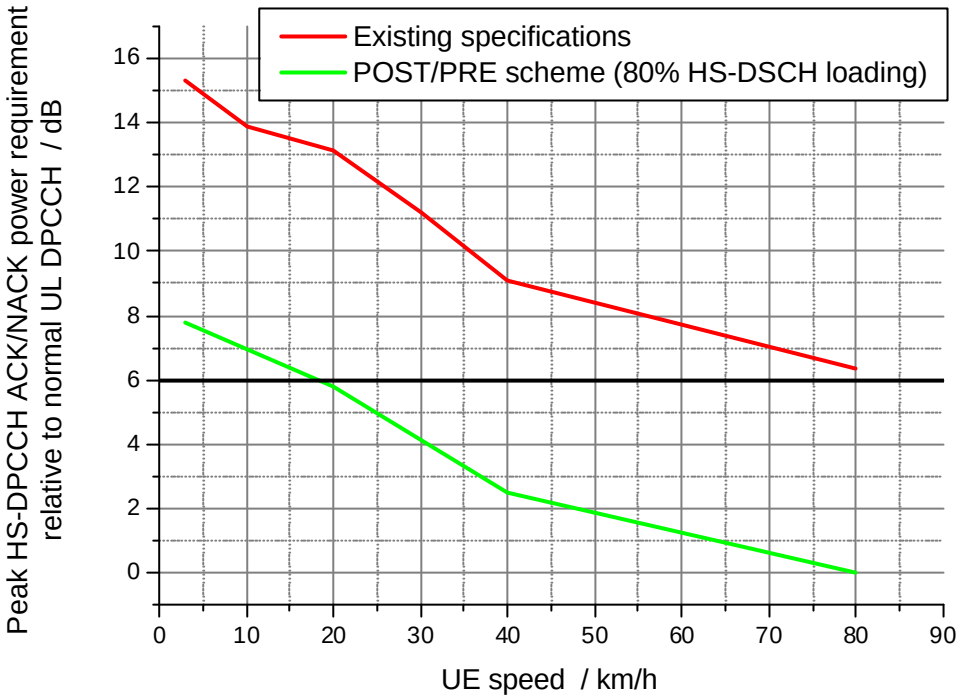


**Figure 9: Performance of POST/PRE scheme for original error rate requirements in SHO (N_acknack_transmit = 2)**

### B.2 Non-SHO

It can be seen from **Error! Reference source not found.** that the POST/PRE scheme enables the relaxed requirements to be met at all UE speeds when the UE is not in SHO, without requiring the use of repetition.

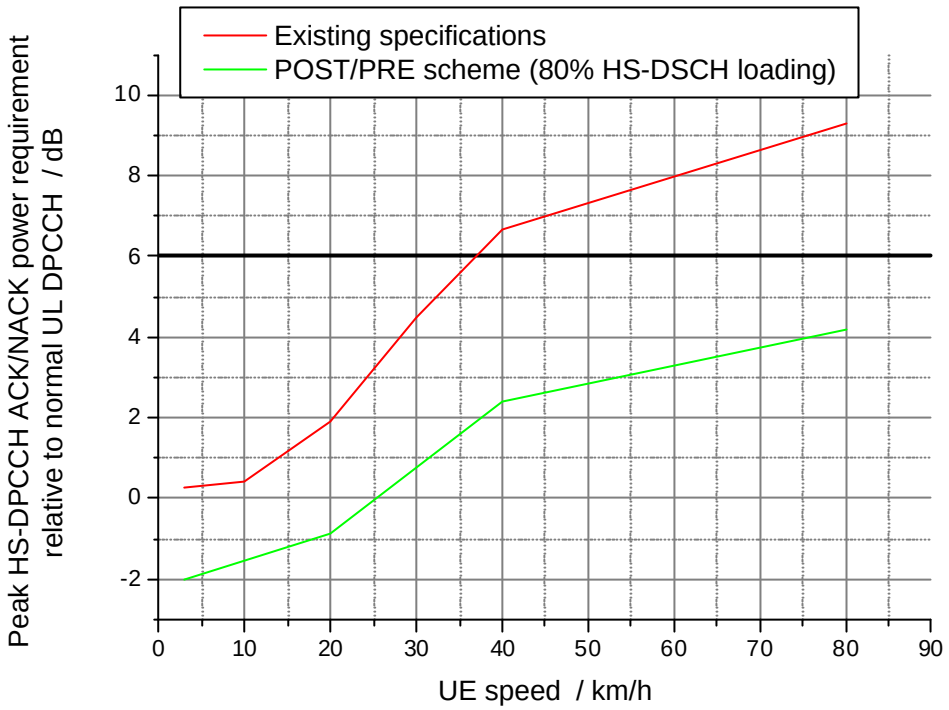


**Figure 10: Non-SHO: Performance of POST/PRE scheme for relaxed performance requirements (N_acknack_transmit = 1)**

**Error! Reference source not found.** shows that the POST/PRE scheme also enables the original performance requirements to be met at speeds up to 40km/h.

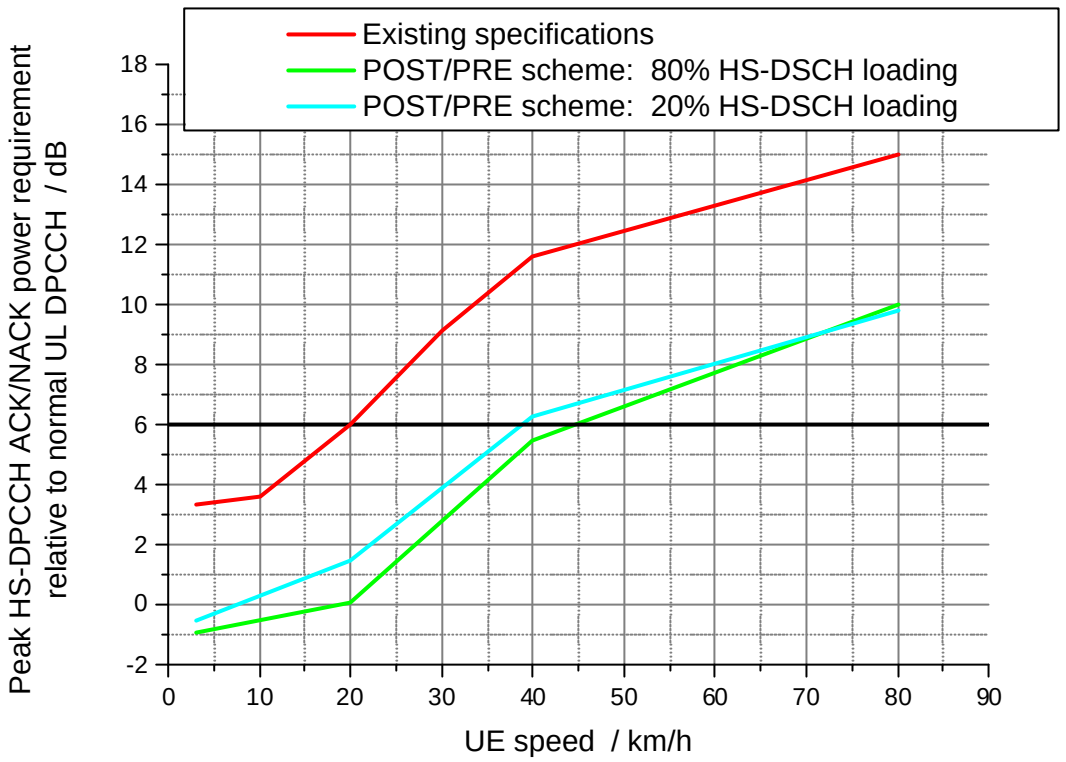


**Figure 11: Non-SHO, original performance requirements, N_acknack_transmit = 1**