TSG RAN Meeting #18 **RP-020800**
New Orleans, US, 3 - 6 December, 2002

Title **CR (Rel-5) to TR 25.991**
Source **TSG RAN WG4**
Agenda Item **7.4.5**

RAN4 Tdoc	Spec	CR	R	Cat	Rel	Curr Ver	Title	Work Item
R4-021511	25.991	001		F	Rel-5	5.0.0	Correction to Pilot Interference Mitigation Technical Report	RInImp-UERecPerf

CR-Form-v7

CHANGE REQUEST

⌘	**25.991**	**CR**	**001**	⌘ **rev**		⌘ Current version:	**5.0.0** ⌘

*For **HELP** on using this form, see bottom of this page or look at the pop-up text over the ⌘ symbols.*

Proposed change affects:	UICC apps⌘ [ ]	ME [X]	Radio Access Network [ ]	Core Network [ ]

Title:	⌘	Correction to Pilot Interference Mitigation Technical Report
Source:	⌘	RAN WG4
Work item code:	⌘	RInImp-UERecPerf
Date:	⌘	26/11/2002
Category:	⌘	**F**
Release:	⌘	Rel-5

Use one of the following categories:
F *(correction)*
A *(corresponds to a correction in an earlier release)*
B *(addition of feature),*
C *(functional modification of feature)*
D *(editorial modification)*
Detailed explanations of the above categories can be found in 3GPP TR 21.900.

Use one of the following releases:
2 (GSM Phase 2)
R96 (Release 1996)
R97 (Release 1997)
R98 (Release 1998)
R99 (Release 1999)
Rel-4 (Release 4)
Rel-5 (Release 5)
Rel-6 (Release 6)

Reason for change:	⌘	To correct the listed Intel power consumption estimate according to Tdoc R4-011483 and to fix some reference numbers.
Summary of change:	⌘	• In Sec. 6.1.1, current consumption of 10 mA corrected to power consumption of 10 mW in accordance with R4-011483 • Reference numbers fixed in Clauses 4, 5.1.1, 5.2.1.1, and Annex B. Punctuation fixed in Sec. 5.1.1. Reference R4-011483 added to Sec. 2.
Consequences if not approved:	⌘	Error in Intel's listed power consumption estimate

Clauses affected:	⌘	2, 4, 5.1.1, 6.1.1, Annex B				
		Y	**N**			
Other specs affected:	⌘			Other core specifications	⌘	
				Test specifications		
				O&M Specifications		
Other comments:	⌘					

How to create CRs using this form:

Comprehensive information and tips about how to create CRs can be found at http://www.3gpp.org/specs/CR.htm. Below is a brief summary:

1) Fill out the above form. The symbols above marked ⌘ contain pop-up help information about the field that they are closest to.

2) Obtain the latest version for the release of the specification to which the change is proposed. Use the MS Word "revision marks" feature (also known as "track changes") when making the changes. All 3GPP specifications can be

downloaded from the 3GPP server under ftp://ftp.3gpp.org/specs/ For the latest version, look for the directory name with the latest date e.g. 2001-03 contains the specifications resulting from the March 2001 TSG meetings.

3) With "track changes" disabled, paste the entire CR form (use CTRL-A to select it) into the specification just in front of the clause containing the first piece of changed text. Delete those parts of the specification which are not relevant to the change request.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies. In the case of a reference to a 3GPP document (including a GSM document), a non-specific reference implicitly refers to the latest version of the document *in the same Release as the present document.*

[1] 3GPP TSGR1-00-1371, "CPICH interference cancellation as a means for increasing DL capacity," Intel, Nov. 2000.

[2] 3GPP TSGR1-00-0030, "Further Results on CPICH Interference Cancellation as A Means for Increasing DL Capacity," Intel Corporation, Jan. 2001.

[3] 3GPP TSGR4-01-0238, "CPICH Interference Cancellation as a Means for Increasing DL Capacity," Intel, Feb. 2001.

[4] 3GPP TSGRP-01-0177, "Mitigating the Effect of CPICH Interference at the UE," Intel Corporation, Mar. 2001.

[5] 3GPP TSGR4-01-0650, "On the Implementation Complexity of CPICH Interference Cancellation," Intel, May 2001.

[6] 3GPP TSGR4-01-1014, "On the potential capacity gain of CPICH interference mitigation," Intel, July 2001.

[7] 3GPP TSGR4-01-1015, "Study description for SI: Mitigating the effect of CPICH interference at the UE," Intel, 7/01.

[8] 3GPP TSGR4-01-0967, "CPICH cancellation," Motorola, July 2001.

[9] 3GPP TS 25.101, "UE Radio transmission and reception (FDD)".

[10] 3GPP TS 25.942, "RF system scenarios".

[11] 3GPP TS 34.121, "Terminal conformance specification; radio transmission and reception (FDD)"

[12] 3GPP TSGR4-01-1330, "Feasibility Assessment for CPICH Interference Mitigation", Intel, September 2001.

[13] 3GPP TSGR4-01-1230, "CPICH cancellation, 2-way soft handoff capacity gain" Motorola, September 2001.

[14] 3GPP TSGR4-01-1231, "CPICH cancellation, UE sample time offsets" Motorola, September 2001.

[15] 3GPP TSGR4-01-1232, "CPICH cancellation complexity" Motorola, September 2001.

[16] 3GPP TSGR4-01-1202, "Simulation results for CPICH interference mitigation" Nokia, September 2001.

[17] 3GPP TSGR4-01-1256, "Capacity gain from CPICH cancellation", Telia, September 2001.

[18] 3GPP TSGR4-01-1392, "Comments on the CPICH Interference Cancellation Scheme," Ericsson, Nov. 2001

[19] 3GPP TSGR4-01-1455, "CPICH Interference Mitigation Accuracy," Intel Corp., Nov. 2001.

[20] 3GPP TSGR4-01-1483, “Correction on CPICH Interference Mitigation Complexity”, Intel, November 2001.

4 Background and Introduction

The present document provides the results of the 3GPP Study Item on Mitigating the Effect of CPICH (Common Pilot Channel) Interference at the UE. The objective of the study, and thus, of the present document, is to assess the potential benefits of this UE capability and to evaluate its implementation complexity. Additional information on this topic can be found in a number of prior 3GPP contributions [1] to [78].

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5 Performance Evaluation

5.1 Radio Network Level Simulations

In this clause we evaluate the potential capacity gains of CPICH interference mitigation by means of radio network level simulations. A number of companies have submitted simulation results, which are detailed below.

5.1.1 Intel Simulation Results

The radio network simulations presented here were originally reported in [12] to assess capacity gains available through CPICH interference mitigation. The proposed methodology for the simulations are very similar to the methodology defined in document TR 25.942 [10] for FDD to FDD coexistence studies. For each snapshot of the Monte Carlo simulation, users are randomly placed across the cells, and power control and handover are modeled as described in TR 25.942. System capacity is defined as the number of users supported when the network is loaded to the point where 95% of the users are satisfied. The simulations will focus on a single operator, macro-cell environment and will compare system capacity for systems with and without pilot interference mitigation enabled.

The assumptions for the radio network simulations that were used to generate the results reported in the next clause are shown in annex A, which mostly follow those first presented in [7], (and which are mostly identical to those found in [10]). Two difference are that the maximum number of users in the Active Set was increased to 3, and 3 sector cells where used instead of omni-directional cells, (as requested by Work Group 4 delegates over the email reflector). In addition the 144 kbps service was added for simulation, and the maximum transmit powers for 64 kbps and 144 kbps services were adjusted to reflect more realistic values. Note that the suggested Eb/No target values in Annex A were taken from the Case 3 FDD performance requirements in TS 25.101, (where Ec/Ior requirements were converted to Eb/No requirements by the formula in clause 12 of TS 25.942 [10]). Note also that a 100% activity factor was used for the 12.2 kbps simulations, as in [10], instead of 50% initially specified in [87].

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5.2 Link Level Simulations

In this clause we evaluate the performance of CPICH interference mitigation by means of link level simulations. The objective is to assess the gains of CPICH interference mitigation in realistic receiver conditions as compared to ideal receiver conditions.

5.2.1 Intel Simulation Results

These results, (initially reported in [12]), are presented in order to enable an assessment of the performance under realistic receiver conditions, including imperfect knowledge of channel, frequency, and timing.

5.2.1.1 Simulation Assumptions

The link level simulation assumptions/parameters are described in Annex B, (first presented in [87]). The assumptions mostly follow the standard assumptions used for FDD simulations in Work Group 4. Note that $\tilde{I}_{oc}$ includes the power spectral densities of other-cell base stations that may be included in the simulation, (i.e., in a multi-base link level simulation, whether or not the "other-cell" is in the Active Set). Also, the different values that were listed for CPICH_Ec/Ior were included to enable the study to consider multi-base link level simulations with surrounding cells transmitting at less than full power. Thus, if we assume that P-CPICH_Ec/Ior of the neighboring base station is –7 dB, this corresponds to an assumption of the base station transmitting at 50% of peak transmit power.

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6 Complexity Evaluation

6.1 Intel Complexity Assessment

The results reported here were initially presented in [5,12].

6.1.1 Basic Complexity Assessment

This clause summarizes the complexity evaluation reported in [5] for CPICH interference mitigation. This evaluation is based on the pilot cancellation approach illustrated in figure 1 of the present document.

A key component of pilot interference cancellation is the calculation of a cross correlation term between pilot spreading code and voice/data channel spreading code, (see Appendix in [1] for more details). Fortunately, this operation has a very simple hardware implementation, as illustrated in [5].

The other main components needed for CPICH interference cancellation are:

1) Pilot despreaders, time trackers, and channel estimators.

2) Weighting of the crosscorrelations (i.e., according to the channel and transmit/receive filter response) to generate the interference terms.

3) Cancellation of the interference terms at the RAKE receiver.

The concept of pilot-cross correlation-selection was also introduced in [5] to illustrate the ability to drastically reduce the number of terms that need to be computed and cancelled. There it was shown that by selecting only the stronger terms for processing, one could reduce implementation complexity, with little resulting performance degradation. Using this approach, it was estimated in [5] and [20] that the total hardware gate count for CPICH interference cancellation is less than 100K gates, the DSP requirements are less than 5 MIPS, and the current power consumption is less than 10mWA. These numbers were presented simply as comfortable upper bounds, in order to address feasibility.

Annex B: Link Level Simulation Assumptions

The table below contains a set of standard simulation assumptions used for the Intel Link Level Simulations.

Table B.1: Link level simulation assumptions

Parameter	Value				
1) Chip Rate	3.84 Mcps				
2) Closed Loop Power Control	OFF				
3) AGC	OFF				
4) Channel Estimation	Ideal				
5) Number Samples Per Chip	1				
6) Propagation Conditions	As specified in annex B of TS 25.101				
7) Number of Bits in AD Converter	Floating Point Simulations				
8) Number of RAKE Fingers	Equal to number of taps in propagation condition models, (up to a maximum of 6).				
9) Downlink Common Physical Channels and Power Levels (excluding P-CPICH)	CPICH_Ec/Ior	= -10, -7, -5 dB			
	PCCPCH_Ec/Ior	= -12 dB			
	SCH_Ec/Ior	= -12 dB			
	PICH_Ec/Ior	= -15 dB			
	OCNS_Ec/Ior	As specified in TS 25.101, annex C			
	DPCH_Ec/Ior	= power needed to meet required BLER target			
10) Target BLER	10^{-1}, 10^{-2}				
11) BLER Calculation	BLER is calculated by comparing transmitted and received bits.				
12) PCCPCH, PICH, DCCH Models	Random symbols transmitted, ignored in the receiver				
13) TFCI Model	Random symbols, ignored in the receiver but it is assumed that the receiver gets error free reception of TFCI information				
14) Used OVSF and Scrambling Codes	Codes are chosen from the allowed set				
15) $\hat{I}_{or} / \tilde{I}_{oc}$ Values	**Data Rate**	**Static**	**Case1**	**Case 2**	**Case 3**
	12.2 kbps	-1	9	-3	-3
	64 kbps	-1	9	-3	-3
16) $\tilde{I}_{oc}$	Combined received power spectral density of AWGN and second base station				
17) Turbo Decoding	MaxLogMap algorithm is used with 8 iterations				
18) SCH Positions	Offset between SCH and DPCH is zero chips, i.e., the SCH overlaps with the first symbols in DPCH at the beginning of DPCH slot structure				
19) Measurement Channels	12.2 kbps and 64 kbps as specified in annex A of TS 25.101 [~~7~~9]				
20) Phase Reference	P-CPICH				