

TSG RAN Meeting #18
New Orleans, US, 3 - 6 December, 2002

RP-020782

Title CRs (Rel-4 and Rel-5 Category A) to TS 25.102
Source TSG RAN WG4
Agenda Item 7.4.4

RAN4 Tdoc	Spec	CR	R	Cat	Rel	Curr Ver	Title	Work Item
R4-021559	25.102	129		F	Rel-4	4.6.0	Introduction of Rel-5 clarifications and small corrections in Rel-4	TEI4
R4-021576	25.102	130		F	Rel-4	4.6.0	Name correction of logical and transport channels	TEI4
R4-021577	25.102	131		A	Rel-5	5.2.0	Name correction of logical and transport channels	TEI4

CHANGE REQUEST

⌘ **25.102 CR 129** ⌘ rev ⌘ Current version: **4.6.0** ⌘

For **HELP** on using this form, see bottom of this page or look at the pop-up text over the ⌘ symbols.

Proposed change affects: UICC apps ME Radio Access Network Core Network

Title:	⌘ Introduction of Rel-5 clarifications and small corrections in Rel-4		
Source:	⌘ RAN WG4		
Work item code:	⌘ TEI4	Date:	⌘ 26/11/2002
Category:	⌘ F	Release:	⌘ Rel-4
	Use <u>one</u> of the following categories:		Use <u>one</u> of the following releases:
	F (correction)	2 (GSM Phase 2)	
	A (corresponds to a correction in an earlier release)	R96 (Release 1996)	
	B (addition of feature),	R97 (Release 1997)	
	C (functional modification of feature)	R98 (Release 1998)	
	D (editorial modification)	R99 (Release 1999)	
	Detailed explanations of the above categories can be found in 3GPP TR 21.900 .	Rel-4 (Release 4)	
		Rel-5 (Release 5)	
		Rel-6 (Release 6)	

Reason for change:	⌘ Before RAN#17, CRs considered as "non-essential" were only agreed for Rel-5 in RAN4. It was agreed that such corrections could be introduced into Rel-4 as well. This CR proposes to apply to Rel-4 all already agreed "non-essential" Rel-5 CRs that are applicable to Rel-4.
Summary of change:	⌘ Corrections presented in the following CRs for Rel-5 are proposed for Rel-4: - Removal of "AFC on" condition for frequency stability requirement (CR108) - Update of reference to ITU-R recommendation SM.329-9 (CR125)
Consequences if not approved:	⌘ Rel-4 and Rel-5 specifications are not inlined with respect to issues that are covered in both releases. Isolated Impact Analysis: This CR has no impact on UE-Node B interworking since the proposed corrections are clarification of the standard.

Clauses affected:	⌘ 6.3, 6.6.3						
Other specs affected:	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="width: 20px; text-align: center;">Y</td> <td style="width: 20px; text-align: center;">N</td> </tr> <tr> <td style="text-align: center;"><input type="checkbox"/></td> <td style="text-align: center;"><input checked="" type="checkbox"/></td> </tr> </table> Other core specifications	Y	N	<input type="checkbox"/>	<input checked="" type="checkbox"/>	⌘	
Y	N						
<input type="checkbox"/>	<input checked="" type="checkbox"/>						
	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="width: 20px; text-align: center;">Y</td> <td style="width: 20px; text-align: center;">N</td> </tr> <tr> <td style="text-align: center;"><input type="checkbox"/></td> <td style="text-align: center;"><input checked="" type="checkbox"/></td> </tr> </table> Test specifications	Y	N	<input type="checkbox"/>	<input checked="" type="checkbox"/>	⌘	
Y	N						
<input type="checkbox"/>	<input checked="" type="checkbox"/>						
	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="width: 20px; text-align: center;">Y</td> <td style="width: 20px; text-align: center;">N</td> </tr> <tr> <td style="text-align: center;"><input type="checkbox"/></td> <td style="text-align: center;"><input checked="" type="checkbox"/></td> </tr> </table> O&M Specifications	Y	N	<input type="checkbox"/>	<input checked="" type="checkbox"/>	⌘	
Y	N						
<input type="checkbox"/>	<input checked="" type="checkbox"/>						
Other comments:	⌘ No corresponding Rel-5 CR since corrections were already agreed for Rel-5.						

How to create CRs using this form:

Comprehensive information and tips about how to create CRs can be found at <http://www.3gpp.org/specs/CR.htm>. Below is a brief summary:

- 1) Fill out the above form. The symbols above marked ¶ contain pop-up help information about the field that they are closest to.
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- 3) With "track changes" disabled, paste the entire CR form (use CTRL-A to select it) into the specification just in front of the clause containing the first piece of changed text. Delete those parts of the specification which are not relevant to the change request.

6.3 UE frequency stability

The UE modulated carrier frequency shall be accurate to within ± 0.1 PPM observed over a period of one timeslot compared to carrier frequency received from the BS. These signals will have an apparent error due to BS frequency error and Doppler shift. In the later case, signals from the BS must be averaged over sufficient time that errors due to noise or interference are allowed for within the above ± 0.1 PPM figure. The UE shall use the same frequency source for both RF frequency generation and the chip clock.

Table 6.2: voidFrequency stability

AFC	Frequency stability
ON	within ± 0.1 PPM

---NEXT SECTION---

6.6.3 Spurious emissions

Spurious emissions are emissions which are caused by unwanted transmitter effects such as harmonics emission, parasitic emission, intermodulation products and frequency conversion products, but exclude out of band emissions.

The frequency boundary and the detailed transitions of the limits between the requirement for out band emissions and spectrum emissions are based on ITU-R Recommendations SM.329-98.

CR-Form-v7

CHANGE REQUEST

⌘ **25.102 CR 130** ⌘ rev ⌘ Current version: **4.6.0** ⌘

For **HELP** on using this form, see bottom of this page or look at the pop-up text over the ⌘ symbols.

Proposed change affects: UICC apps ⌘ ME Radio Access Network Core Network

Title:	⌘	Name correction of logical and transport channels		
Source:	⌘	RAN WG4		
Work item code:	⌘	TEI4	Date:	⌘ 26/11/2002
Category:	⌘	F	Release:	⌘ Rel-4
		Use <u>one</u> of the following categories: F (correction) A (corresponds to a correction in an earlier release) B (addition of feature), C (functional modification of feature) D (editorial modification) Detailed explanations of the above categories can be found in 3GPP TR 21.900 .		Use <u>one</u> of the following releases: 2 (GSM Phase 2) R96 (Release 1996) R97 (Release 1997) R98 (Release 1998) R99 (Release 1999) Rel-4 (Release 4) Rel-5 (Release 5) Rel-6 (Release 6)

Reason for change:	⌘	No clear distinction between logical and transport channels. Puncturing levels and code rates are different for the data and control part of the transport channel.		
Summary of change:	⌘	Referencing the DCH of the DTCH and the DCH of the DCCH instead of DCCH and DCH in general for puncturing levels and coding rates.		
Consequences if not approved:	⌘	Incorrect description and inconsistency with respect to WG1 specifications.		
		<u>Isolated impact analysis:</u> The correction has no impact on UE-BS interworking.		

Clauses affected:	⌘	A.2										
Other specs affected:	⌘	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="width: 20px; text-align: center;">Y</td> <td style="width: 20px; text-align: center;">N</td> </tr> <tr> <td style="text-align: center;">X</td> <td style="text-align: center;"></td> </tr> <tr> <td style="text-align: center;"></td> <td style="text-align: center;">X</td> </tr> <tr> <td style="text-align: center;"></td> <td style="text-align: center;">X</td> </tr> </table> Other core specifications Test specifications O&M Specifications	Y	N	X			X		X	⌘	25.105 in CR129
Y	N											
X												
	X											
	X											
Other comments:	⌘	Equivalent CRs in other Releases: CR131 cat. A to 25.102 v5.2.0										

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Annex A (normative): Measurement channels

A.1 General

A.2 Reference measurement channel

A.2.1 UL reference measurement channel (12.2 kbps)

A.2.1.1 3.84 Mcps TDD Option

Table A.1

Parameter	Value
Information data rate	12.2 kbps
RU's allocated	2 RU
Midamble	512 chips
Interleaving	20 ms
Power control	2 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate 1/3 : DCH of the DTCH / DCH of the DCCH	10% / 0%

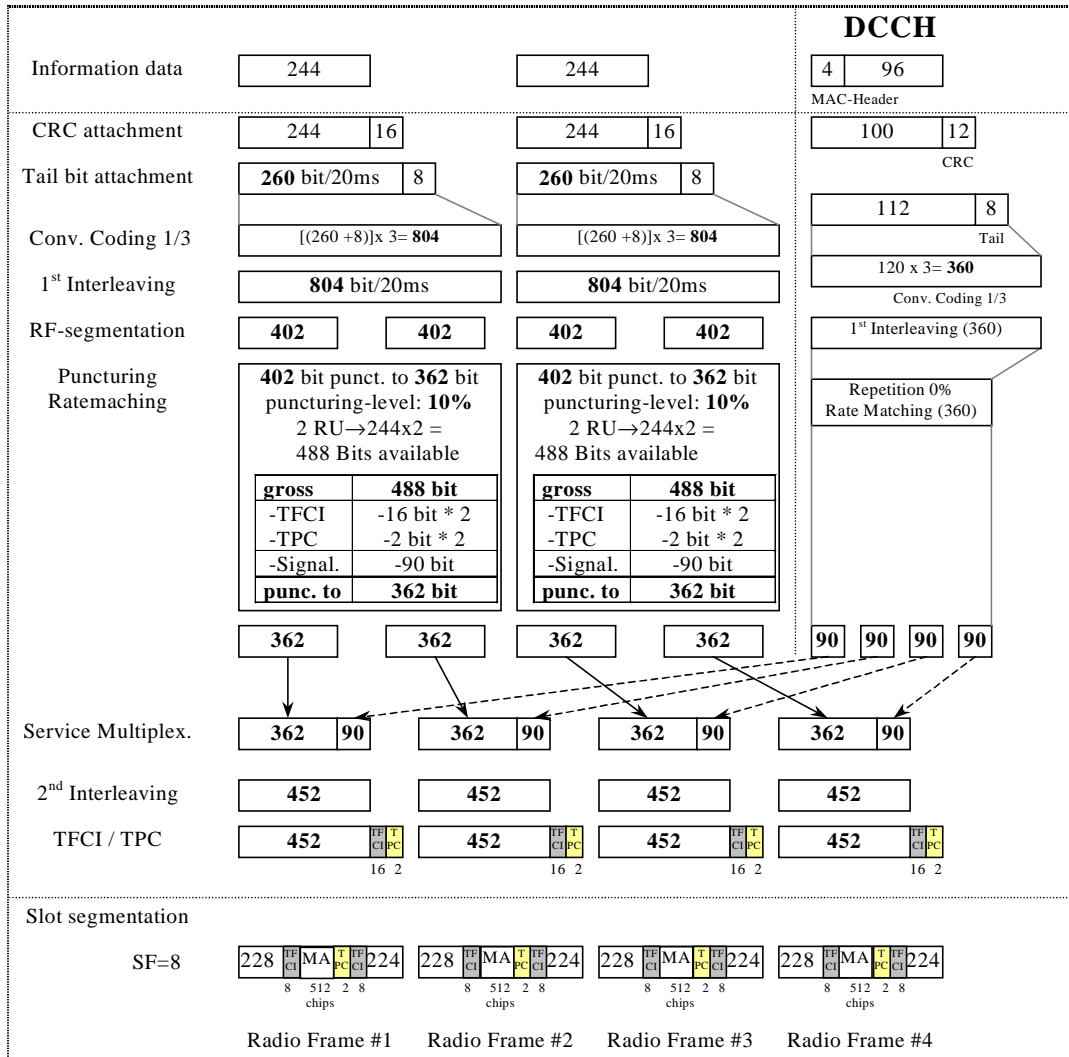


Figure A.1

A.2.1.2 1.28 Mcps TDD Option

Table A.1A

Parameter	Value
Information data rate	12.2 kbps
RU's allocated	1TS (1*SF8) = 2RU/5ms
Midamble	144
Interleaving	20 ms
Power control	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
4 Bit reserved for future use (place of SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate 1/3 : <u>DCH of the DTCH</u> / <u>DCH of the DCCH</u>	33% / 33%

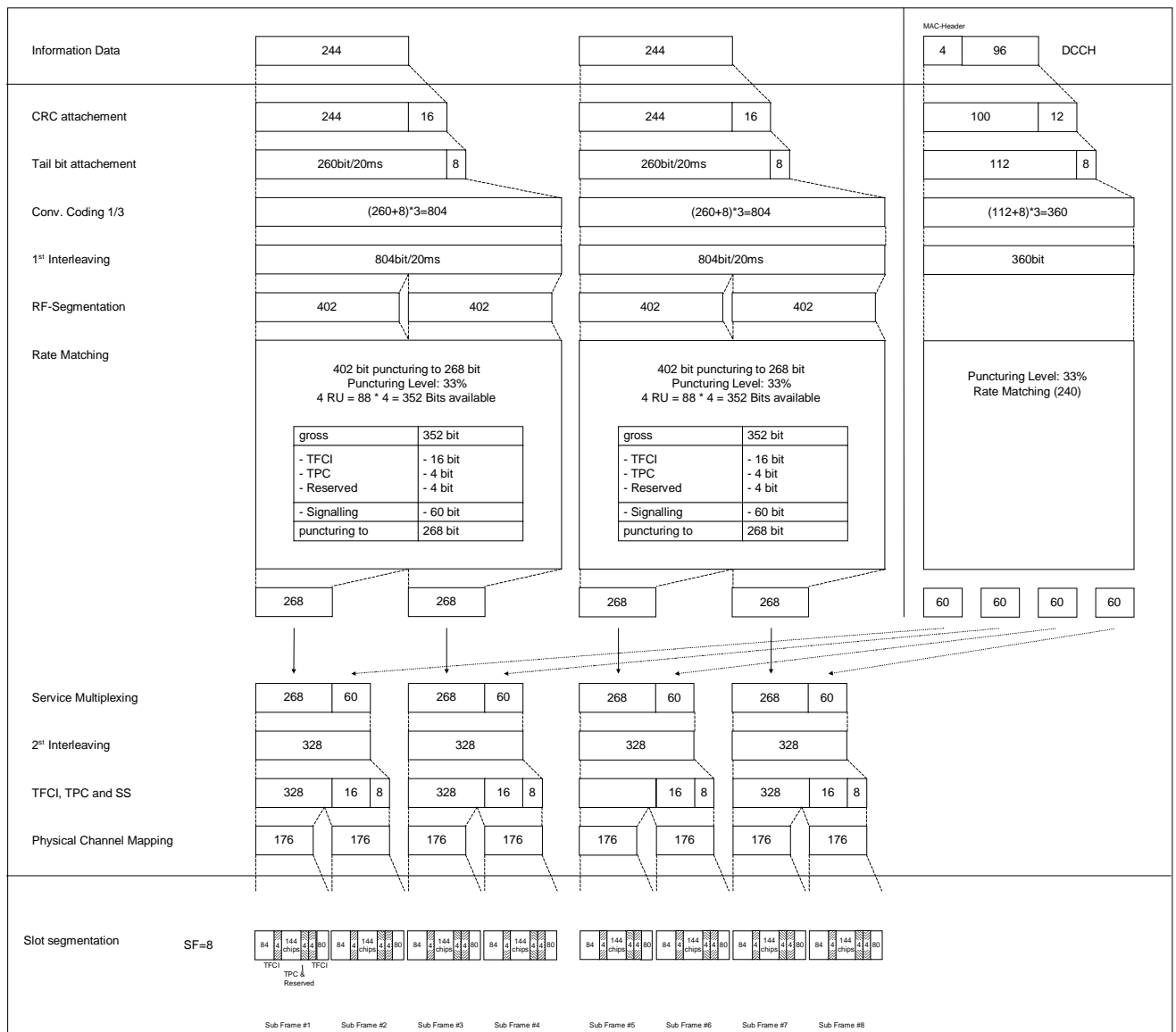


Figure A.1A

A.2.2 DL reference measurement channel (12.2 kbps)

A.2.2.1 3.84 Mcps TDD Option

Table A.2

Parameter	Value
Information data rate	12.2 kbps
RU's allocated	2 RU
Midamble	512 chips
Interleaving	20 ms
Power control	0 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate 1/3 : DCH of the DICH / DCH of the DCCH	5% / 0 %

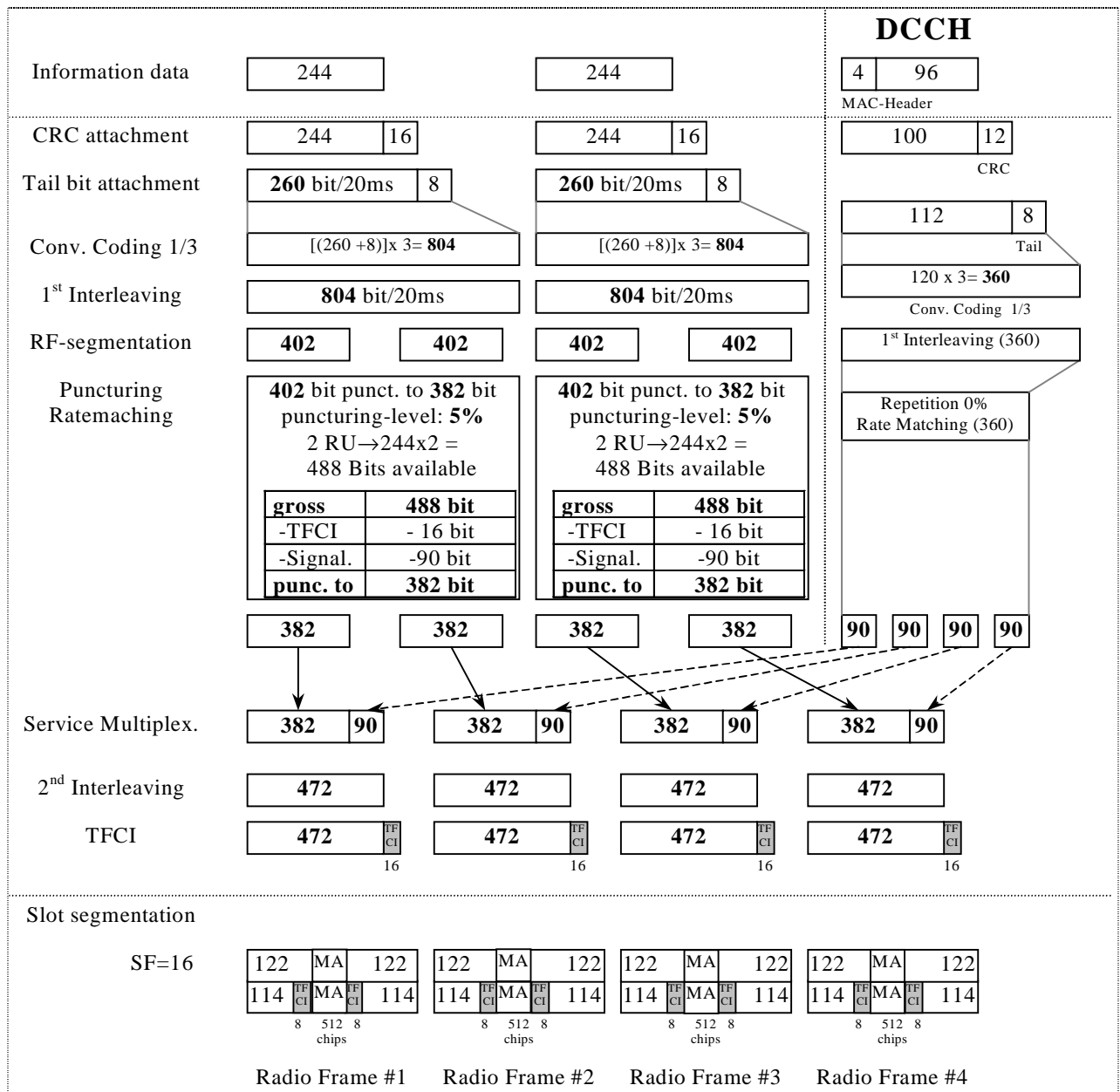


Figure A.2

A.2.2.2 1.28 Mcps TDD Option

Table A.2A

Parameter	Value
Information data rate	12.2 kbps
RU's allocated	1TS (2*SF16) = 2RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
Synchronisation Shift (SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate 1/3: <u>DCH of the DTCH / DCH of the DCCH</u>	33% / 33%

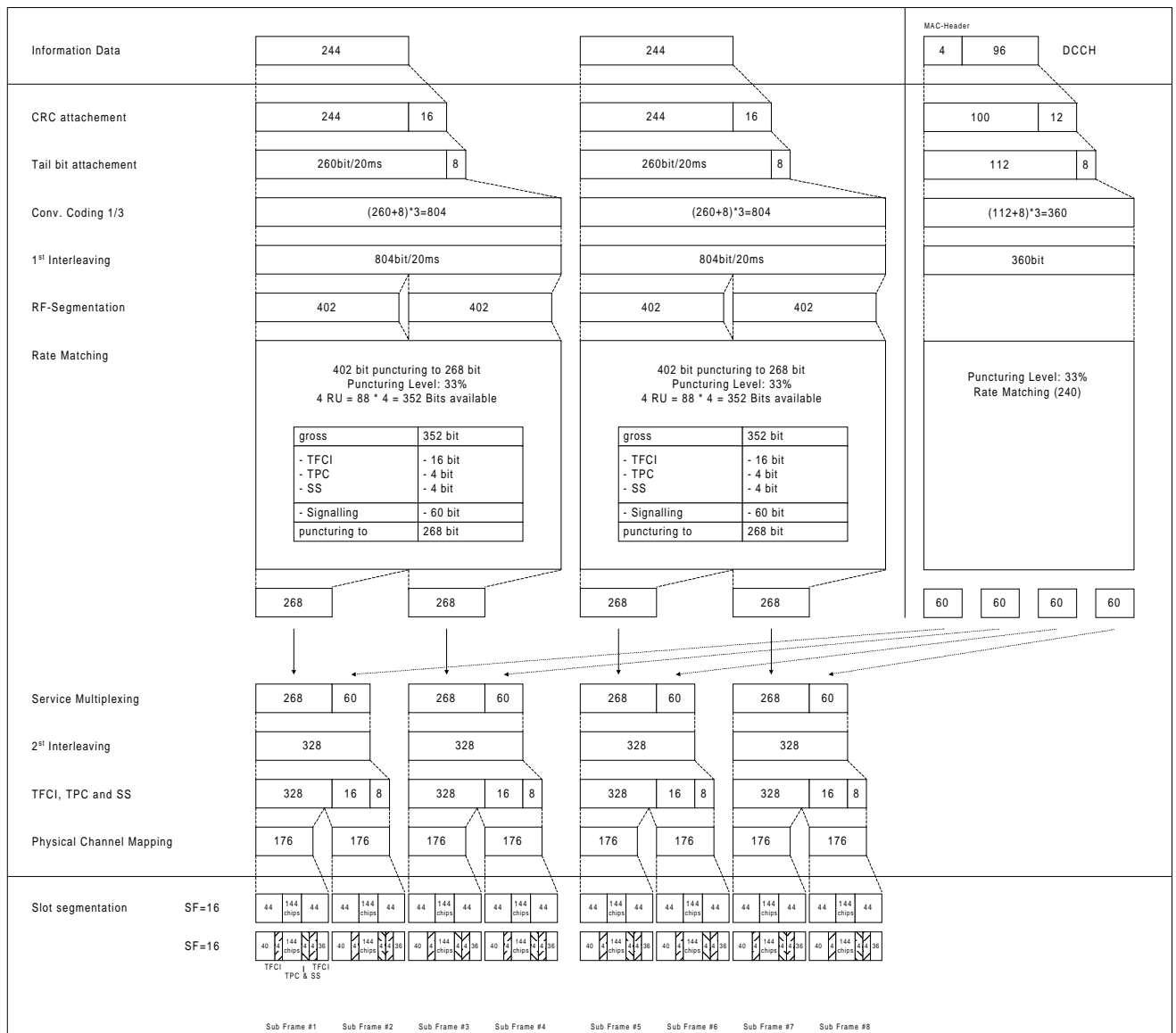


Figure A.2A

A.2.3 DL reference measurement channel (64 kbps)

A.2.3.1 3.84 Mcps TDD Option

Table A.3

Parameter	Value
Information data rate	64 kbps
RU's allocated	5 codes SF16 = 5RU
Midamble	512 chips
Interleaving	20 ms
Power control	0 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate : 1/3 DCH of the DTCH / 1/2 DCH of the DCCH	41.1% / 10%

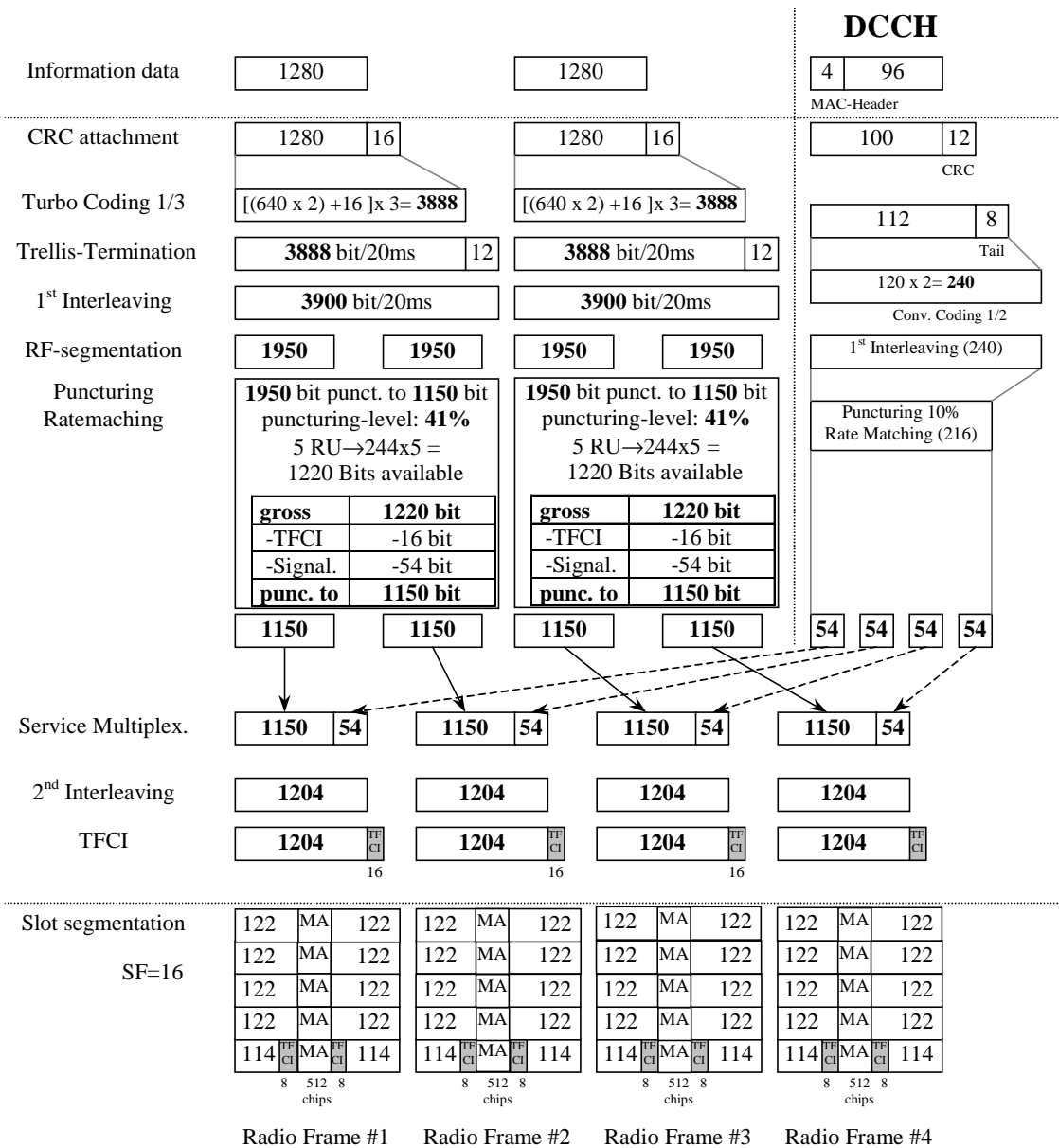


Figure A.3

A.2.3.2 1.28 Mcps TDD Option

Table A.3A

Parameter	Value
Information data rate	64 kbps
RU's allocated	1TS (8*SF16) = 8RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
Synchronisation Shift (SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate: 1/3 DCH of the DTCH / 1/2 DCH of the DCCH	32% / 0

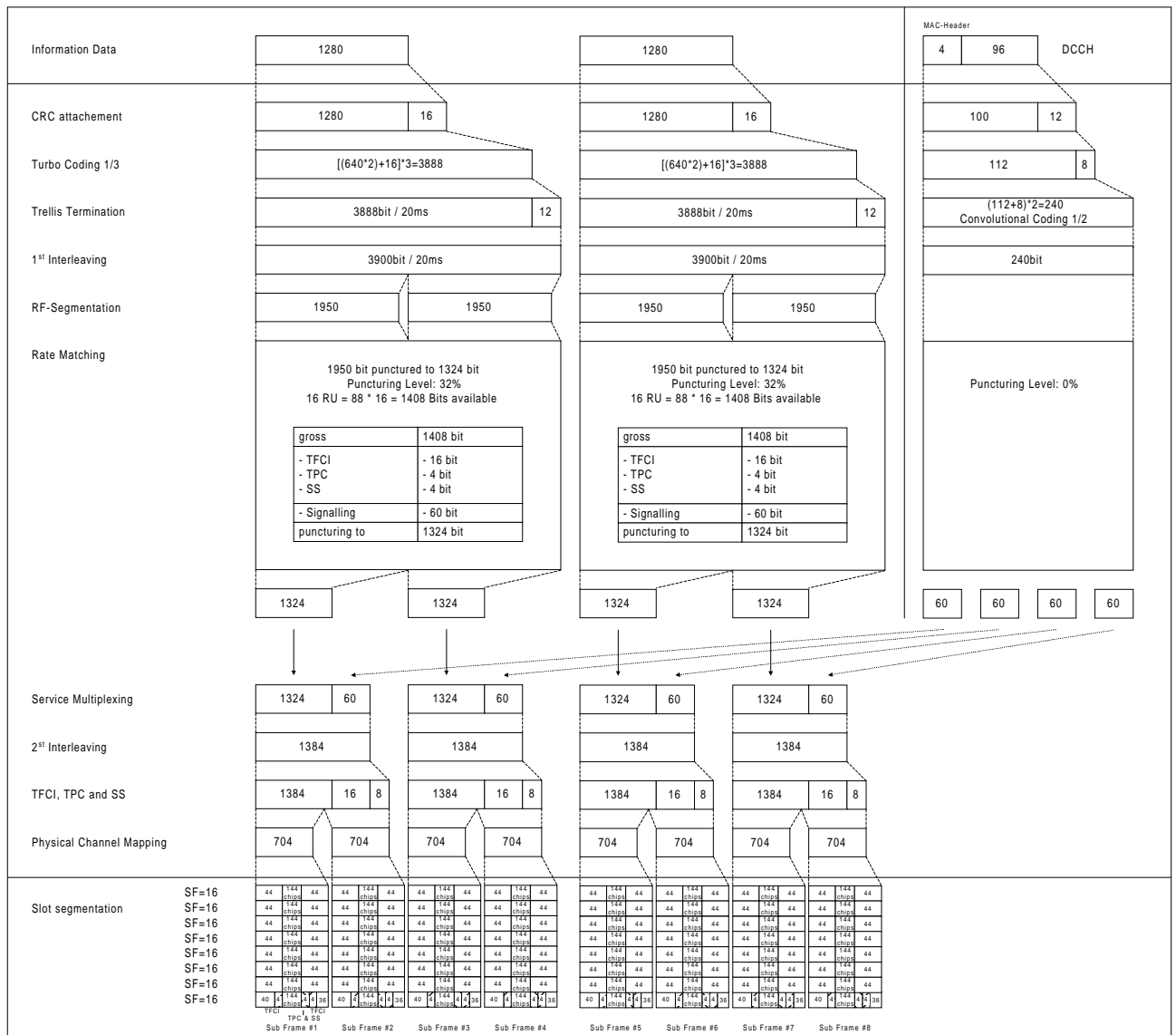


Figure A.3A

A.2.4 DL reference measurement channel (144 kbps)

A.2.4.1 3.84 Mcps TDD Option

Table A.4

Parameter	Value
Information data rate	144 kbps
RU's allocated	9 codes SF16 = 9RU
Midamble	256 chips
Interleaving	20 ms
Power control	0 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate: 1/3 <u>DCH of the DTCH</u> / 1/2 <u>DCH of the DCCH</u>	44.5% / 16.6%

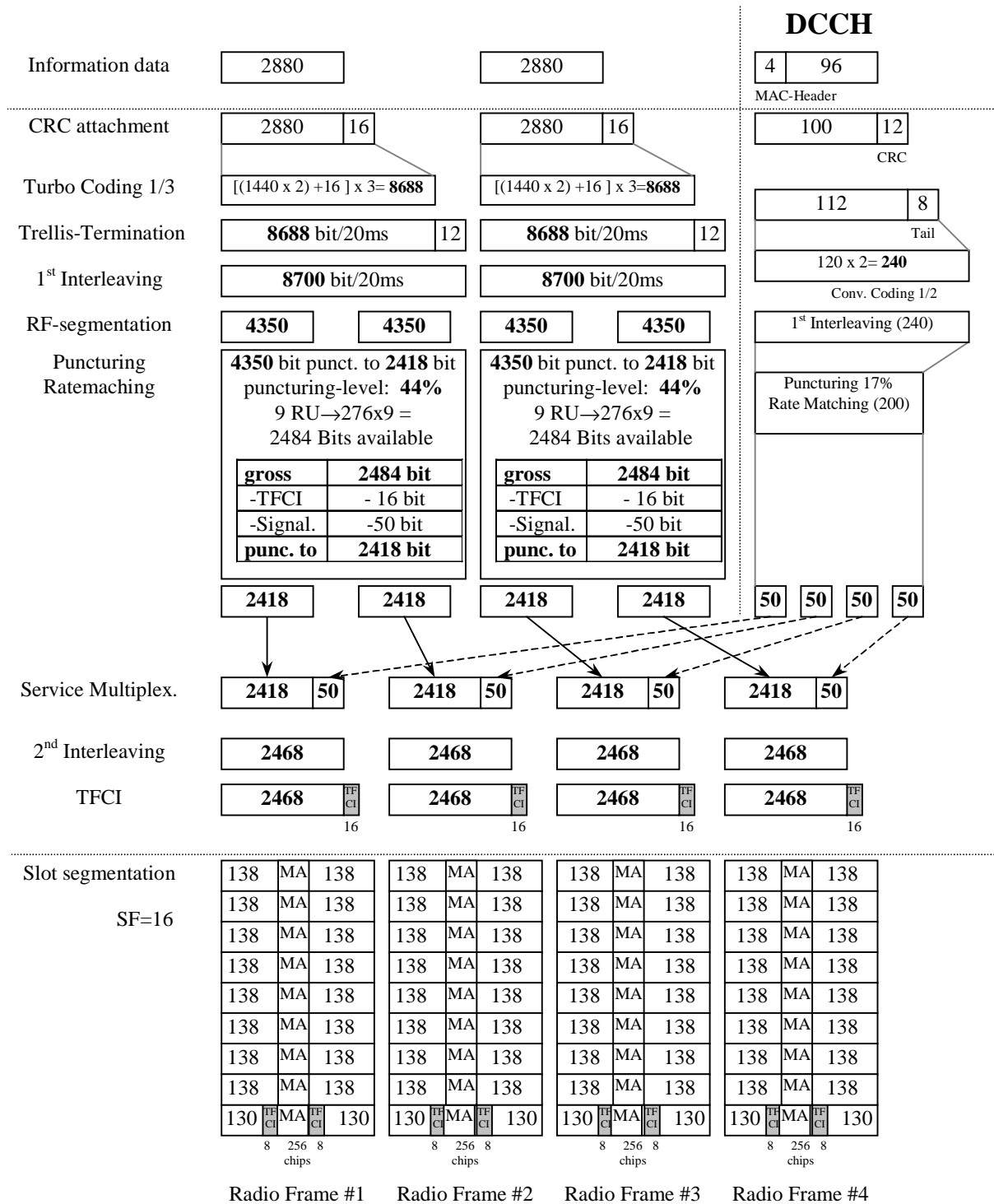


Figure A.4

A.2.4.2 1.28 Mcps TDD Option

Table A.4A

Parameter	Value
Information data rate	144 kbps
RU's allocated	2TS (8*SF16) = 16RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	8 Bit/user/10ms
TFCI	32 Bit/user/10ms
Synchronisation Shift (SS)	8 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate: 1/3 <u>DCH of the DCH</u> / 1/2 <u>DCH of the DCCH</u>	38% / 7%

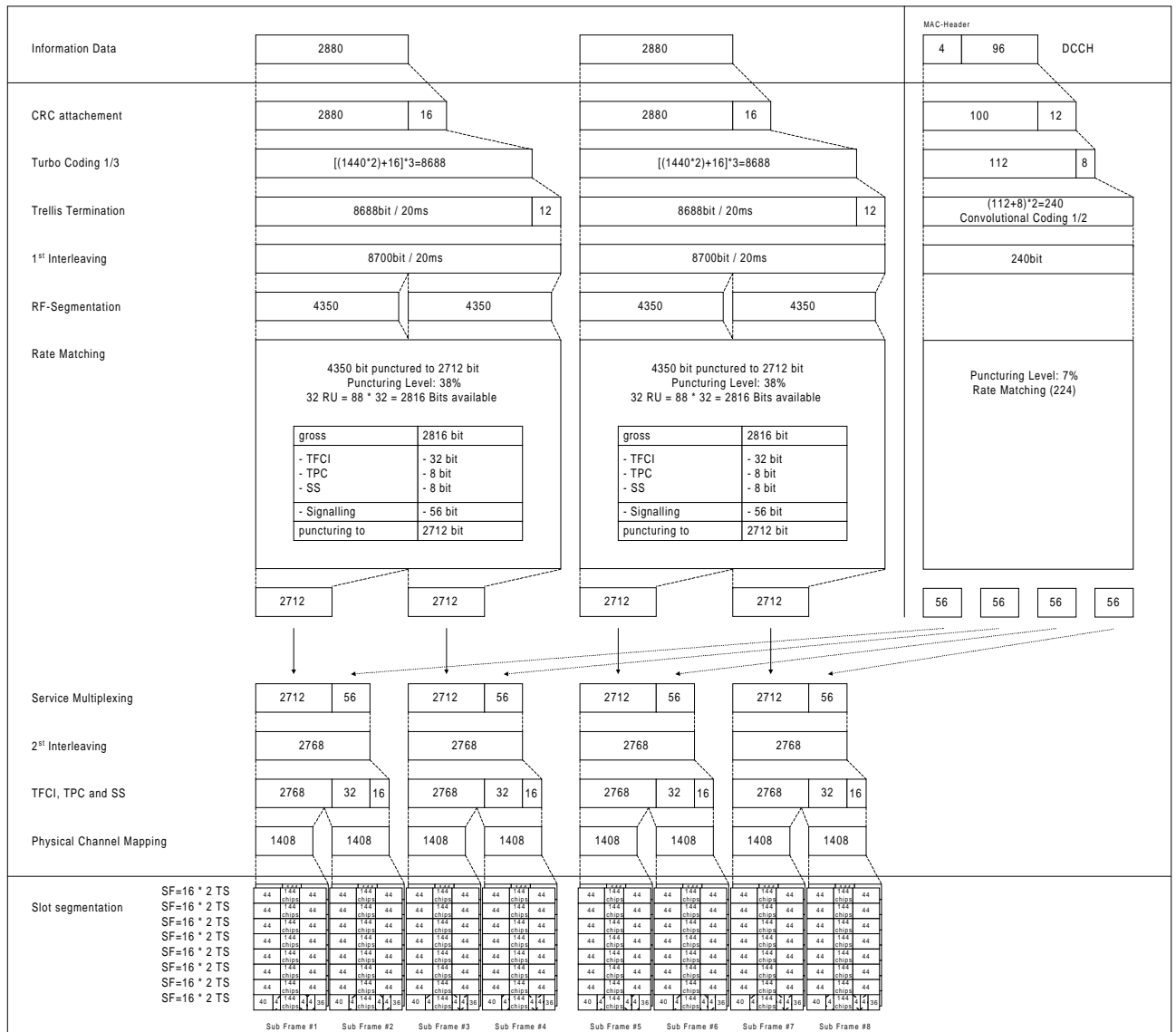


Figure A.4A

A.2.5 DL reference measurement channel (384 kbps)

A.2.5.1 3.84 Mcps TDD Option

Table A.5

Parameter	Value
Information data rate	384 kbps
RU's allocated	8*3TS = 24RU
Midamble	256 chips
Interleaving	20 ms
Power control	0 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate : 1/3 DCH of the D T CH / 1/2 DCH of the DCCH	43.4% / 15.3%

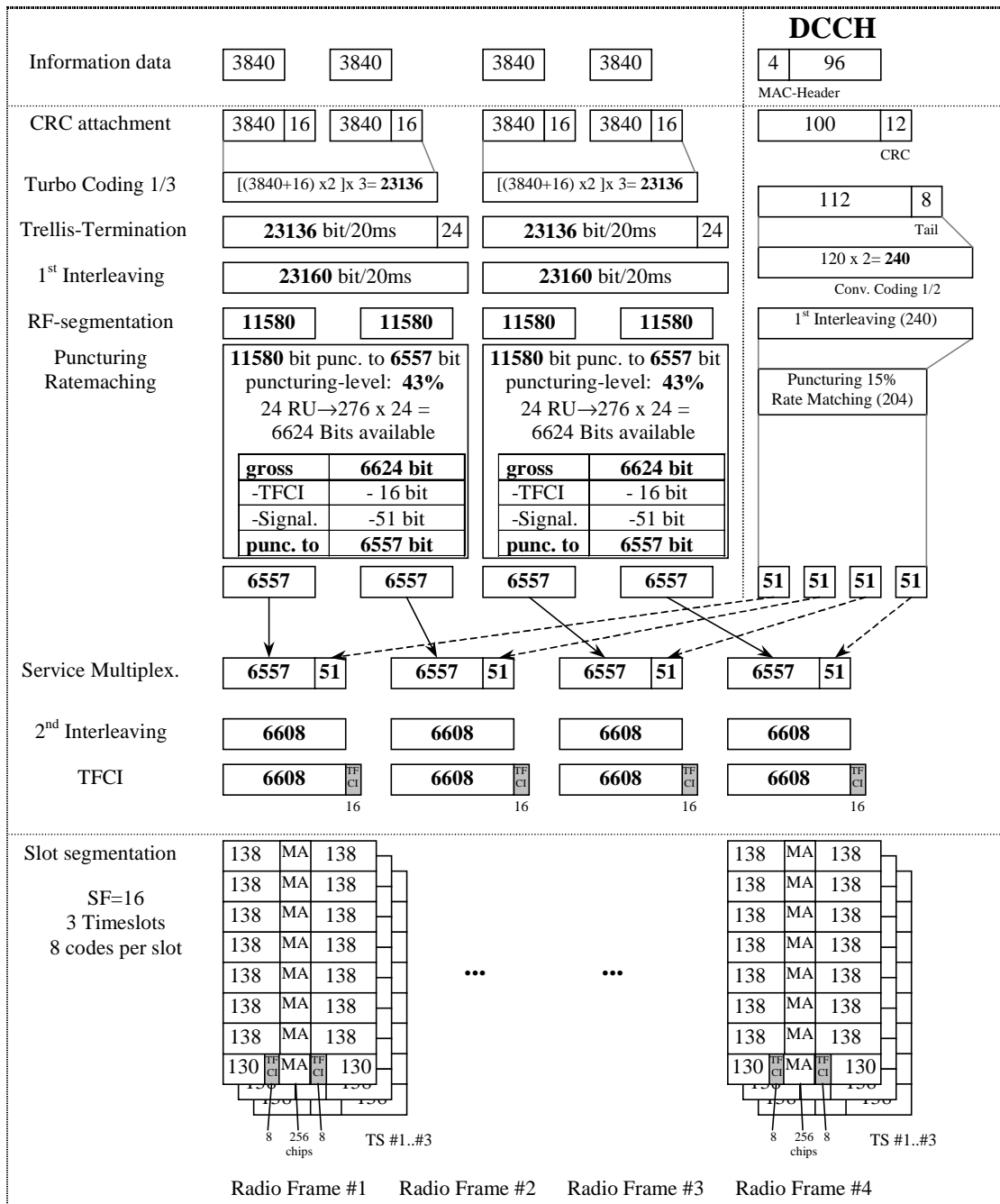


Figure A.5

A.2.5.2 1.28 Mcps TDD Option

Table A.5A

Parameter	Value
Information data rate	384 kbps
RU's allocated	4TS (10*SF16) = 40RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	16 Bit/user/10ms
TFCI	64 Bit/user/10ms
Synchronisation Shift (SS)	16 Bit/user/10ms
Inband signalling DCCH	max.2 kbps
Puncturing level at Code rate: 1/3 <u>DCH of the DTCH</u> / 1/2 <u>DCH of the DCCH</u>	41% / 12%

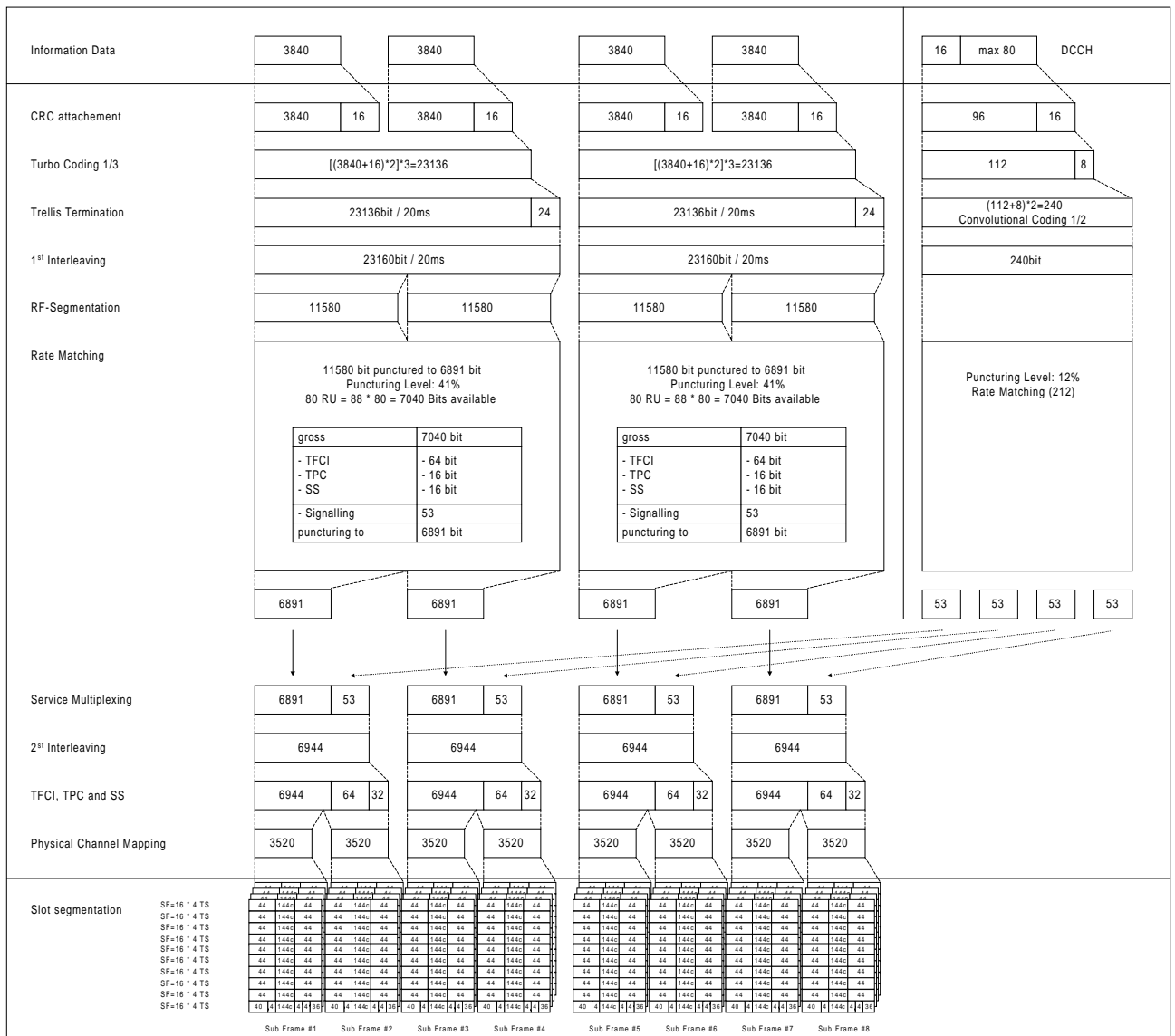


Figure A.5A

A.2.6 BCH reference measurement channel

[mapped to 1 code SF16]

A.2.6.1 3.84 Mcps TDD Option

Table A.6

Parameter	Value
Information data rate:	12.3 kbps
RU's allocated	1 RU
Midamble	512 chips
Interleaving	20 ms
Power control	0 bit
TFCI	0 bit
Puncturing level	10%

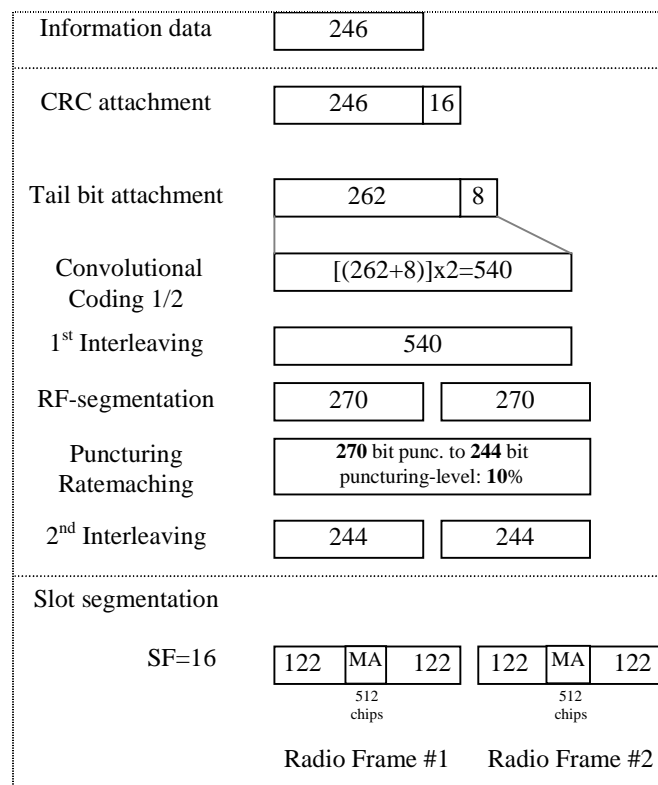


Figure A.6

A.2.6.2 1.28 Mcps TDD Option

Table A.6A

Parameter	Value
Information data rate:	12.3 kbps
RU's allocated	2 RU
Midamble	144 chips
Interleaving	20 ms
Power control	0 bit
TFCI	0 bit
Puncturing level	13%

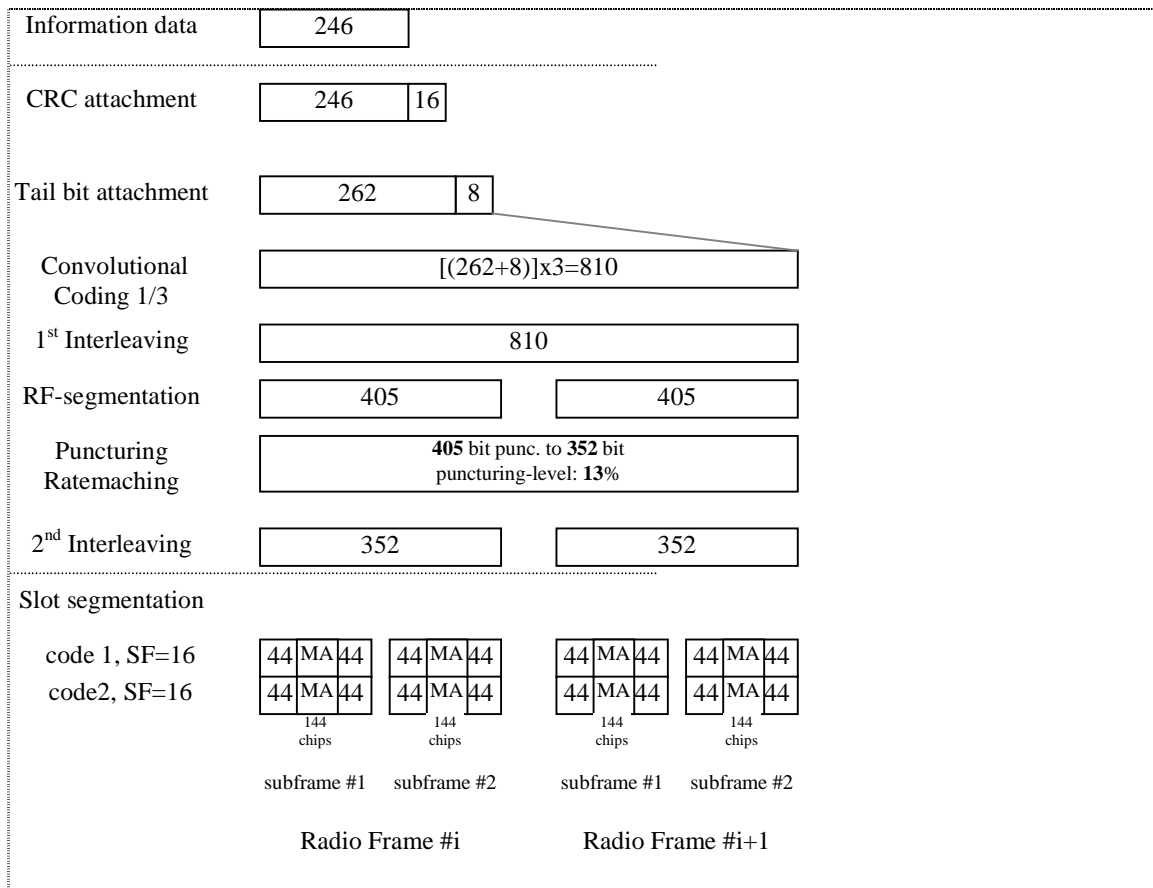


Figure A.6A

A.2.7 UL multi code reference measurement channel (12.2 kbps)

A.2.7.1 3.84 Mcps TDD Option

Table A.7

Parameter	Value
Information data rate	12.2 kbps
RU's allocated	2 RU
Midamble	512 chips
Interleaving	20 ms
Power control	2 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate 1/3 : DCH of the DTCH / DCH of the DCCH	5% / 0 %

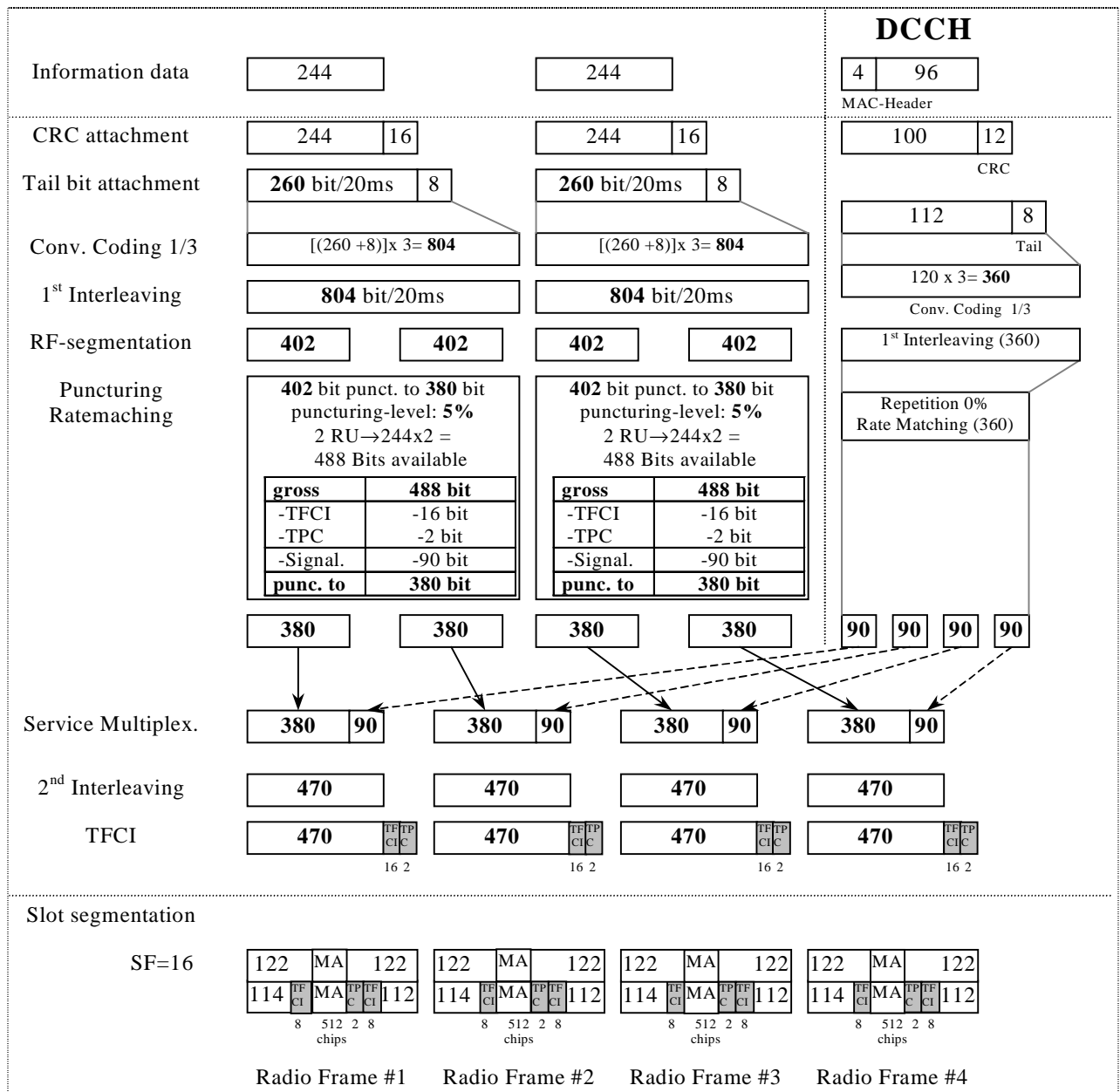


Figure A.7

A.2.7.2 1.28 Mcps TDD Option

Table A.7A

Parameter	Value
Information data rate	12.2 kbps
RU's allocated	1TS (2*SF16) = 2RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
4 Bit reserved for future use (place of SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate 1/3: <u>DCH of the DTCH / DCH of the DCCH</u>	33% / 33%

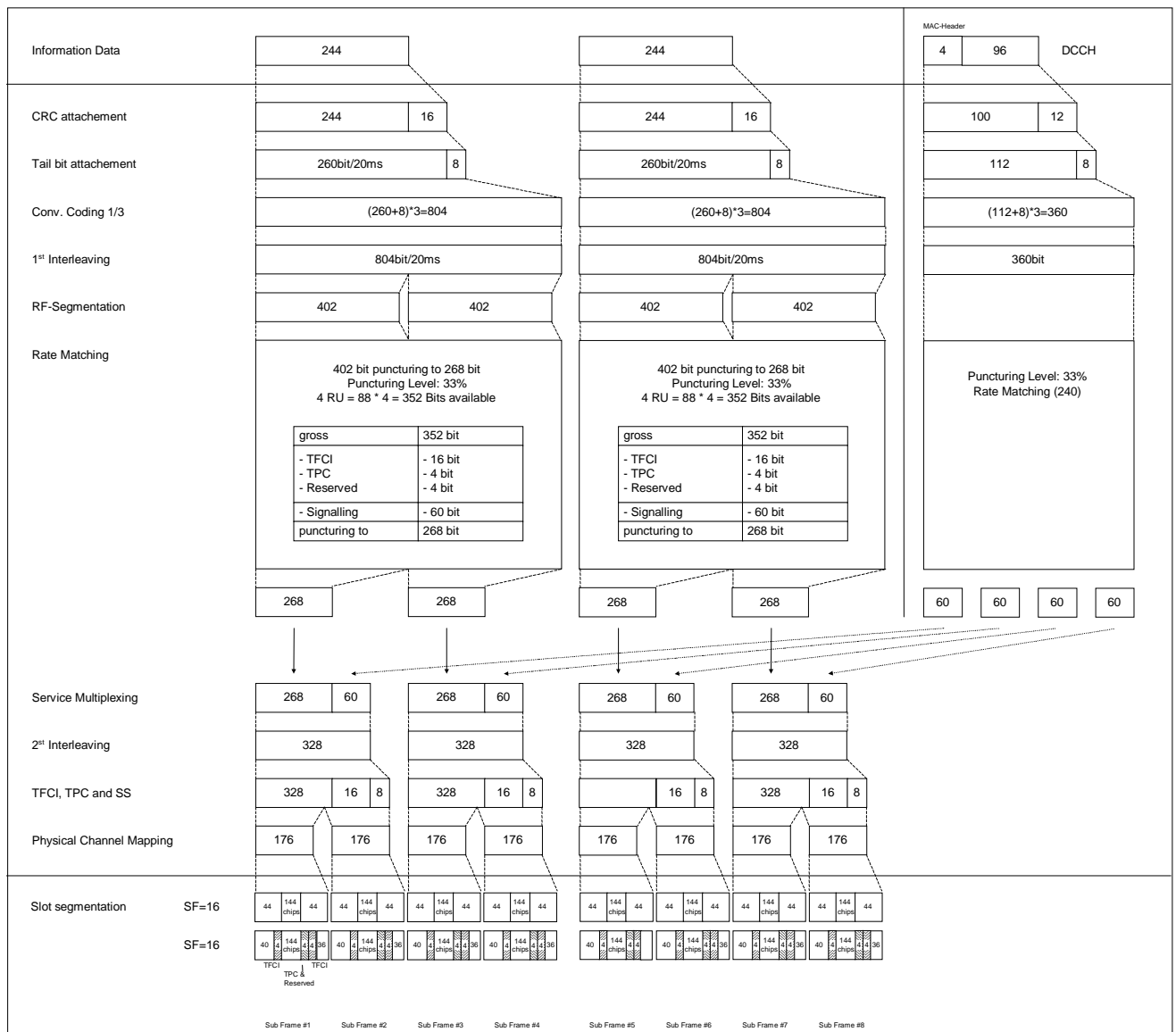


Figure A.7A

A.2.8 DL reference measurement channel (2 Mbps)

A.2.8.1 3.84 Mcps TDD Option

Table A.8

Parameter	Value
Information data rate	2048 kbps
RU's allocated	16*12TS = 192RU
Midamble	256 chips
Interleaving	10 ms
Power control	0 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate 1/3 : DCH of the DICH / DCH of the DCCH	13.9% / 0%

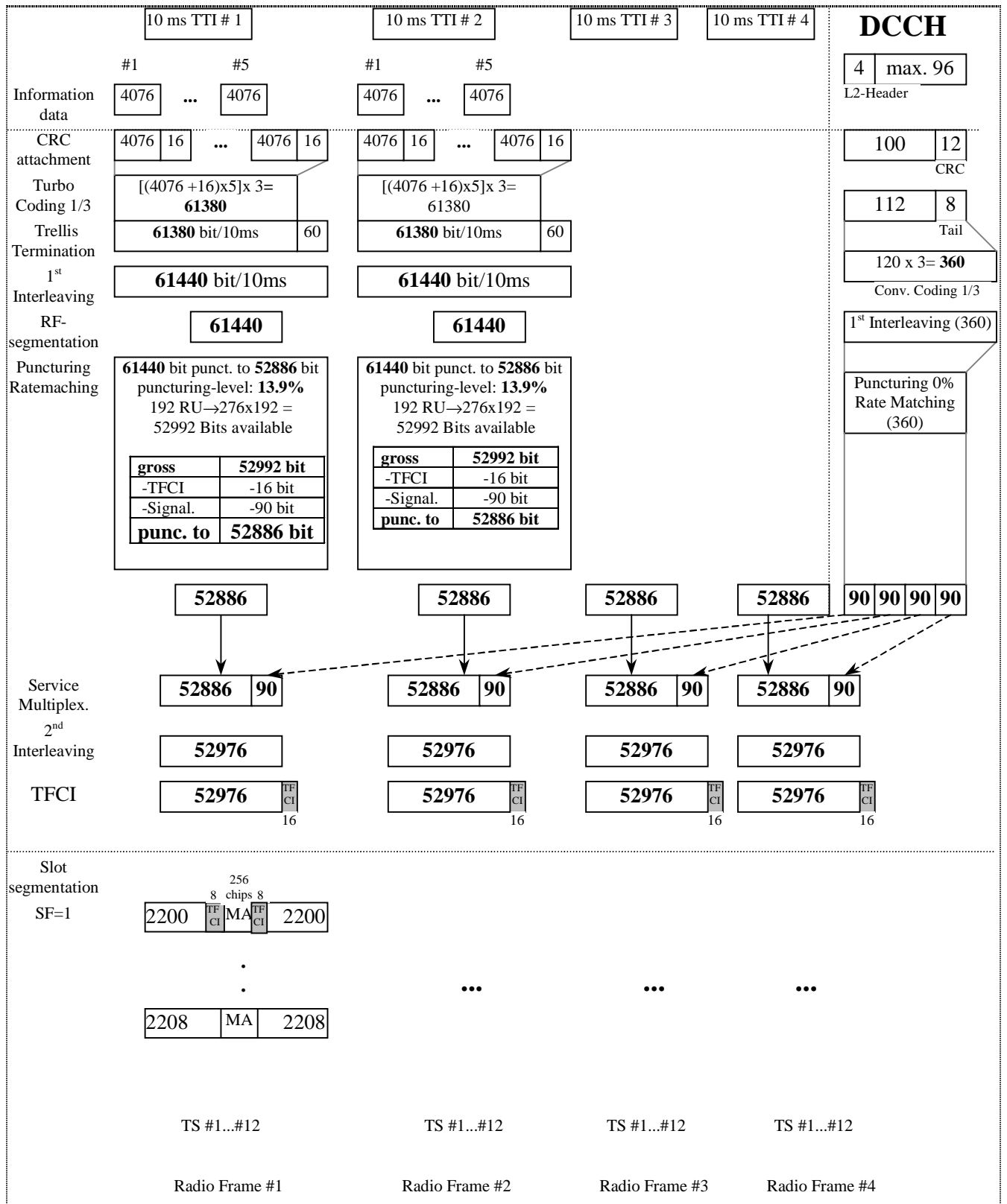


Figure A.8

A.2.8.2 1.28 Mcps TDD Option

Table A.8A

Parameter	Value
Information data rate	2048 kbps
RU's allocated	5TS (1*SF1) = 80RU/5ms
Midamble	144
Interleaving	10 ms
Power control (TPC)	6 Bit/user/10ms
TFCI	48 Bit/user/10ms
Synchronisation Shift (SS)	6 Bit/user/10ms
Inband signalling DCCH	no
Coding	no
Modulation	8PSK

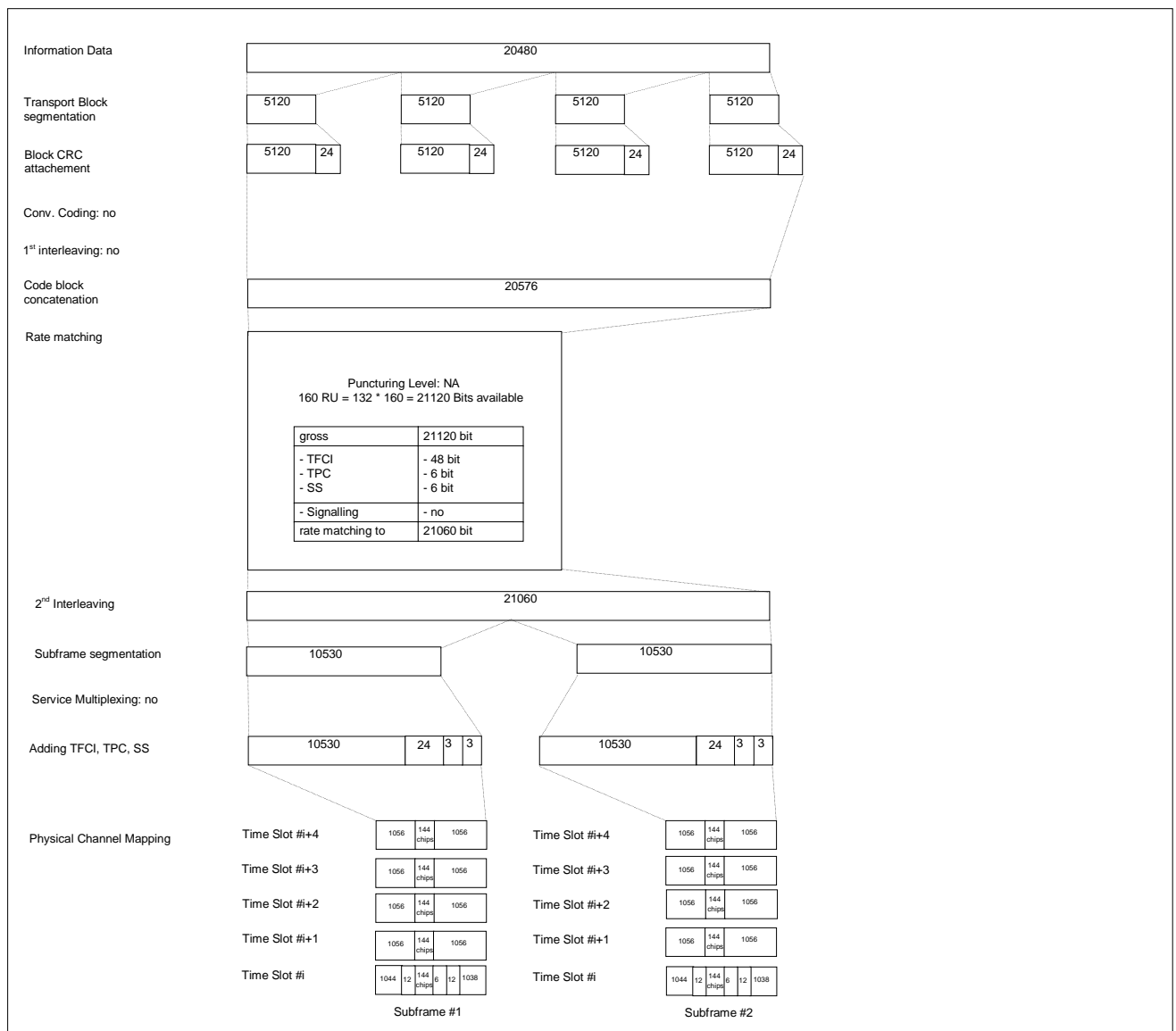


Figure A.8A

CHANGE REQUEST

⌘ **25.102 CR 131** ⌘ rev ⌘ Current version: **5.2.0** ⌘

For [HELP](#) on using this form, see bottom of this page or look at the pop-up text over the ⌘ symbols.

Proposed change affects: UICC apps ME Radio Access Network Core Network

Title:	⌘ Name correction of logical and transport channels		
Source:	⌘ RAN WG4		
Work item code:	⌘ TEI4	Date:	⌘ 26/11/2002
Category:	⌘ A	Release:	⌘ Rel-5
	Use <u>one</u> of the following categories: F (correction) A (corresponds to a correction in an earlier release) B (addition of feature), C (functional modification of feature) D (editorial modification) Detailed explanations of the above categories can be found in 3GPP TR 21.900 .		Use <u>one</u> of the following releases: 2 (GSM Phase 2) R96 (Release 1996) R97 (Release 1997) R98 (Release 1998) R99 (Release 1999) Rel-4 (Release 4) Rel-5 (Release 5) Rel-6 (Release 6)

Reason for change:	⌘ No clear distinction between logical and transport channels. Puncturing levels and code rates are different for the data and control part of the transport channel.
Summary of change:	⌘ Referencing the DCH of the DTCH and the DCH of the DCCH instead of DCCH and DCH in general for puncturing levels and coding rates.
Consequences if not approved:	⌘ Incorrect description and inconsistency with respect to WG1 specifications. <u>Isolated impact analysis:</u> The correction has no impact on UE-BS interworking.

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Other specs affected:	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="width: 20px; text-align: center;">Y</td> <td style="width: 20px; text-align: center;">N</td> </tr> <tr> <td style="text-align: center;">X</td> <td></td> </tr> <tr> <td></td> <td style="text-align: center;">X</td> </tr> <tr> <td></td> <td style="text-align: center;">X</td> </tr> </table> Other core specifications Test specifications O&M Specifications	Y	N	X			X		X	⌘ 25.105 in CR130	
Y	N										
X											
	X										
	X										
Other comments:	⌘ Equivalent CRs in other Releases: CR130 cat. F to 25.102 v4.6.0										

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Annex A (normative): Measurement channels

A.1 General

A.2 Reference measurement channel

A.2.1 UL reference measurement channel (12.2 kbps)

A.2.1.1 3.84 Mcps TDD Option

Table A.1

Parameter	Value
Information data rate	12.2 kbps
RU's allocated	2 RU
Midamble	512 chips
Interleaving	20 ms
Power control	2 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate 1/3 : DCH of the DTCH / DCH of the DCCH	10% / 0%

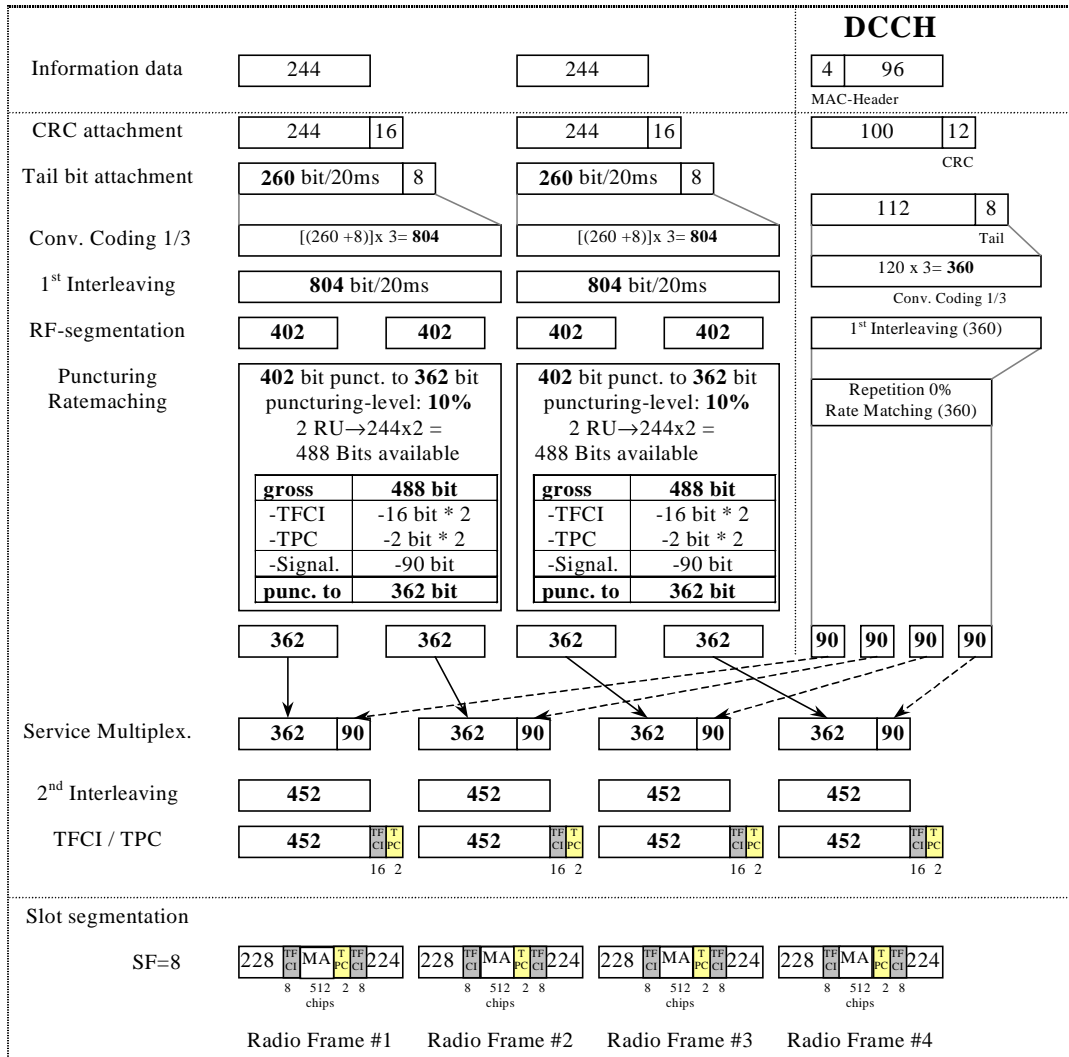


Figure A.1

A.2.1.2 1.28 Mcps TDD Option

Table A.1A

Parameter	Value
Information data rate	12.2 kbps
RU's allocated	1TS (1*SF8) = 2RU/5ms
Midamble	144
Interleaving	20 ms
Power control	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
4 Bit reserved for future use (place of SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate 1/3 : <u>DCH of the DTCH</u> / <u>DCH of the DCCH</u>	33% / 33%

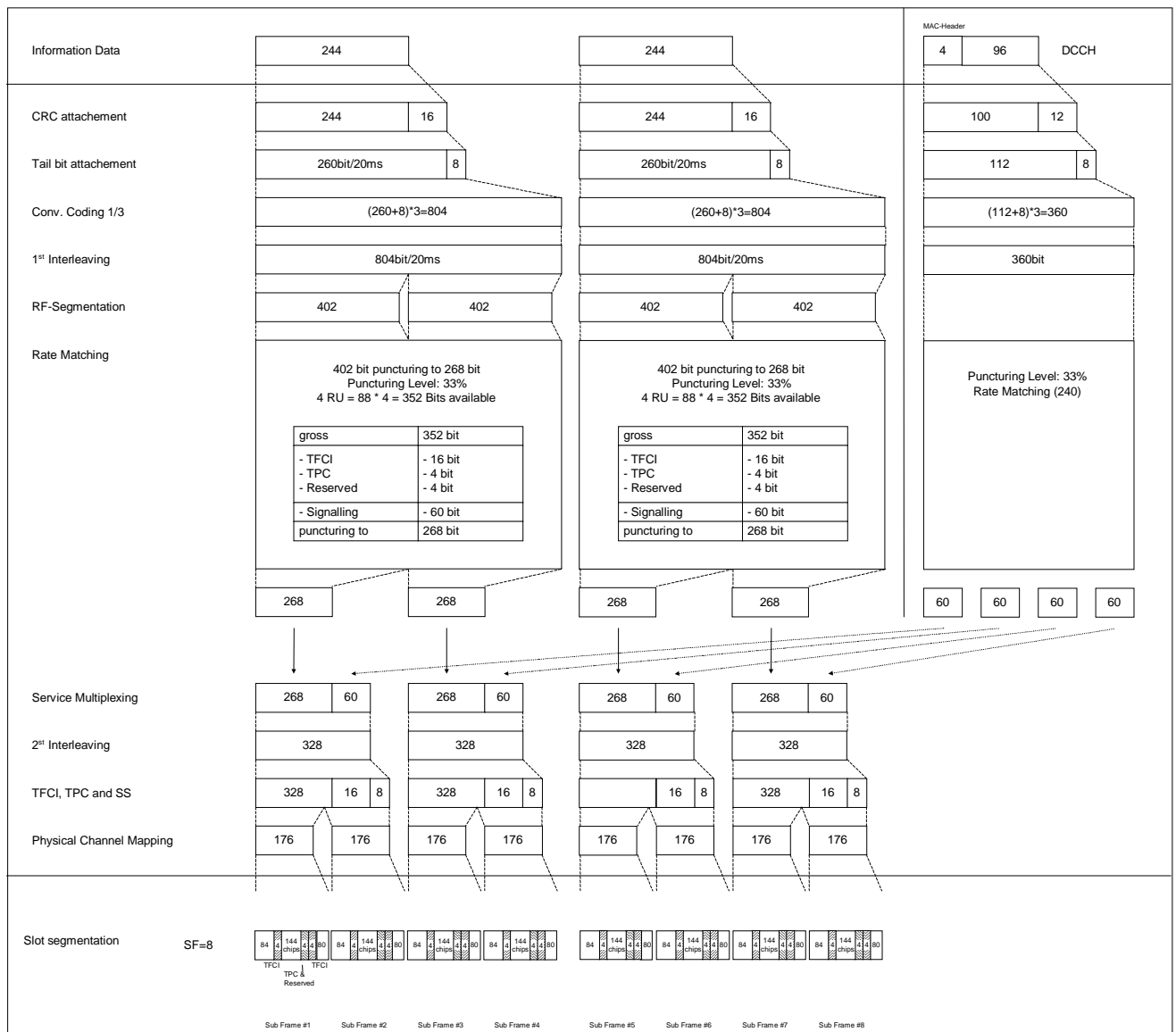


Figure A.1A

A.2.2 DL reference measurement channel (12.2 kbps)

A.2.2.1 3.84 Mcps TDD Option

Table A.2

Parameter	Value
Information data rate	12.2 kbps
RU's allocated	2 RU
Midamble	512 chips
Interleaving	20 ms
Power control	0 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate 1/3 : DCH of the DICH / DCH of the DCCH	5% / 0 %

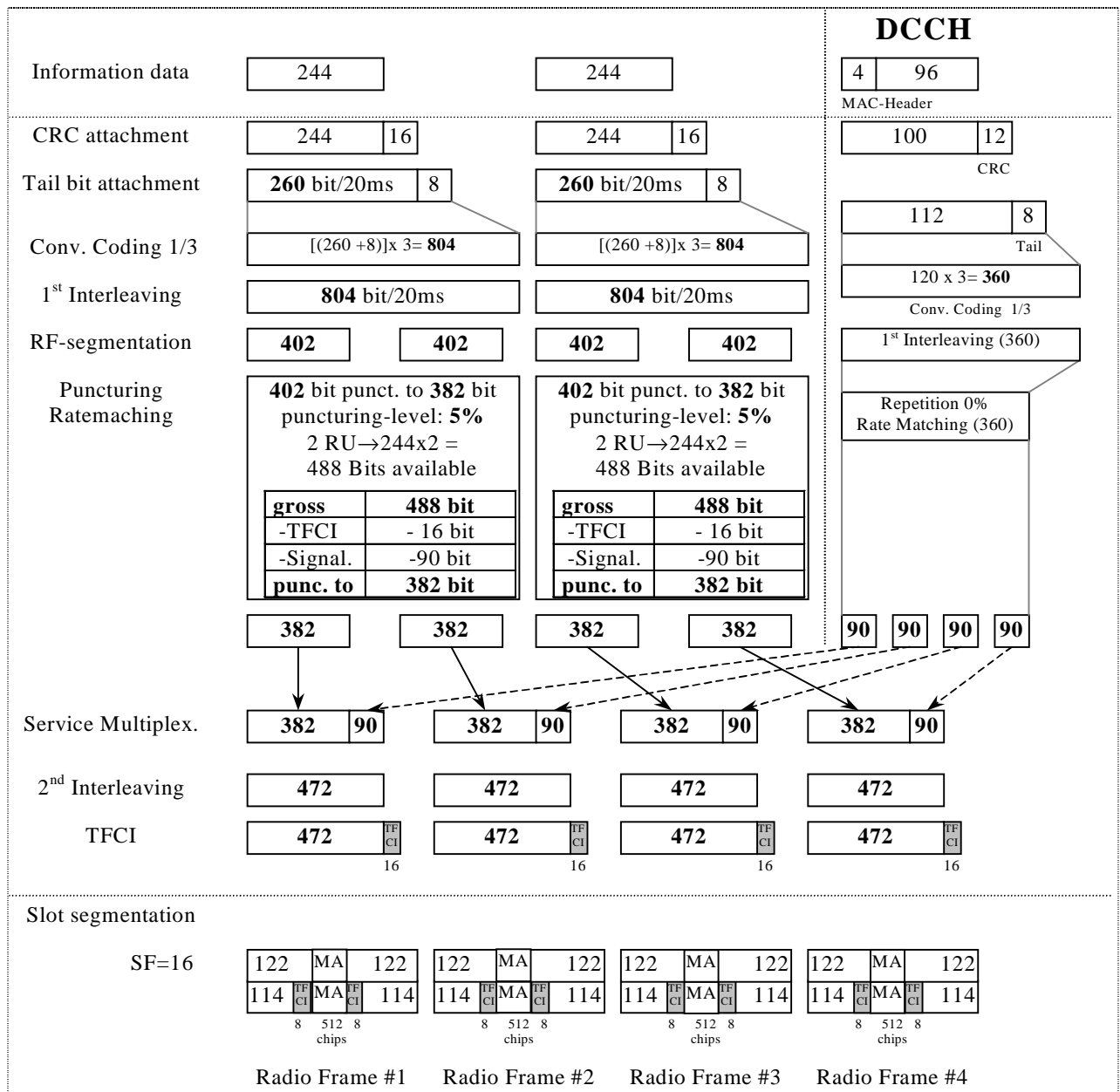


Figure A.2

A.2.2.2 1.28 Mcps TDD Option

Table A.2A

Parameter	Value
Information data rate	12.2 kbps
RU's allocated	1TS (2*SF16) = 2RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
Synchronisation Shift (SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate 1/3: <u>DCH of the DTCH / DCH of the DCCH</u>	33% / 33%

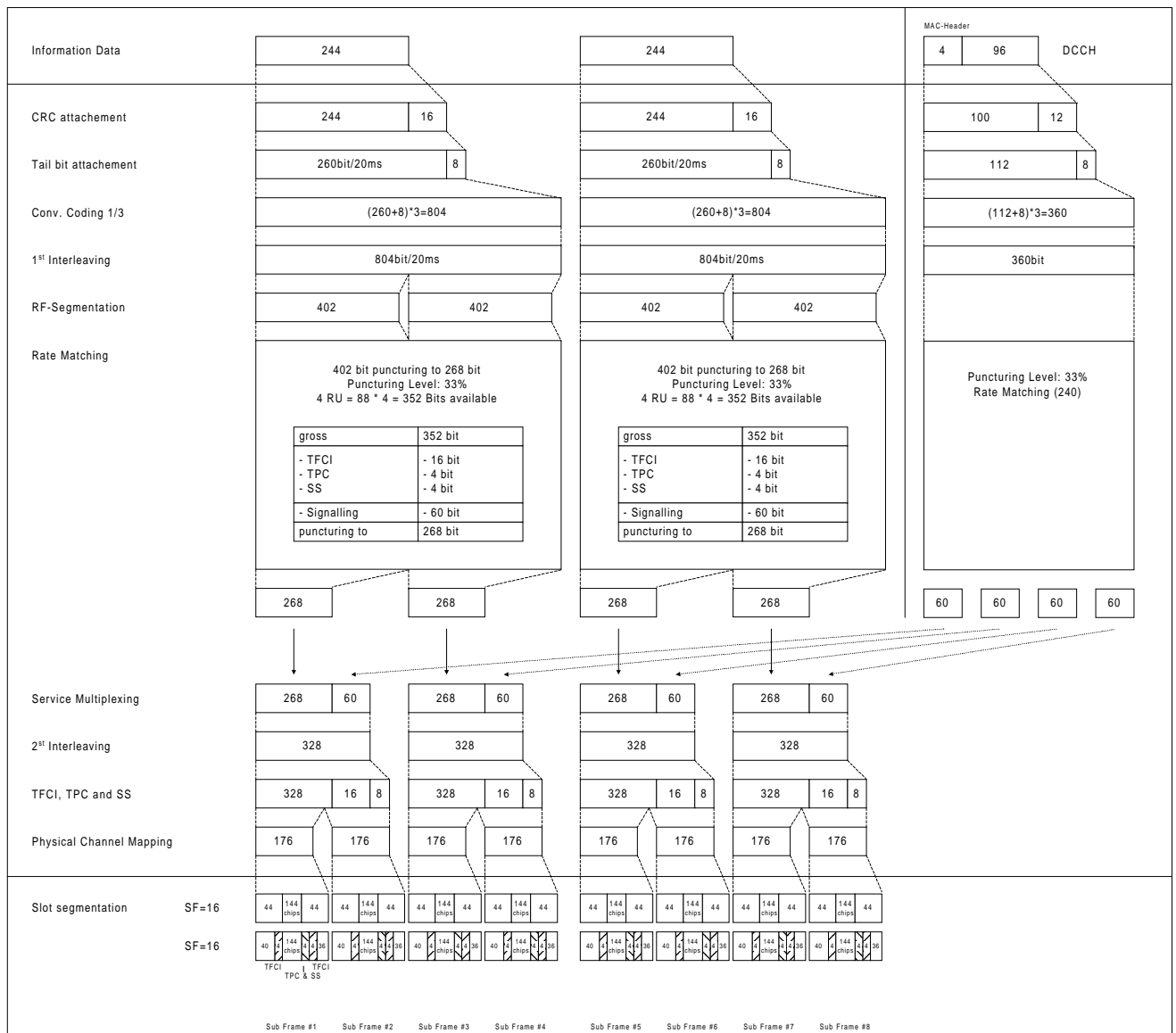


Figure A.2A

A.2.3 DL reference measurement channel (64 kbps)

A.2.3.1 3.84 Mcps TDD Option

Table A.3

Parameter	Value
Information data rate	64 kbps
RU's allocated	5 codes SF16 = 5RU
Midamble	512 chips
Interleaving	20 ms
Power control	0 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate : 1/3 DCH of the DTCH / 1/2 DCH of the DCCH	41.1% / 10%

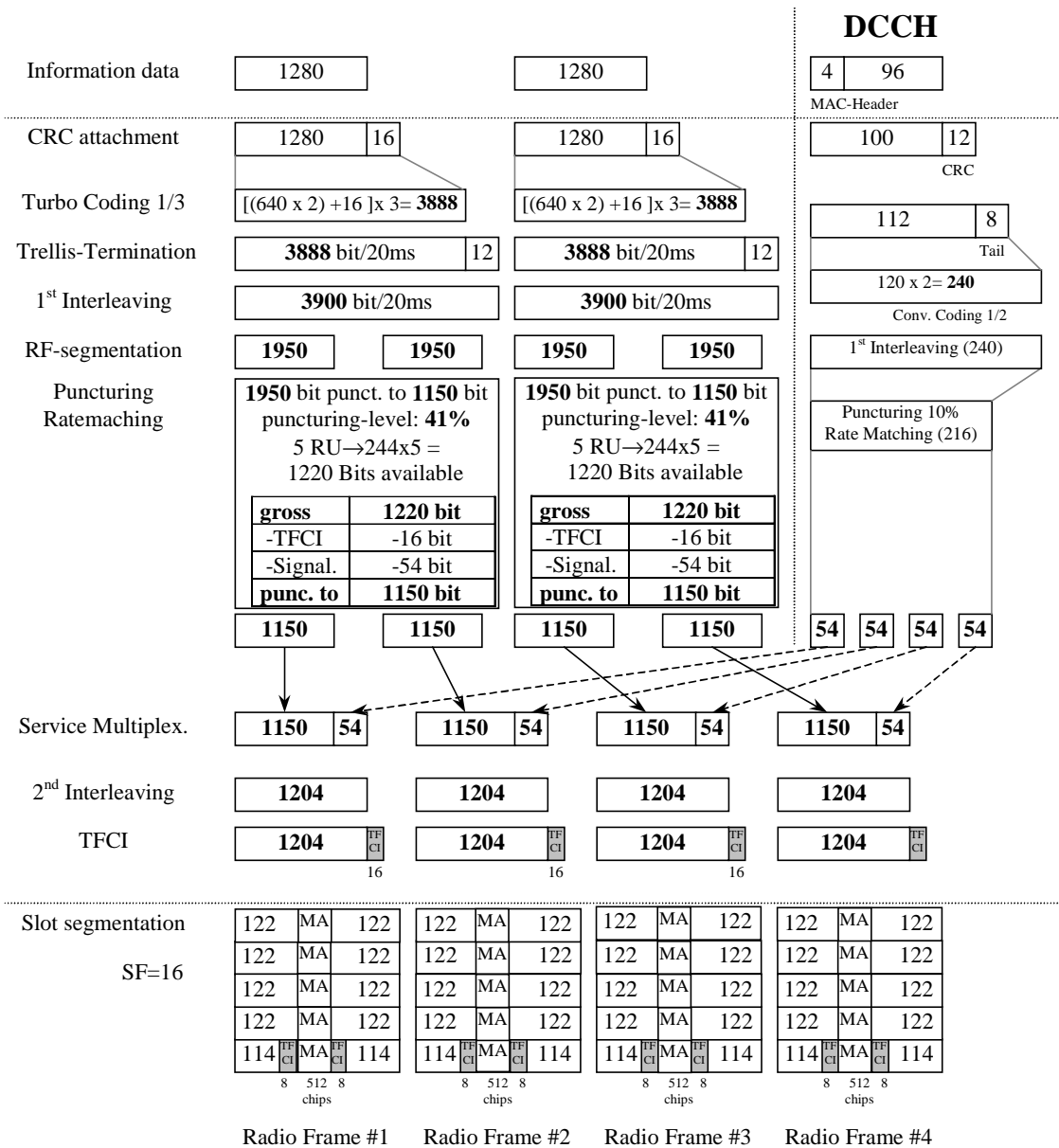


Figure A.3

A.2.3.2 1.28 Mcps TDD Option

Table A.3A

Parameter	Value
Information data rate	64 kbps
RU's allocated	1TS (8*SF16) = 8RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
Synchronisation Shift (SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate: 1/3 DCH of the DTCH / 1/2 DCH of the DCCH	32% / 0

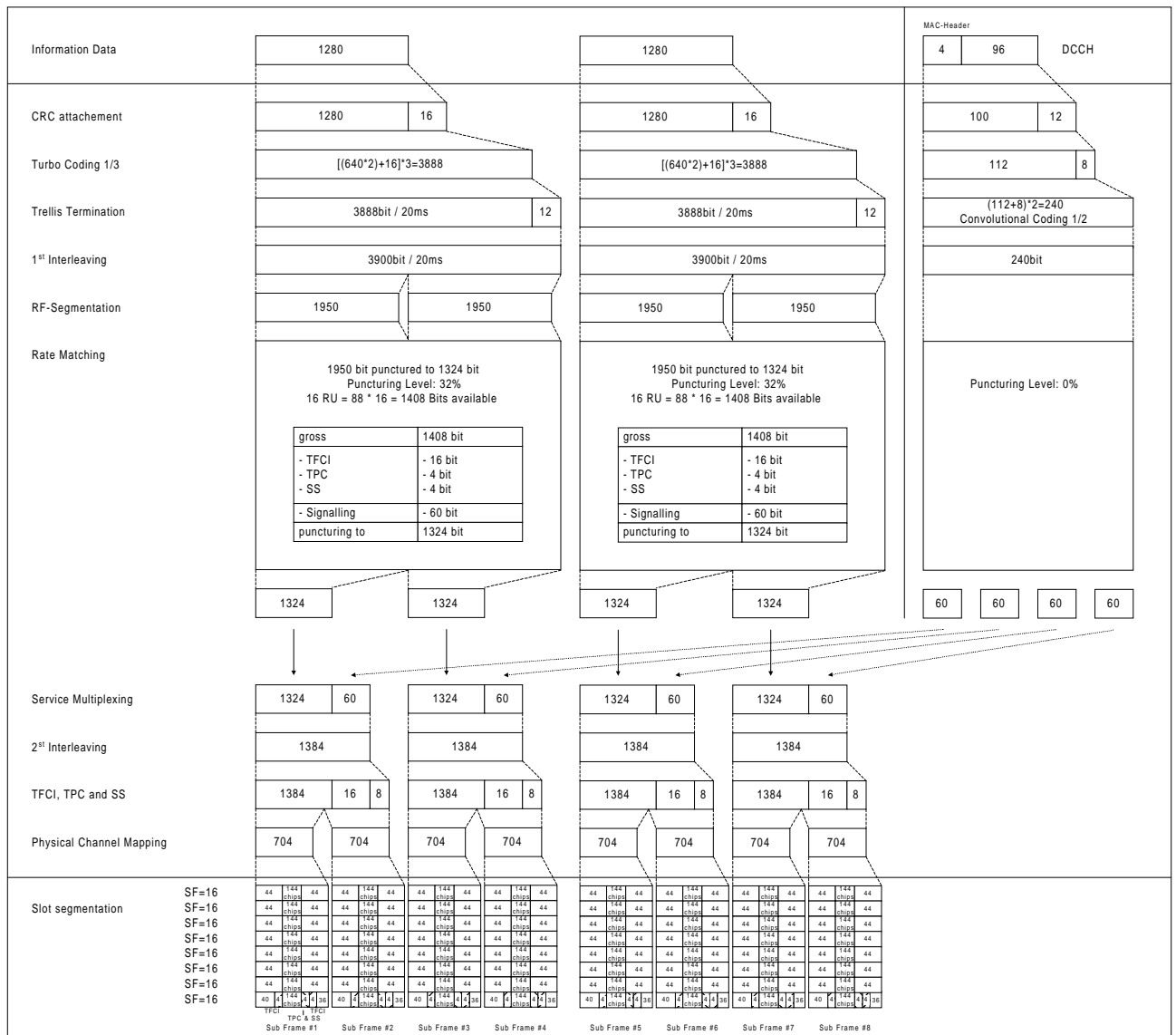


Figure A.3A

A.2.4 DL reference measurement channel (144 kbps)

A.2.4.1 3.84 Mcps TDD Option

Table A.4

Parameter	Value
Information data rate	144 kbps
RU's allocated	9 codes SF16 = 9RU
Midamble	256 chips
Interleaving	20 ms
Power control	0 Bit/user
TFCI	16 Bit/user
Inband signalling DCCCH	2 kbps
Puncturing level at Code rate: 1/3 <u>DCH of the DICH</u> / 1/2 <u>DCH of the DCCH</u>	44.5% / 16.6%

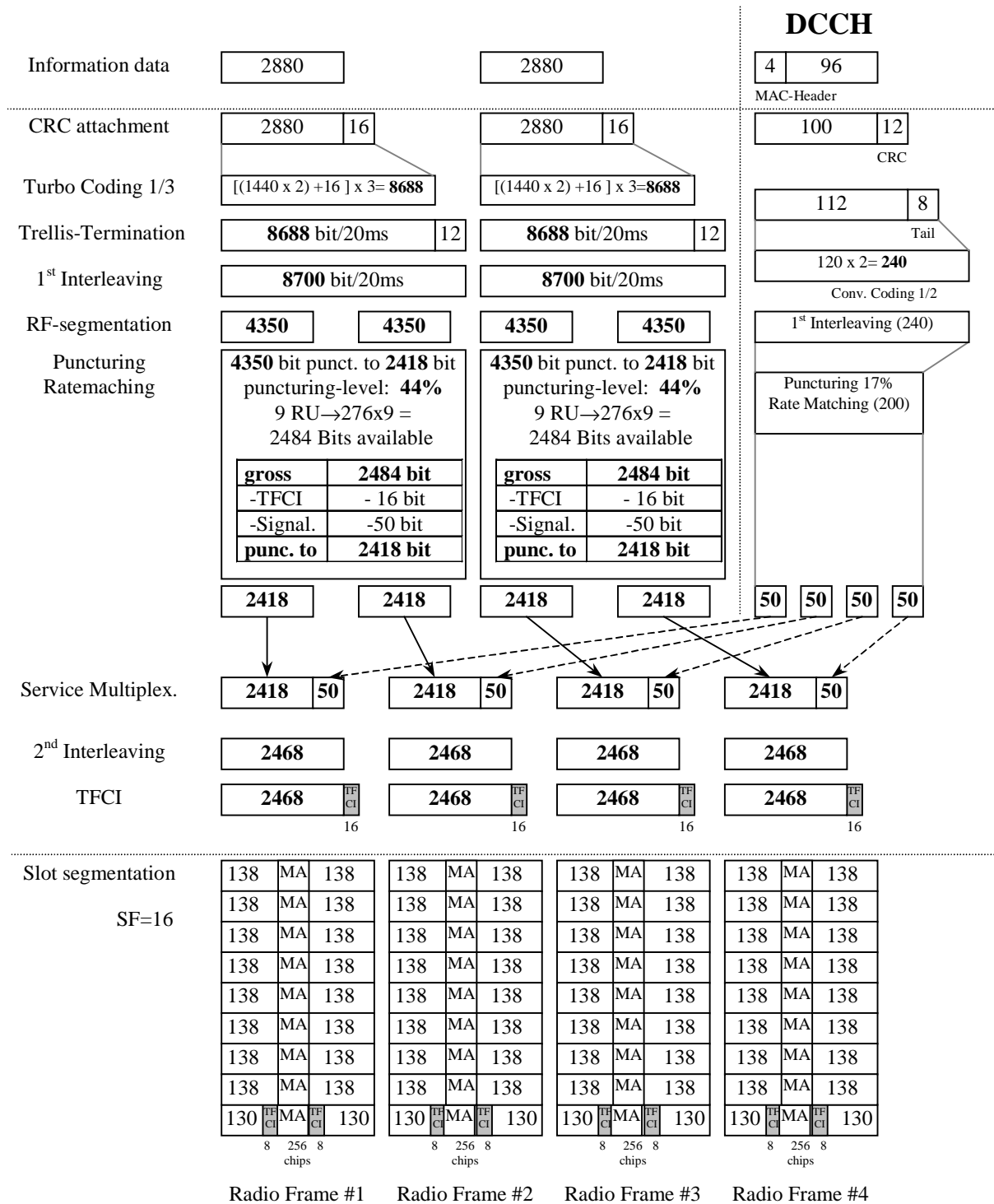


Figure A.4

A.2.4.2 1.28 Mcps TDD Option

Table A.4A

Parameter	Value
Information data rate	144 kbps
RU's allocated	2TS (8*SF16) = 16RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	8 Bit/user/10ms
TFCI	32 Bit/user/10ms
Synchronisation Shift (SS)	8 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate: 1/3 <u>DCH of the DCH</u> / 1/2 <u>DCH of the DCCH</u>	38% / 7%

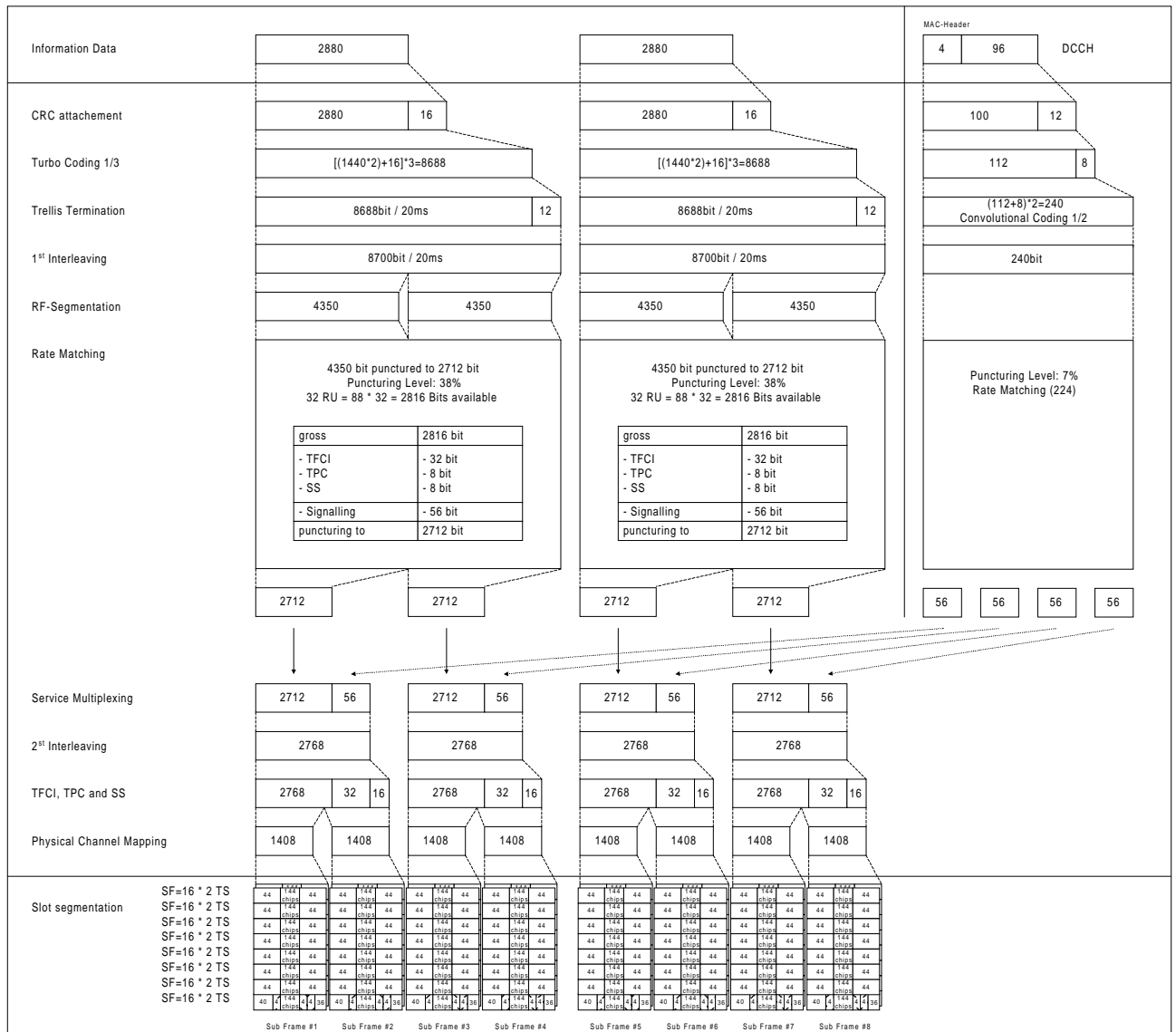


Figure A.4A

A.2.5 DL reference measurement channel (384 kbps)

A.2.5.1 3.84 Mcps TDD Option

Table A.5

Parameter	Value
Information data rate	384 kbps
RU's allocated	8*3TS = 24RU
Midamble	256 chips
Interleaving	20 ms
Power control	0 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate : 1/3 DCH of the D T CH / 1/2 DCH of the DCCH	43.4% / 15.3%

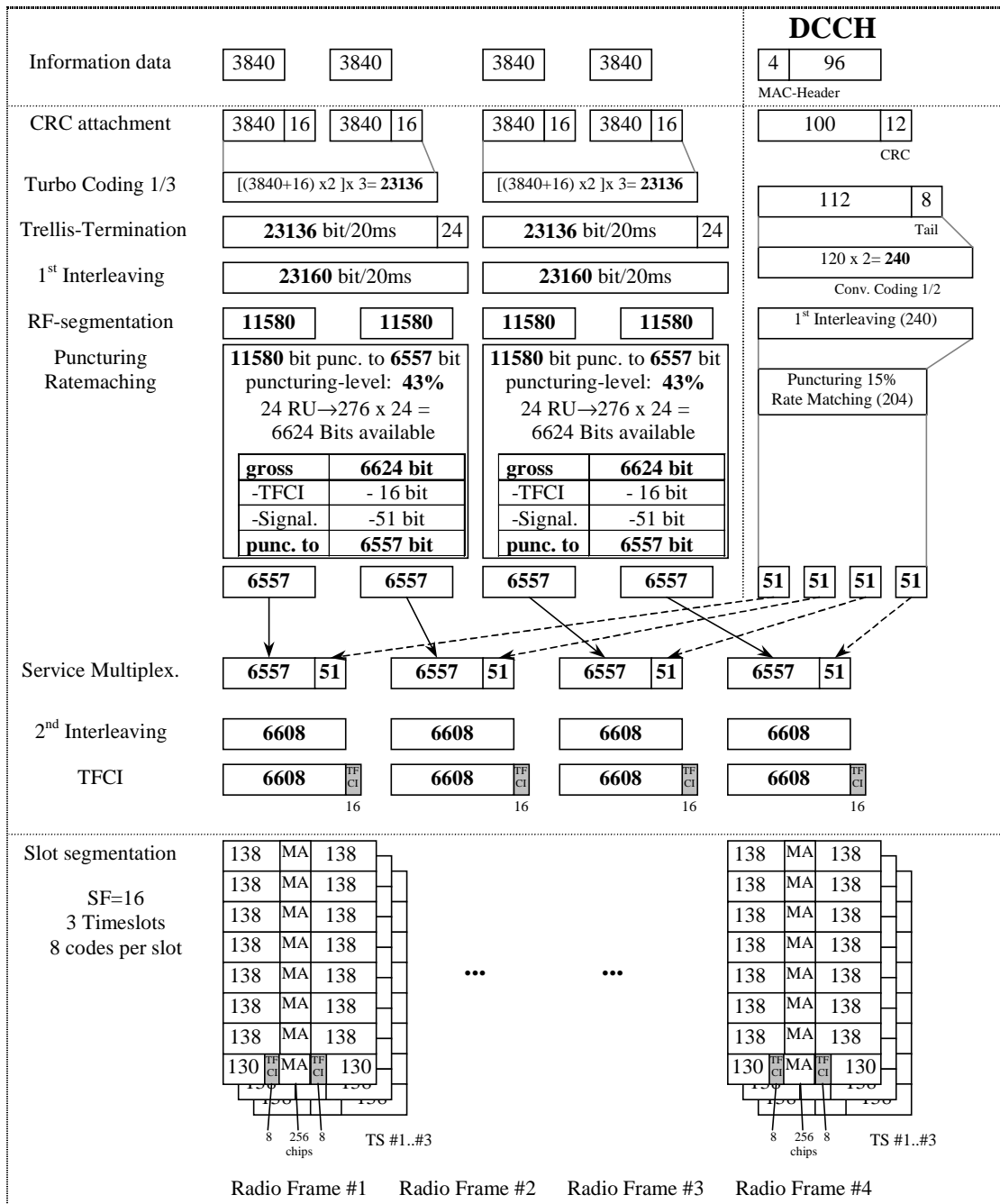


Figure A.5

A.2.5.2 1.28 Mcps TDD Option

Table A.5A

Parameter	Value
Information data rate	384 kbps
RU's allocated	4TS (10*SF16) = 40RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	16 Bit/user/10ms
TFCI	64 Bit/user/10ms
Synchronisation Shift (SS)	16 Bit/user/10ms
Inband signalling DCCH	max.2 kbps
Puncturing level at Code rate: 1/3 <u>DCH of the DTCH</u> / 1/2 <u>DCH of the DCCH</u>	41% / 12%

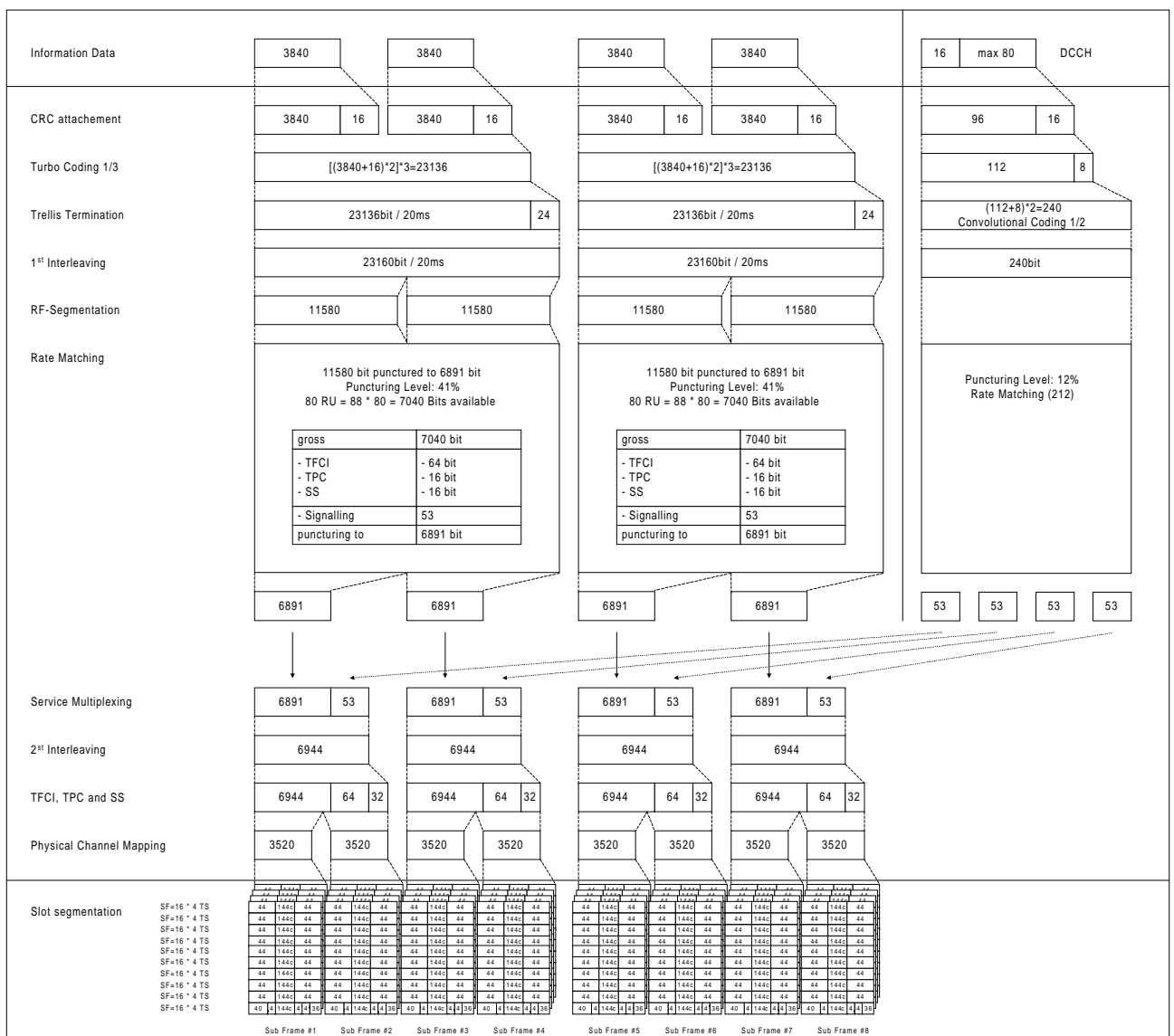


Figure A.5A

A.2.6 BCH reference measurement channel

[mapped to 1 code SF16]

A.2.6.1 3.84 Mcps TDD Option

Table A.6

Parameter	Value
Information data rate:	12.3 kbps
RU's allocated	1 RU
Midamble	512 chips
Interleaving	20 ms
Power control	0 bit
TFCI	0 bit
Puncturing level	10%

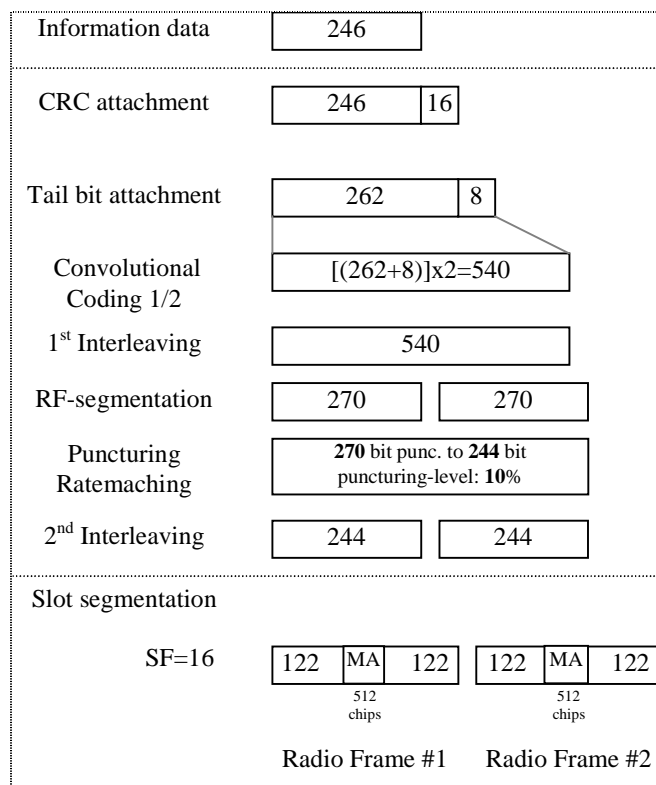


Figure A.6

A.2.6.2 1.28 Mcps TDD Option

Table A.6A

Parameter	Value
Information data rate:	12.3 kbps
RU's allocated	2 RU
Midamble	144 chips
Interleaving	20 ms
Power control	0 bit
TFCI	0 bit
Puncturing level	13%

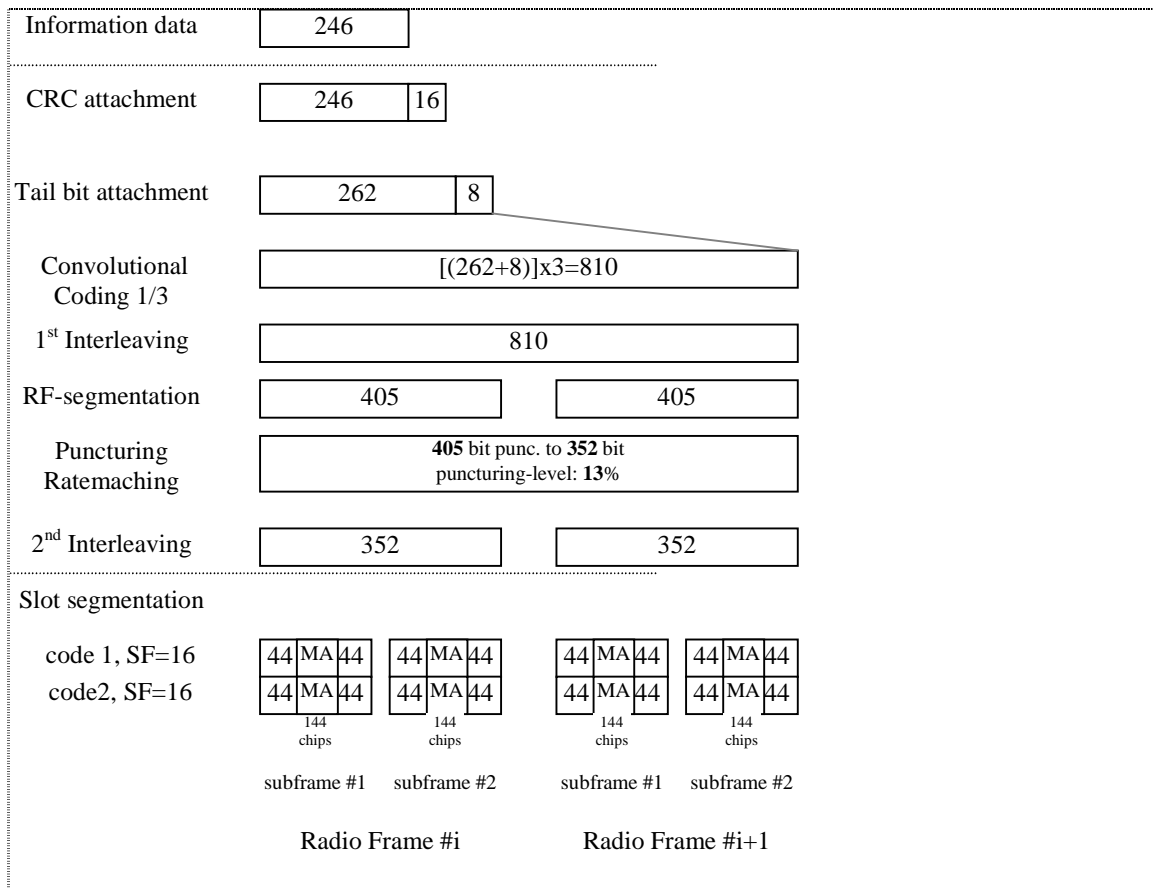


Figure A.6A

A.2.7 UL multi code reference measurement channel (12.2 kbps)

A.2.7.1 3.84 Mcps TDD Option

Table A.7

Parameter	Value
Information data rate	12.2 kbps
RU's allocated	2 RU
Midamble	512 chips
Interleaving	20 ms
Power control	2 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate 1/3 : DCH of the DTCH / DCH of the DCCH	5% / 0 %

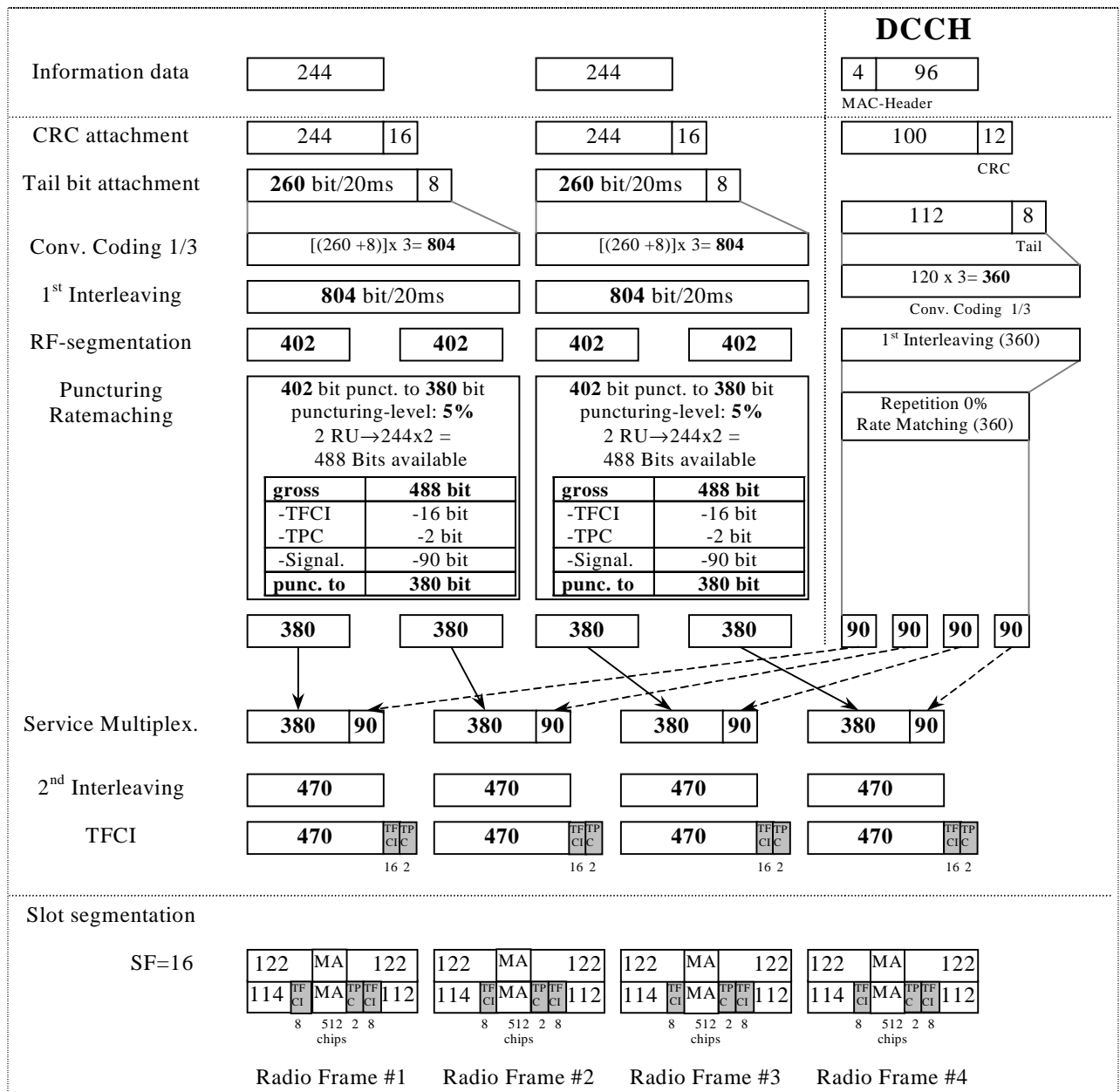


Figure A.7

A.2.7.2 1.28 Mcps TDD Option

Table A.7A

Parameter	Value
Information data rate	12.2 kbps
RU's allocated	1TS (2*SF16) = 2RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
4 Bit reserved for future use (place of SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate 1/3: <u>DCH of the DTCH / DCH of the DCCH</u>	33% / 33%

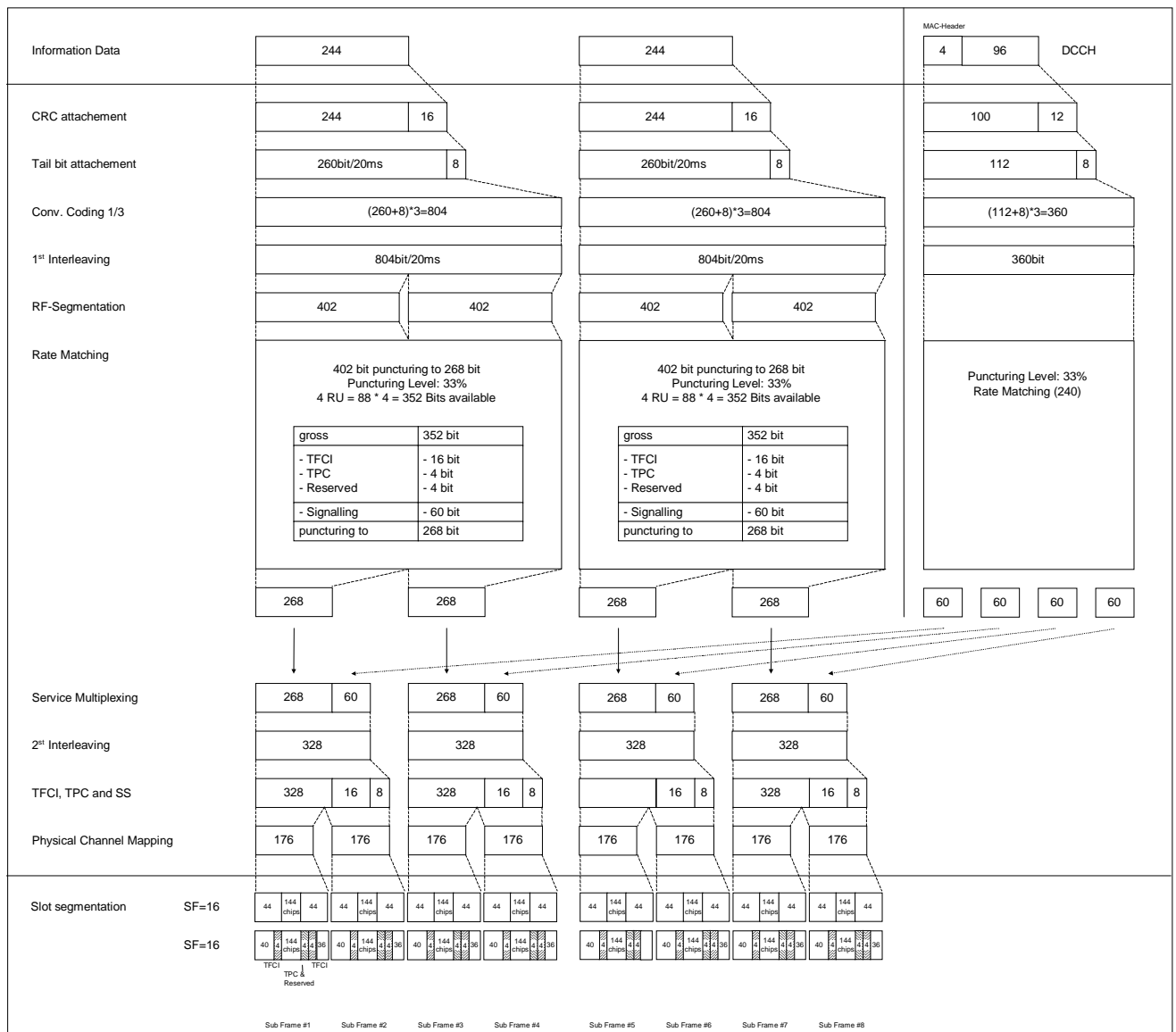


Figure A.7A

A.2.8 DL reference measurement channel (2 Mbps)

A.2.8.1 3.84 Mcps TDD Option

Table A.8

Parameter	Value
Information data rate	2048 kbps
RU's allocated	16*12TS = 192RU
Midamble	256 chips
Interleaving	10 ms
Power control	0 Bit/user
TFCI	16 Bit/user
Inband signalling DCCH	2 kbps
Puncturing level at Code rate 1/3 : DCH of the DICH / DCH of the DCCH	13.9% / 0%

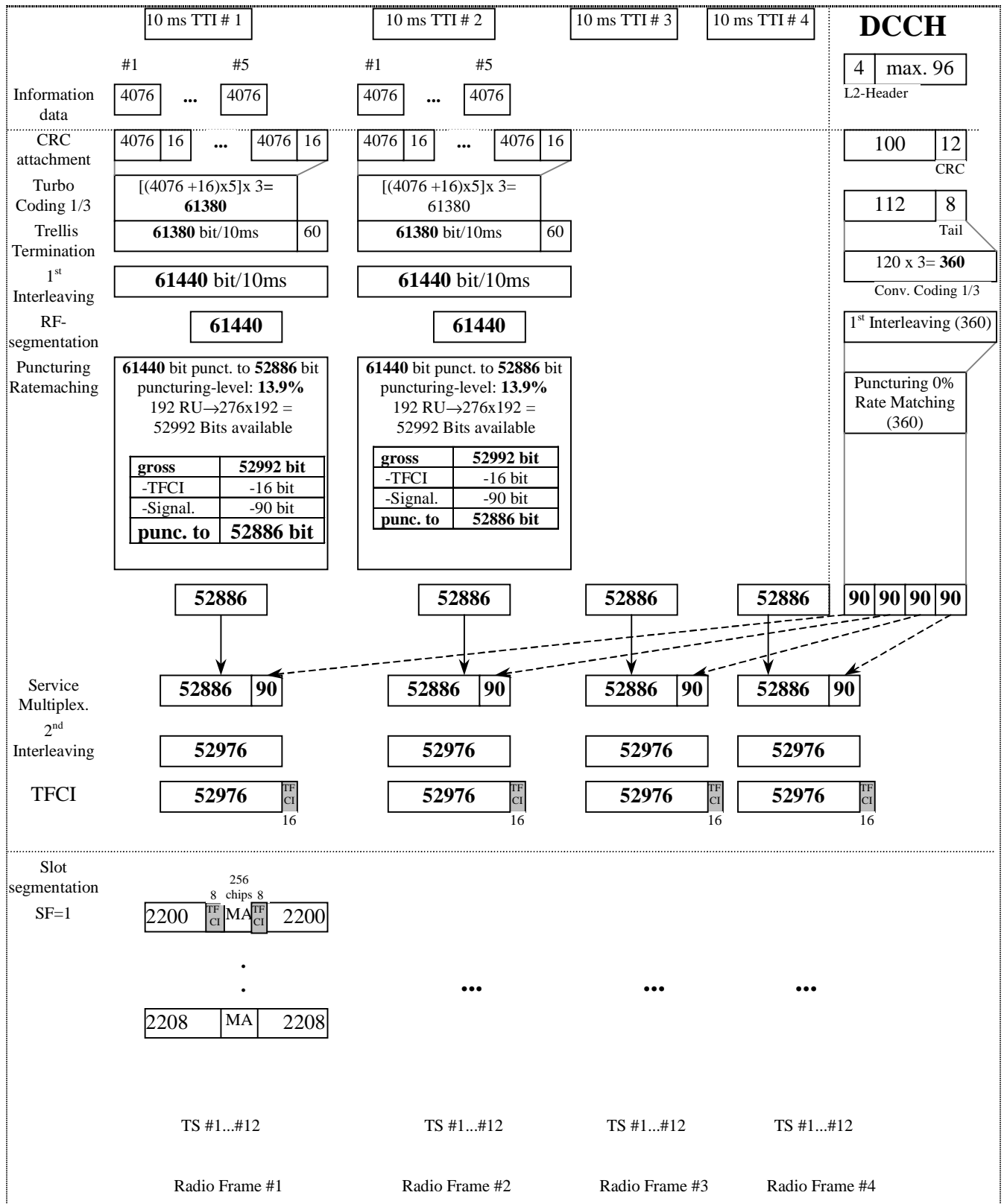


Figure A.8

A.2.8.2 1.28 Mcps TDD Option

Table A.8A

Parameter	Value
Information data rate	2048 kbps
RU's allocated	5TS (1*SF1) = 80RU/5ms
Midamble	144
Interleaving	10 ms
Power control (TPC)	6 Bit/user/10ms
TFCI	48 Bit/user/10ms
Synchronisation Shift (SS)	6 Bit/user/10ms
Inband signalling DCCH	no
Coding	no
Modulation	8PSK

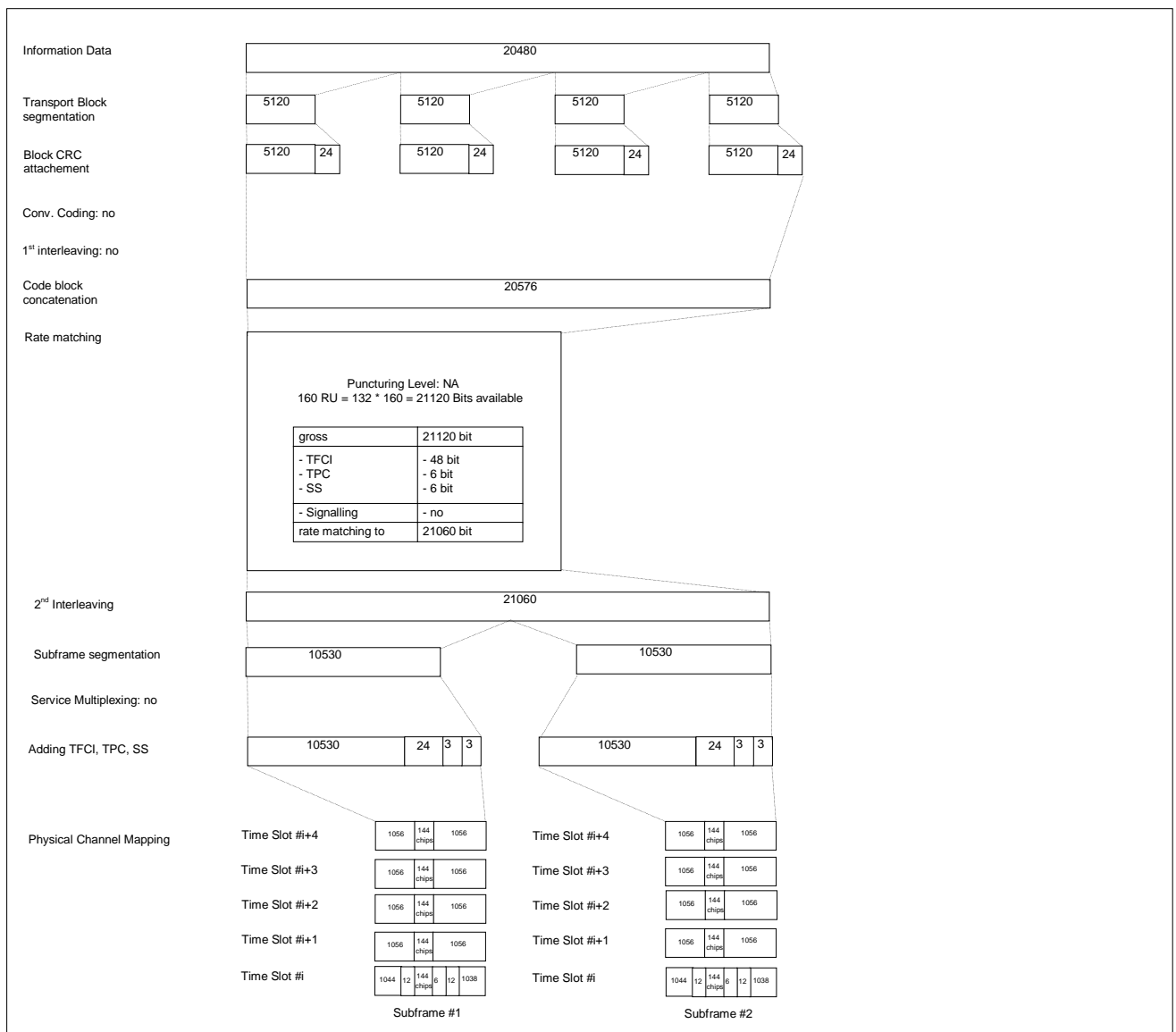


Figure A.8A

A.3 HSDPA reference measurement channels

A.3.1 void

A.3.2 HSDPA reference measurement channels for 1.28 Mcps TDD option

A.3.2.1 Reference measurement channels for 1.4 Mbps UE class

A.3.2.1.1 QPSK modulation scheme

Table [A.9]

Parameter	Value
Maximum information data rate	528 kbps
RU's allocated	4TS (10*SF16) = 40RU/5ms
Midamble	144 chips
Puncturing level at code rate 1/3 : first stage/second stage	12% / 50%

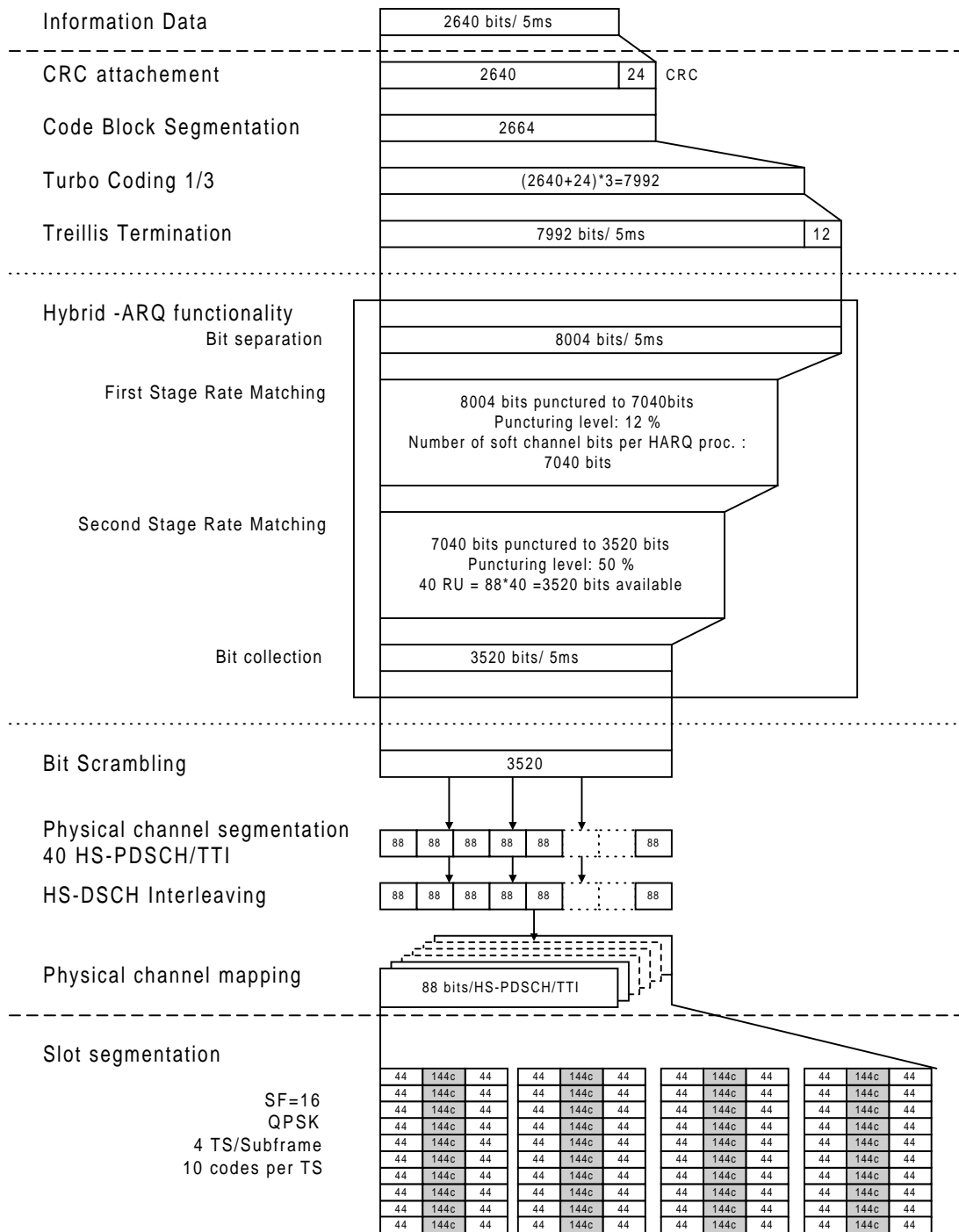


Figure [A.9]

A.3.2.1.2 16QAM modulation scheme

Table [A.10]

Parameter	Value
Maximum information data rate	750 kbps
RU's allocated	4TS (9*SF16) = 36RU/5ms
Midamble	144 chips
Puncturing level at code rate 1/3 : first stage/second stage	38% / 10%

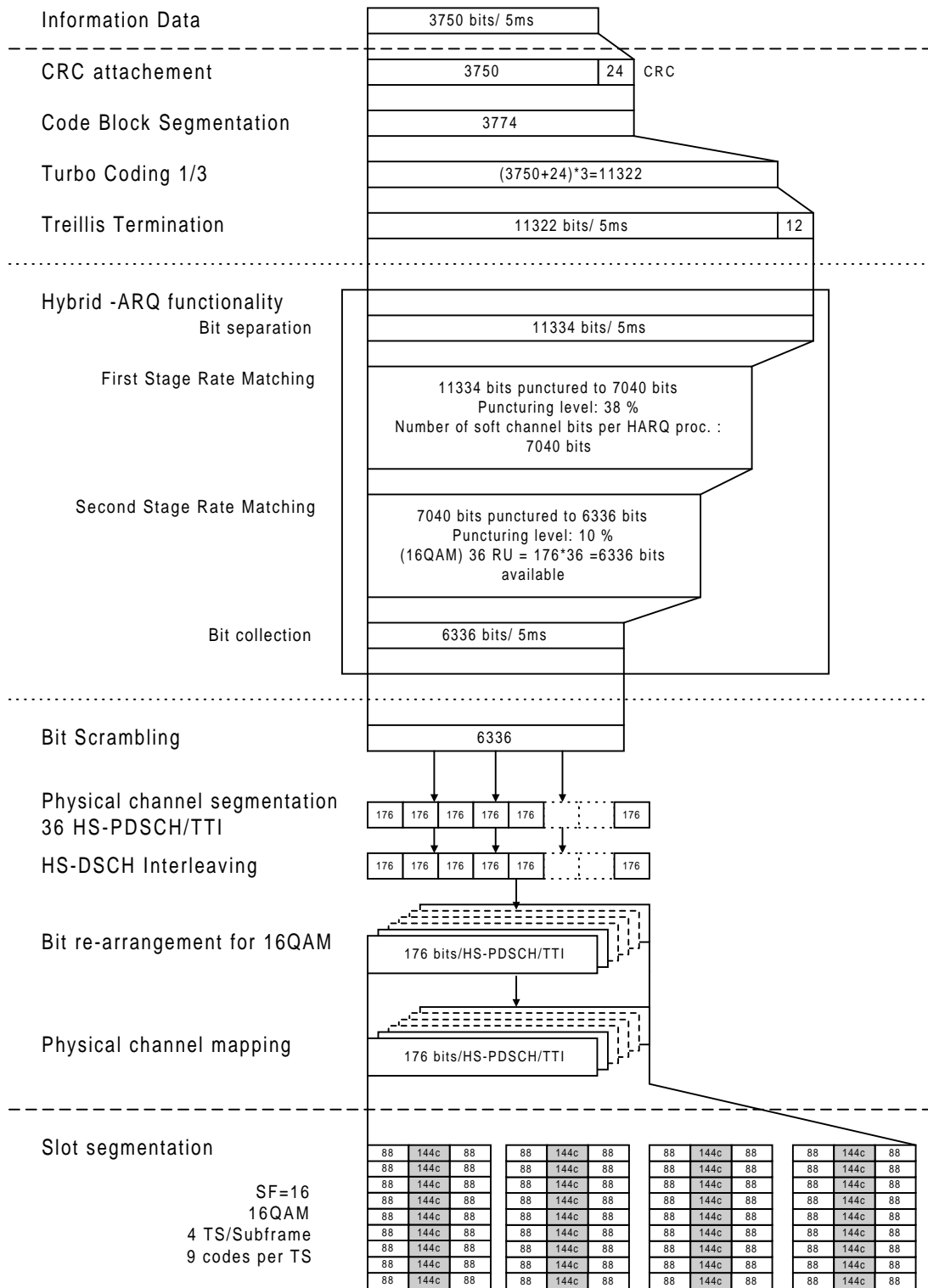


Figure [A.10]