3GPP TSG RAN Meeting #17 **_RP-020585_**
Biarritz, France, 3 – 6, September 2002

Title: **Agreed CRs (Rel-5) to TS 25.222**

Source: **TSG-RAN WG1**

Agenda item: **7.1.5**

No.	Spec	CR	Rev	R1 T-doc	Subject	Phase	Cat	Workitem	V_old	V_new
1	25.222	089	1	R1-02-0933	Clarification of TFRI bits for 3.84Mcps HSDPA TDD	Rel-5	F	HSDPA-Phys	5.1.0	5.2.0
2	25.222	091	1	R1-02-1094	HS-SCCH corrections for TDD	Rel-5	F	HSDPA-Phys	5.1.0	5.2.0
3	25.222	093	-	R1-02-1102	HS-DSCH Interleaving for TDD	Rel-5	F	HSDPA-Phys	5.1.0	5.2.0

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R1-02-0933

CR-Form-v7

CHANGE REQUEST

⌘	**25.222**	**CR**	**089**	⌘ **rev**	**1**	⌘	Current version:	**5.1.0**	⌘

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Proposed change affects:	UICC apps⌘ [ ]	ME [X]	Radio Access Network [X]	Core Network [ ]

Title:	⌘	Clarification of TFRI bits for 3.84Mcps HSDPA TDD		
Source:	⌘	TSG RAN WG1		
Work item code:	⌘	HSDPA-Phys	***Date:*** ⌘	28/06/2002
Category:	⌘	**F**	***Release:*** ⌘	Rel-5
		Use one of the following categories: ***F*** *(correction)* ***A*** *(corresponds to a correction in an earlier release)* ***B*** *(addition of feature),* ***C*** *(functional modification of feature)* ***D*** *(editorial modification)* Detailed explanations of the above categories can be found in 3GPP TR 21.900.		*Use one of the following releases:* *2 (GSM Phase 2)* *R96 (Release 1996)* *R97 (Release 1997)* *R98 (Release 1998)* *R99 (Release 1999)* *Rel-4 (Release 4)* *Rel-5 (Release 5)* *Rel-6 (Release 6)*

Reason for change:	⌘	There are only 13 bits available for addressing the HSDPA timeslots, corresponding to the maximum number that can be used for HSDPA DL transmissions. Therefore a rule is required to define which 13 of the 15 slots in a frame are candidates slots, or equivalently, which 2 are excluded.
Summary of change:	⌘	The need for slot assignment by higher layer signaling is eliminated. The order of the timeslots assignment is clearly stated and the 2 excluded slots are identified as it was done for LCR TDD.
Consequences if not approved:	⌘	Unclear slot assignment, unidentied excluded slots.

		Y	N			
Clauses affected:	⌘	4.6.1.2.2				
Other specs affected:	⌘		X	Other core specifications	⌘	
			X	Test specifications		
			X	O&M Specifications		
Other comments:	⌘					

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3) With "track changes" disabled, paste the entire CR form (use CTRL-A to select it) into the specification just in front of the clause containing the first piece of changed text. Delete those parts of the specification which are not relevant to the change request.

4.6.1.2 Timeslot information mapping

4.6.1.2.1 1.28 Mcps TDD

For 1.28 Mcps, the timeslots to be used for HS-PDSCH resources are signalled by the bits $x_{ts,1}$, $x_{ts,2}$, …, $x_{ts,5}$, where bit $x_{ts,n}$ carries the information for timeslot n+1. Timeslots 0 and 1 cannot be used for HS-DSCH resources. If the signalling bit is set (i.e. equal to 1), then the corresponding timeslot shall be used for HS-PDSCH resources. Otherwise, the timeslot shall not be used. All used timeslots shall use the same channelisation code set, as signalled by the channelisation code set information bits.

4.6.1.2.2 3.84 Mcps TDD

For 3.84 Mcps, the timeslots to be used for HS-PDSCH resources are signalled by the bits $x_{ts,1}$, $x_{ts,2}$, …, $x_{ts,13}$, where bit $x_{ts,n}$ carries the information for the nth available timeslot for HS-PDSCH resources, where the order of the timeslots available for HS-PDSCH resources shall be~~ signalled by higher layers~~ the same as the order of the 15 time slots within each frame with the following two slots removed:

- The slot containing the P-CCPCH
- The first slot in a frame containing the PRACH

If the P-CCPCH and/or PRACH are assigned to some, but not all frames, then the corresponding time slots shall remain unavailable for these frames as well.

If the bit is set (i.e. equal to 1), then the corresponding timeslot shall be used for HS-PDSCH resources. Otherwise, the timeslot shall not be used. All used timeslots shall use the same channelisation code set, as signalled by the channelisation code set information bits.

R1-02-1094

CR-Form-v7

CHANGE REQUEST

⌘	**25.222**	**CR**	**091**	⌘ **rev**	**1**	⌘	Current version:	**5.1.0**	⌘

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Proposed change affects: UICC apps⌘ [ ] ME [X] Radio Access Network [X] Core Network [ ]

Title:	⌘	HS-SCCH Corrections for TDD		
Source:	⌘	TSG RAN WG1		
Work item code:	⌘	HSDPA-Phys	***Date:*** ⌘	15/08/2002
Category:	⌘	**F**	***Release:*** ⌘	Rel-5
		Use one of the following categories: ***F*** *(correction)* ***A*** *(corresponds to a correction in an earlier release)* ***B*** *(addition of feature),* ***C*** *(functional modification of feature)* ***D*** *(editorial modification)* Detailed explanations of the above categories can be found in 3GPP TR 21.900.		*Use one of the following releases:* *2 (GSM Phase 2)* *R96 (Release 1996)* *R97 (Release 1997)* *R98 (Release 1998)* *R99 (Release 1999)* *Rel-4 (Release 4)* *Rel-5 (Release 5)* *Rel-6 (Release 6)*

Reason for change:	⌘	Notation of channelisation code set signalling on HS-SCCH is inconsistent. HS-SCCH coding and multiplexing figure is untitled. CRC attachment is incompletely specified. Field mappings missing.
Summary of change:	⌘	Use of $x_{css,n}$ to describe channelisation code set signalling is corrected to $x_{ccs,n}$. HS-SCCH coding and multiplexing figure is assigned as Figure 18c. CRC attachment and H-RNTI masking aligned with corresponding text in 25.212. Missing field mappings added.
Consequences if not approved:	⌘	Unclear specification. Unclear CRC masking function may cause incompatibilities between different UE and UTRAN implementations.

Clauses affected:	⌘	4.5, 4.6, 4.6.1.5, 4.6.1.6, 4.6.2, 4.6.3			
		Y	**N**		
Other specs affected:	⌘		**X**	Other core specifications	⌘
			X	Test specifications	
			X	O&M Specifications	
Other comments:	⌘				

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3) With "track changes" disabled, paste the entire CR form (use CTRL-A to select it) into the specification just in front of the clause containing the first piece of changed text. Delete those parts of the specification which are not relevant to the change request.

4.5 Coding for HS-DSCH

Figure 16 illustrates the overall concept of transport-channel coding~~ and multiplexing~~ for HS-DSCH. Data arrives ~~to ~~at the coding~~/multiplexing~~ unit in the form of one transport block once every ~~transmission time interval~~TTI. The ~~transmission time interval~~TTI is 5 ms for 1.28 Mcps TDD and 10 ms for 3.84 Mcps TDD.

The following coding~~/multiplexing~~ steps for HS-DSCH can be identified:

- add CRC to each ~~transmission time interval~~transport block (see subclause 4.5.1);
- code block segmentation (see subclause 4.5.2);
- channel coding (see subclause 4.5.3);
- hybrid ARQ (see subclause 4.5.4);
- bit scrambling (see subclause 4.5.5);
- physical channel segmentation (see subclause 4.5.6);
- interleaving for HS-DSCH (see subclauses 4.5.7);
- constellation re-arrangement for 16QAM (see subclause 4.5.8);
- mapping to physical channels (see subclause 4.5.9).

The coding steps for HS-DSCH are shown in figure 16.

4.6 Coding/Multiplexing for HS-SCCH

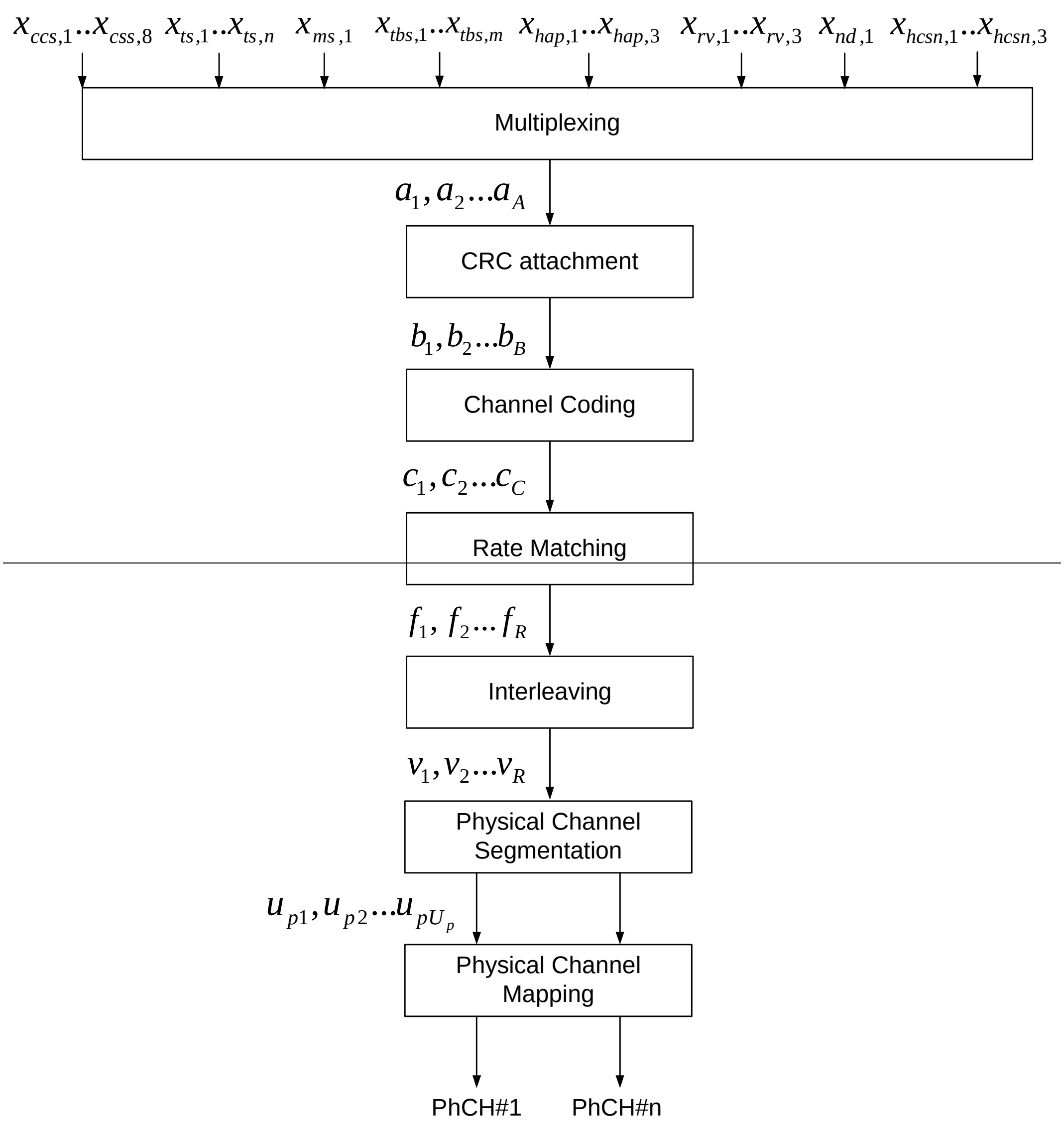
The following information, provided by higher layers, is transmitted by means of the HS-SCCH physical channel.

- Channelisation-code-set information (8 bits): $x_{ccs,1}$, $x_{ccs,2}$, …, $x_{ccs,8}$
- Time slot information (n bits where n = 5 for 1.28 Mcps TDD and n = 13 for 3.84 Mcps TDD): $x_{ts,1}$, $x_{ts,2}$, …, $x_{ts,n}$
- Modulation scheme information (1 bit): $x_{ms,1}$
- Transport-block size information (m bits where m = 6 for 1.28 Mcps TDD and m = 9 for 3.84 Mcps TDD): $x_{tbs,1}$, $x_{tbs,2}$, …, $x_{tbs,m}$
- Hybrid-ARQ process information (3 bits): $x_{hap,1}$, $x_{hap,2}$, $x_{hap,3}$
- Redundancy version information (3 bits): $x_{rv,1}$, $x_{rv,2}$,$x_{rv,3}$
- New data indicator (1 bit): $x_{nd,1}$
- HS-SCCH cyclic sequence number (3 bits): $x_{hcsn,1}$, $x_{hcsn,2}$, $x_{hcsn,3}$
- UE identity (16 bits): $x_{ue,1}$, $x_{ue,2}$, …, $x_{ue,16}$

The following coding/multiplexing steps can be identified:

- multiplexing of HS-SCCH information (see subclause 4.6.2)
- CRC attachment (see subclause 4.6.3);
- channel coding (see subclause 4.6.4);
- rate matching (see subclause 4.6.5);
- interleaving for HS-SCCH (see subclause 4.6.6);
- mapping to physical channels (see subclauses 4.6.7 and 4.6.8).

The general coding/multiplexing flow is shown in ~~the figure below~~Figure 18c.


$x_{ccs,1}..x_{css,8}$ $x_{ts,1}..x_{ts,n}$ $x_{ms,1}$ $x_{tbs,1}..x_{tbs,m}$ $x_{hap,1}..x_{hap,3}$ $x_{rv,1}..x_{rv,3}$ $x_{nd,1}$ $x_{hcsn,1}..x_{hcsn,3}$
Multiplexing
$a_1, a_2 \ldots a_A$
CRC attachment
$b_1, b_2 \ldots b_B$
Channel Coding
$c_1, c_2 \ldots c_C$
Rate Matching
$f_1, f_2 \ldots f_R$
Interleaving
$v_1, v_2 \ldots v_R$
Physical Channel Segmentation
$u_{p1}, u_{p2} \ldots u_{pU_p}$
Physical Channel Mapping
PhCH#1
PhCH#n

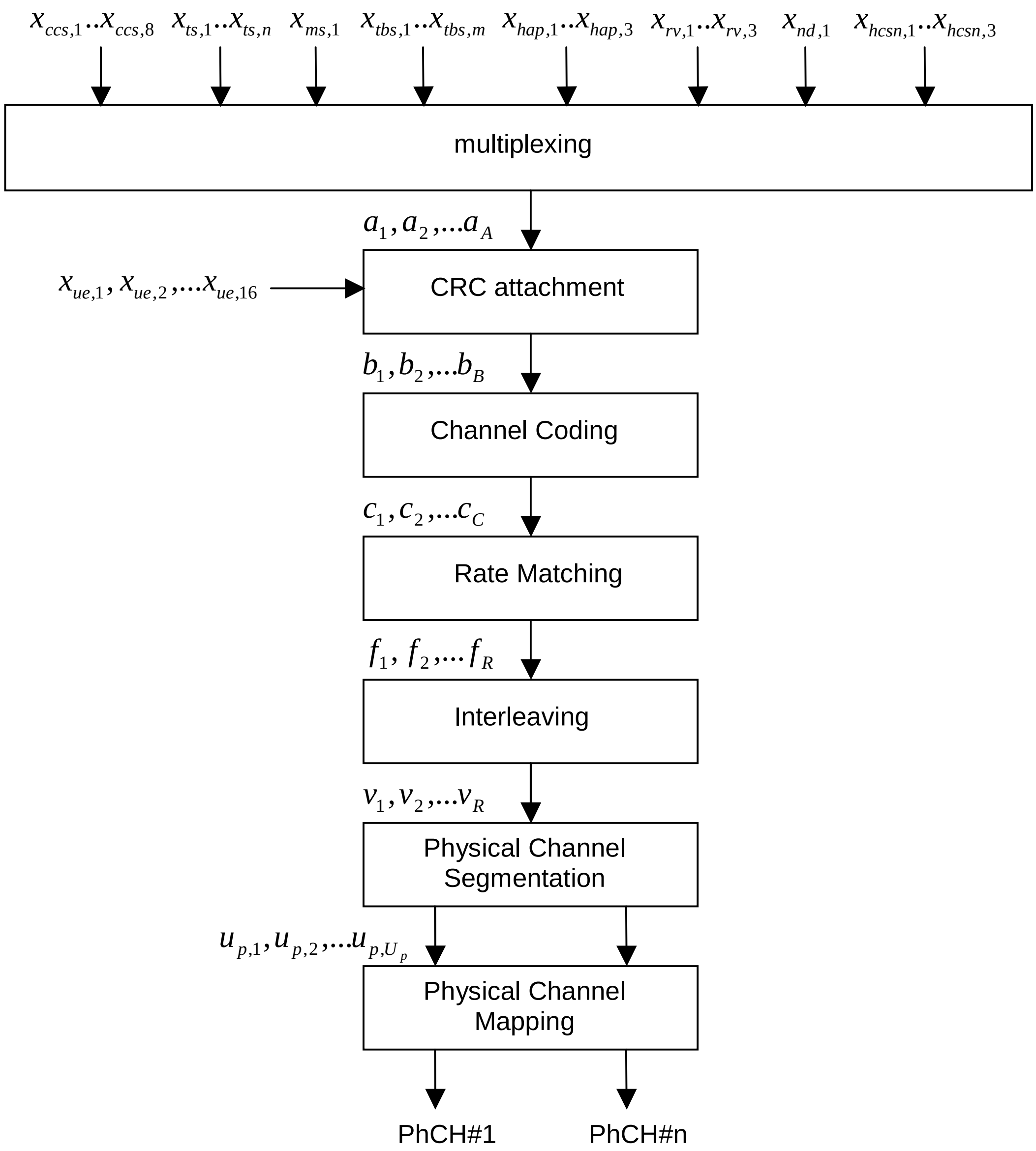


Figure 18c Coding and Multiplexing for HS-SCCH

4.6.1.5 HS-SCCH cyclic sequence number

The HS-SCCH cyclic sequence number is mapped such that $x_{hcsn,1}$ corresponds to the MSB and $x_{hcsn,3}$ to the LSB.

4.6.1.6 UE identity

The UE identity is the HS-DSCH Radio Network Identifier (H-RNTI) defined in [12]. This is mapped such that $x_{ue,1}$ corresponds to the MSB and $x_{ue,16}$ to the LSB.

4.6.2 Multiplexing of HS-SCCH information

The information carried on the HS-SCCH is multiplexed onto the bits $a_1, a_2, \ldots a_A$ according to the following rule :

$$\underline{a_1, a_2 \ldots a_8 = x_{ccs,1}, x_{ccs,2} \ldots x_{ccs,8}} \; \cancel{a_1, a_2 \ldots a_8 = x_{ccs,1}, x_{css,2} \ldots x_{css,8}}$$

$$a_9, a_{10} \ldots a_{9+n-1} = x_{ts,1}, x_{ts,2} \ldots x_{ts,n}$$

$$a_{9+n} = x_{ms,1}$$

$$a_{9+n+1}, a_{9+n+2} \ldots a_{9+n+m} = x_{tbs,1}, x_{tbs,2} \ldots x_{tbs,m}$$

$$a_{10+n+m}, a_{11+n+m}, a_{12+n+m} = x_{hap,1}, x_{hap,2}, x_{hap,3}$$

$$a_{13+n+m}, a_{14+n+m}, a_{15+n+m} = x_{rv,1}, x_{rv,2}, x_{rv,3}$$

$$a_{16+n+m} = x_{nd,1}$$

$$a_{17+n+m}, a_{18+n+m}, a_{19+n+m} = x_{hcsn,1}, x_{hcsn,2}, x_{hcsn,3}$$

4.6.3 CRC attachment for HS-SCCH

~~The bits b_1, ..., b_B are generated by adding the computed CRC of length 16 as described in the general section 4.2.1.1, and then scrambling the computed CRC by the modulo 2 addition of the UE identifier, $x_{ue,1}$, $x_{ue,2}$, …, $x_{ue,16}$.~~

From the sequence of bits $a_1, a_2, \ldots a_A$ a 16 bit CRC is calculated according to Section 4.2.1.1. This gives a sequence of bits $y_1, y_2, \ldots y_{16}$. This latter sequence of bits is then masked with the UE identity and appended to the sequence of bits $a_1, a_2, \ldots a_A$. The bits at the output of the CRC attachment block is the sequence of bits $b_1, b_2, \ldots b_B$, where

$$b_i = a_i \qquad i=1,2,\ldots,A$$

$$b_i = \left(y_{i-A} + x_{ue,i-A}\right) \bmod 2 \qquad i=A+1\ldots B$$

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⌘	**25.222**	**CR**	**093**	⌘ **rev**	**-**	⌘	Current version:	**5.1.0** ⌘

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Proposed change affects: UICC apps⌘ [ ] ME [X] Radio Access Network [X] Core Network [ ]

Title:	⌘	HS-DSCH Interleaving for TDD		
Source:	⌘	TSG RAN WG1		
Work item code:	⌘	HSDPA-Phys	***Date:*** ⌘	16/8/2002
Category:	⌘	**F**	***Release:*** ⌘	Rel-5
		Use <u>one</u> of the following categories: ***F*** *(correction)* ***A*** *(corresponds to a correction in an earlier release)* ***B*** *(addition of feature),* ***C*** *(functional modification of feature)* ***D*** *(editorial modification)* Detailed explanations of the above categories can be found in 3GPP TR 21.900.		*Use <u>one</u> of the following releases:* *2 (GSM Phase 2)* *R96 (Release 1996)* *R97 (Release 1997)* *R98 (Release 1998)* *R99 (Release 1999)* *Rel-4 (Release 4)* *Rel-5 (Release 5)* *Rel-6 (Release 6)*

Reason for change:	⌘	Current specification of HS-DSCH interleaver and physical channel mapping for TDD are incorrect.
Summary of change:	⌘	Frame related interleaving is proposed. Symbol based physical channel mapping based on the Release 99 physical channel mapping scheme is proposed.
Consequences if not approved:	⌘	Implementation of HS-DSCH for TDD will not be possible, physical channel mapping will be suboptimal in the case of uplink / downlink interference and will be out of line with the Release 99 physical channel mapping scheme.

Clauses affected:	⌘	4.5, 4.5.6 – 4.5.9				
		Y	N			
Other specs affected:	⌘		X	Other core specifications	⌘	
			X	Test specifications		
			X	O&M Specifications		
Other comments:	⌘					

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3) With "track changes" disabled, paste the entire CR form (use CTRL-A to select it) into the specification just in front of the clause containing the first piece of changed text. Delete those parts of the specification which are not relevant to the change request.

4.5 Coding for HS-DSCH

Figure 16 illustrates the overall concept of transport-channel coding and multiplexing for HS-DSCH. Data arrives to the coding/multiplexing unit in form of one transport block once every transmission time interval. The transmission time interval is 5 ms for 1.28Mcps TDD and 10ms for 3.84 Mcps TDD.

The following coding/multiplexing steps for HS-DSCH can be identified:

- add CRC to each transmission time interval (see subclause 4.5.1);
- code block segmentation (see subclause 4.5.2);
- channel coding (see subclause 4.5.3);
- hybrid ARQ (see subclause 4.5.4);
- bit scrambling (see subclause 4.5.5);
- ~~physical channel segmentation (see subclause 4.5.6);~~
- interleaving for HS-DSCH (see subclauses 4.5.6~~7~~);
- constellation re-arrangement for 16QAM (see subclause 4.5.7~~8~~);
- mapping to physical channels (see subclause 4.5.8~~9~~).

The coding steps for HS-DSCH are shown in figure 16.

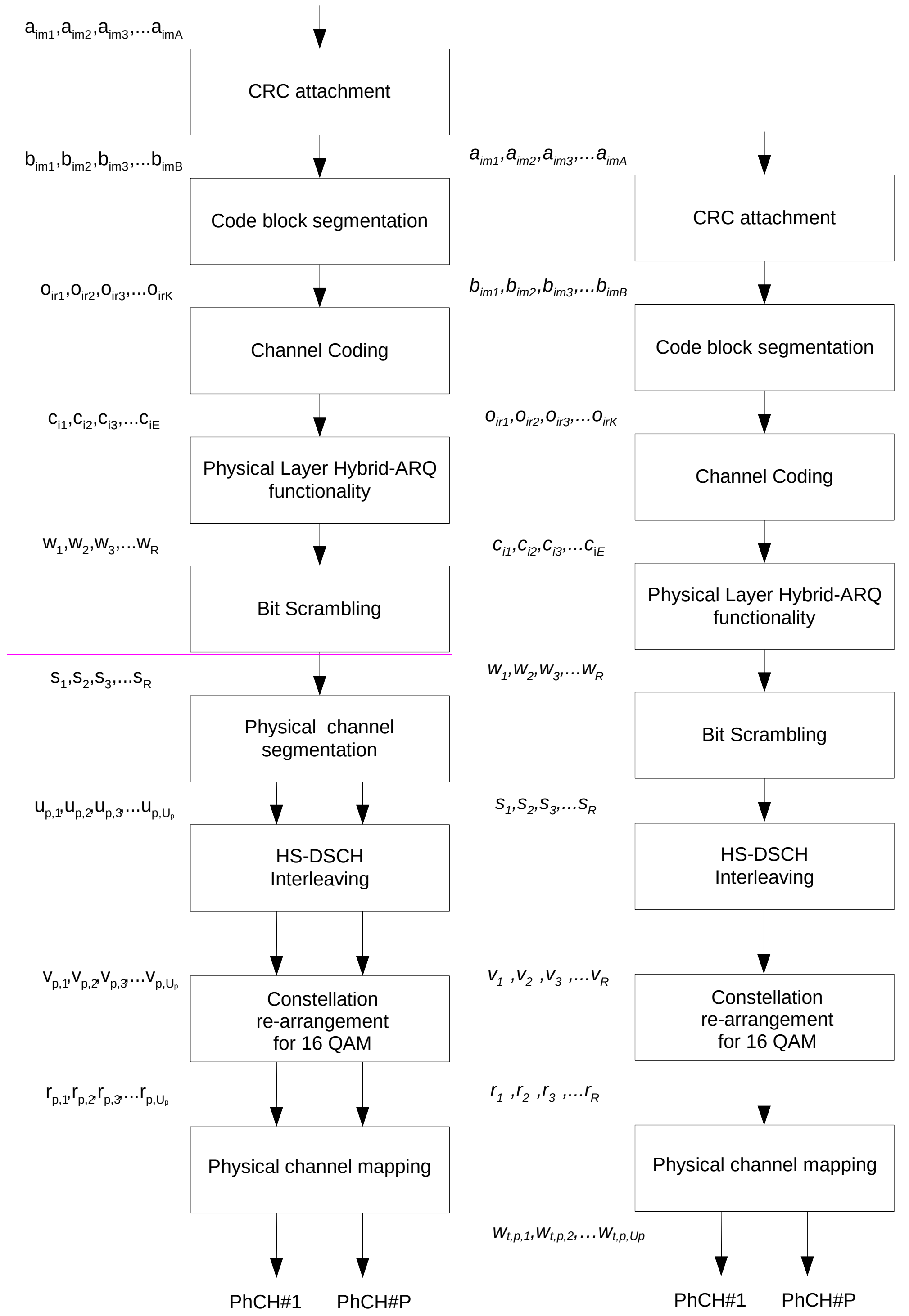

Figure 16. Coding chain for HS-DSCH

In the following the number of transport blocks is always one. When referencing non HS-DSCH formulae which are used in correspondence with HS-DSCH formulae the convention is used that transport block subscripts may be omitted (e.g. X_i when i is always 1 may be written X).

~~4.5.6 Physical channel segmentation for HS-DSCH~~

~~When more than one HS-PDSCH is used, physical channel segmentation divides the bits among the different physical channels. The bits input to the physical channel segmentation are denoted by~~ $s_1, s_2, s_3, \ldots s_R$, ~~where R is the number of bits input to the physical channel segmentation block. The number of PhCHs is denoted by~~ P.

~~The bits after physical channel segmentation are denoted~~ $u_{p1}, u_{p2}, \ldots, u_{pU_p}$, ~~where~~ p ~~is PhCH number and~~ U_p ~~is the number of bits in one TTI for PhCH~~ p, ~~such that:~~

$$R = \sum_{p=1}^{P} U_p$$

~~PhCHs shall be numbered starting from 1 in ascending order of their timeslot number, such that PhCHs allocated to a lower numbered timeslot always have a lower PhCH number than those allocated to a higher numbered timeslot. If more than one PhCH is allocated in a given timeslot, then the PhCHs shall be numbered in ascending order of their channelisation code index (k). The relation between~~ s_k ~~and~~ u_{pk} ~~is given below.~~

~~For all modes, some bits of the input flow are mapped to each code until the number of bits on the code is~~ U_p.

~~Bits on first PhCH after physical channel segmentation:~~

$$u_{1,k} = s_k \qquad k = 1, 2, \ldots, U_1$$

~~Bits on second PhCH after physical channel segmentation:~~

$$u_{2,k} = s_{k+U_1} \qquad k = 1, 2, \ldots, U_2$$

~~…~~

~~Bits on the~~ P^{th} ~~PhCH after physical channel segmentation:~~

$$u_{P,k} = s_{k+\sum_{p=1}^{P-1} U_p} \qquad k = 1, 2, \ldots, U_P$$

4.5.6~~7~~ Interleaving for HS-DSCH

The interleaving for TDD is done over all bits in the TTI, as shown in figure 18a ~~below~~when QPSK modulation is being used for the HS-DSCH, and figure 1~~9~~8b when 16-QAM modulation is being used~~, separately for each physical channel~~. The bits input to the block interleaver are denoted by ~~$u_1, u_2, u_3, \ldots, u_U$~~ $s_1, s_2, s_3, \ldots, s_R$, where R~~U~~ is the number of bits in one TTI. ~~For QPSK the interleaver is the same as Rel99 2nd interleaver described in Section 4.2.11.1. The interleaver is of fixed size: R2=32 rows and C2=30 columns.~~

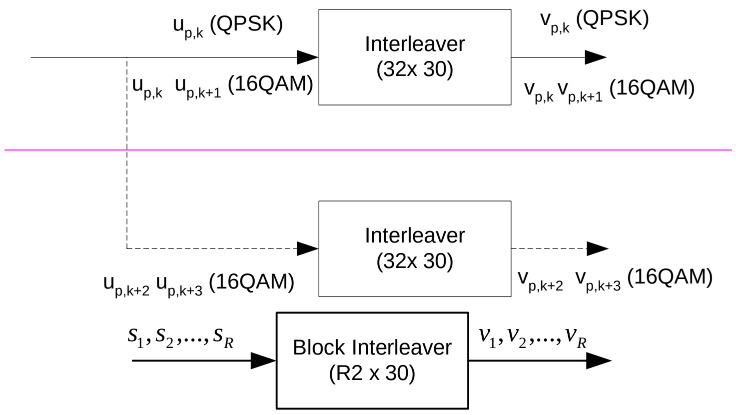

Figure 18a: Interleaver structure for HS-DSCH with QPSK modulation

For QPSK, the interleaver is a block interleaver and consists of bits input to a matrix with padding, the inter-column permutation for the matrix and bits output from the matrix with pruning. The output bit sequence from the block interleaver is derived as follows:

(1) The number of columns of the matrix is 30. The columns of the matrix are numbered 0, 1, 2, …, 29 from left to right.

(2) Determine the number of rows of the matrix, $R2$, by finding minimum integer $R2$ such that $R \leq 30 \times R2$. The rows of rectangular matrix are numbered 0, 1, 2, …, $R2 - 1$ from top to bottom.

(3) Write the input bit sequence $s_1, s_2, s_3, ..., s_R$ into the $R2 \times 30$ matrix row by row starting with bit y_1 in column 0 of row 0:

$$\begin{bmatrix} y_1 & y_2 & y_3 & \cdots & y_{30} \\ y_{31} & y_{32} & y_{33} & \cdots & y_{60} \\ \vdots & \vdots & \vdots & & \vdots \\ y_{30\cdot(R2-1)+1} & y_{30\cdot(R2-1)+2} & y_{30\cdot(R2-1)+3} & \cdots & y_{30\cdot R2} \end{bmatrix}$$

where $y_k = s_k$ for k = 1, 2, …, R and, if $R < 30\times R2$, dummy bits are inserted for $k = R+1, R+2, …, 30\times R2$. These dummy bits are pruned away from the output of the matrix after the inter-column permutation.

(4) Perform the inter-column permutation for the matrix based on the pattern $\left\langle P2(j) \right\rangle_{j\in\{0,1,\ldots,29\}}$ that is shown in Table 8, where P2(j) is the original column position of the j-th permuted column. After permutation of the columns, the bits are denoted by y'_k.

$$\begin{bmatrix} y'_1 & y'_{R2+1} & y'_{2\cdot R2+1} & \cdots & y'_{29\cdot R2+1} \\ y'_2 & y'_{R2+2} & y'_{2\cdot R2+2} & \cdots & y'_{29\cdot R2+2} \\ \vdots & \vdots & \vdots & & \vdots \\ y'_{R2} & y'_{2\cdot R2} & y'_{3\cdot R2} & \cdots & y'_{30\cdot R2} \end{bmatrix}$$

(5) The output of the block interleaver is the bit sequence read out column by column from the inter-column permuted $30\times R2$ matrix. The output is pruned by deleting dummy bits that were padded to the input of the matrix before the inter-column permutation, i.e. bits y'_k that corresponds to bits y_k with $k > R$ are removed from the output. The bits after interleaving are denoted by $v_1, v_2, v_3, ..., v_R$, where v_1 corresponds to the bit y'_k with smallest index k after pruning, v_2 to the bit y'_k with second smallest index k after pruning, and so on.

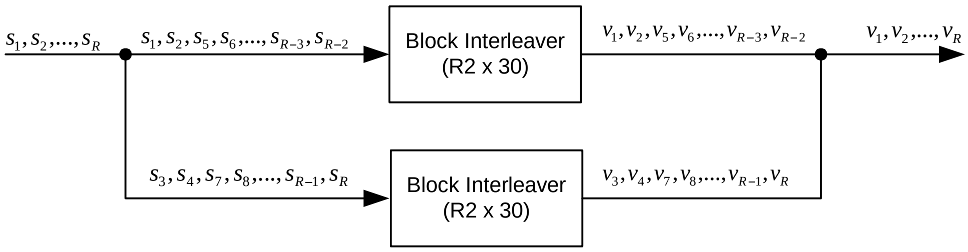

Figure 1~~9~~8b: Interleaver structure for HS-DSCH with 16-QAM modulation

For 16QAM, ~~there are two~~ a second identical interleaver~~s of the same fixed size R2×C2 = 32×30~~operates in parallel to the first. For both interleavers, $R2$ is chosen to be the minimum integer that satisfies $R \leq 60 \times R2$. The output bits from the ~~physical channel segmentation~~bit scrambling operation are divided pairwise between the interleavers: bits ~~$u_{p,k}$~~s_k and ~~$u_{p,k+1}$~~s_{k+1} go to the first interleaver and bits ~~$u_{p,k+2}$~~s_{k+2} and ~~$u_{p,k+3}$~~s_{k+3} go to the second interleaver, where k mod 4 = 1. Bits are collected pairwise from the interleavers: bits ~~$v_{p,k}$~~v_k and ~~$v_{p,k+1}$~~v_{k+1} are obtained from the first interleaver and bits ~~$v_{p,k+2}$~~v_{k+2} and ~~$v_{p,k+3}$~~v_{k+3} are obtained from the second interleaver, where again k mod 4 = 1.

4.5.7~~8~~ Constellation re-arrangement for 16 QAM

This function only applies to 16 QAM modulated bits. In case of QPSK it is transparent.

The following table 16 describes the operations that produce the different rearrangements.

The bits of the input sequence are mapped in groups of 4 so that ~~$v_{p,k}, v_{p,k+1}, v_{p,k+2}, v_{p,k+3}$~~$v_k, v_{k+1}, v_{k+2}, v_{k+3}$ are used, where k mod 4 = 1.

Table 16: Constellation re-arrangement for 16 QAM

Constellation version Parameter *b*	Output bit sequence	Operation
0	$v_k v_{k+1} v_{k+2} v_{k+3}$ ~~$v_{p,k} v_{p,k+1} v_{p,k+2} v_{p,k+3}$~~	None
1	$v_{k+2} v_{k+3} v_k v_{k+1}$ ~~$v_{p,k+2} v_{p,k+3} v_{p,k} v_{p,k+1}$~~	Swapping MSBs with LSBs
2	$v_k v_{k+1} \overline{v_{k+2}}\, \overline{v_{k+3}}$ ~~$v_{p,k} v_{p,k+1} \overline{v_{p,k+2}}\, \overline{v_{p,k+3}}$~~	Inversion of the logical values of LSBs
3	$v_{k+2} v_{k+3} \overline{v_k}\, \overline{v_{k+1}}$ ~~$v_{p,k+2} v_{p,k+3} \overline{v_{p,k}}\, \overline{v_{p,k+1}}$~~	Swapping MSBs with LSBs, and inversion of the logical values of LSBs

The output bit sequences from the table above map to the output bits in groups of 4, i.e. ~~$r_{p,k}, r_{p,k+1}, r_{p,k+2}, r_{p,k+3}$~~ $r_k, r_{k+1}, r_{k+2}, r_{k+3}$, where k mod 4 = 1.

4.5.8~~9~~ Physical channel mapping for HS-DSCH

The HS-PDSCH is defined in [7]. The bits input to the physical channel mapping are denoted by $r_1, r_2, ..., r_R$ ~~$r_{p,1}, r_{p,2}, r_{p,3}, \ldots, r_{p,U_p}$~~, where ~~*p*~~ *R* is the number of physical channel bits in the allocation for the current ~~number and U_p is the number of bits in PhCH *p* in one~~ TTI. These bits are mapped to the physical channel bits, $\{w_{t,p,j} : t = 1, 2, ..., T; p = 1, 2, ..., C; j = 1, 2, ..., U_t\}$, where *t* is the timeslot index, *T* is the number of timeslots in the allocation message, *p* is the physical channel index, *C* is the number of codes per timeslot in the allocation message, *j* is the physical channel bit index and U_t is the number of bits per physical channel in timeslot *t*. The timeslot index, *t*, increases with increasing timeslot number; the physical channel index, *p*, increases with increasing channelisation code index, and the physical channel bit index, *j*, increases with increasing physical channel bit position in time.

The bits $r_{\cancel{p},k}$ shall be mapped to the PhCHs ~~such that the bits for PhCHs shall be transmitted over the air in ascending order with respect to the bit index *k*.~~according to the following rule :

Define $\{y_{t,k} : k = 1, 2, ..., C \cdot U_t\}$ to be the set of bits to be transmitted in timeslot *t* as follows :

$$y_{1,k} = r_k \qquad \text{for } k = 1, 2, ..., C \cdot U_1$$

$$y_{2,k} = r_{k+C \cdot U_1} \qquad \text{for } k = 1, 2, ..., C \cdot U_2$$

…

$$y_{T,k} = r_{k+C\sum_{t=1}^{T-1} U_t} \qquad \text{for } k = 1, 2, ..., C \cdot U_T$$

When the modulation level applied to the physical channels is 16-QAM :

The physical channel *p* used to transmit the k^{th} bit in the sequence $y_{t,k}$ is :

$$p = \left\lfloor \frac{k-1}{4} \right\rfloor \bmod C + 1$$

If *p* is odd then :

$$w_{t,p,j} = y_{t,k} \text{ where } j = 4 \cdot \left\lfloor \frac{k-1}{4 \cdot C} \right\rfloor + (k-1) \bmod 4 + 1$$

If *p* is even then :

$$w_{t,p,j} = y_{t,k} \text{ where } j = U_t - 4 \cdot \left\lfloor \frac{k-1}{4 \cdot C} \right\rfloor - 3 + (k-1) \bmod 4$$

Otherwise, when the modulation level applied to the physical channels is QPSK :

The physical channel *p* used to transmit the k^{th} bit in the sequence $y_{t,k}$ is :

$$p = (k-1) \bmod C + 1$$

If *p* is odd then :

$$w_{t,p,j} = y_{t,k} \text{ where } j = \left\lfloor \frac{k-1}{C} \right\rfloor + 1$$

If p is even then :

$$w_{t,p,j} = y_{y,k} \text{ where } j = U_t - \left\lfloor \frac{k-1}{C} \right\rfloor$$