Status Report for WI to TSG

Work Item Name: RL Timing Adjustment

SOURCE: Rapporteur (Ericsson) **TSG: RAN** **WG: 3 (leading), 2**

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Ref. to WI sheet: RAN_Work_Items.doc

Progress Report since the last TSG (for all involved WGs):

During RAN3 #27, it was agreed that the solution by which the RL timing is adjusted *advancing or delaying (with respect to the SFN timing) the DL DPCH timing by 256 chips* was agreed.
Relevant change requests were agreed on TS 25.433 and TS 25.423, so all the needed support is in place in RAN3 specifications.

During RAN2 #27 a discussion paper and a CR on TS 25.331 were submitted in order to introduce the required support in the RRC specification by means of DL DPCH shifts. The proposed solution and the related change request were approved.

Technical report 25.878 was finalised and agreed as version 2.0.0.

List of open issues:

None

Estimates of the level of completion (when possible):

The WI can be considered finalised, the necessary support is in place for all involved working groups and no open issues remain.

WI completion date review resulting from the discussion at the working groups:

March 2002 (TSG RAN#15).

References to WG's internal documentation and/or TRs:

TR 25.878 2.0.0 (R3-020870).