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Foreword

This Technical Report has been produced by the 3rd Generation Partnership Project (3GPP).

The contents of the present document are subject to continuing work within the TSG and may change following formal TSG approval. Should the TSG modify the contents of the present document, it will be re-released by the TSG with an identifying change of release date and an increase in version number as follows:

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1 Scope

The purpose of this document is to capture the agreements and evaluation criteria of the different techniques being considered for HSDPA with regards to the overall support of UTRAN for HSDPA.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies. In the case of a reference to a 3GPP document (including a GSM document), a non-specific reference implicitly refers to the latest version of that document *in the same Release as the present document*.

[1] 3GPP TR 25.950 v4.0.0 UTRA High Speed Downlink Packet Access

[2] 3GPP TR 25.855 v0.0.5 UTRA High Speed Downlink Packet Access

[3] RAN2 stage2 description for HSDPA (TS25.308)

3 Background and Introduction

In RAN#11 plenary meeting a work item was approved for High Speed Downlink Packet Access. The work item includes techniques such as adaptive modulation and coding, hybrid ARQ and fast scheduling with the goal to increase throughput, reduce delay and achieve high peak rates.

4 Basic physical layer structure of HS-DSCH

4.1 HS-DSCH physical-layer structure in code domain

HS-DSCH transmission for FDD uses channelization codes at a fixed spreading factor SF=16.. Multi-code transmission is allowed, which translates to UE being assigned multiple channelisation codes in the same TTI, depending on its UE capability. The same scrambling code sequence is applied to all the channelisation codes that form a single HS-DSCH CCTrCH. Furthermore, multiple UEs may be assigned channelisation codes in the same TTI i.e. multiplexing of multiple UE's in code-domain is allowed.

HS-DSCH transmission for TDD uses a fixed spreading factor SF=16 and multi-code transmission on one or more timeslots. Furthermore, a combination of code multiplexing and time multiplexing UEs within an HS-DSCH TTI is possible.

4.2 HS-DSCH physical-layer structure in time domain

For FDD , the length of the HS-DSCH TTI is $\mathbf{3\times T_{slot}}$**,** where T_{slot} is equal to 2560 chip (≈0.67 ms). The TTI for HS-DSCH is a static transport-format parameter.

1.28 Mcps TDD uses a fixed single 5ms TTI. The TTI for 3.84 Mcps TDD is for FFS.

5 Channel Coding and Modulation for HS-DSCH

5.1 CCTrCH and transport channels

There is only one CCTrCH of HS-DSCH type per UE. If there are several HS-DSCH transport channels in an HS-DSCH CCTrCH, the transport format combinations are configured in such a way that for any transport format combination, there is a maximum of one transport channel having a transport format with one or more transport blocks. There is no need to balance the quality between several transport channels. As such, there is no need for static rate matching parameters. As for the DSCH of Release-99, flexible positions are assumed.

5.2 Transport block concatenation and code block segmentation

The same transport block concatenation and code block segmentation as in Release-99 is used for HS-DSCH. However, Transport block concatenation is performed before CRC attachment since there is only one CRC per TTI. The maximum code block size for turbo coding is 5114.

5.3 CRC Attachment

A CRC of size 24 bits is calculated and added per HS-DSCH TTI. The CRC polynomial is defined in 3G TS 25.212.

5.4 Channel Coding

HS-DSCH channel coding uses the existing rate 1/3 Turbo code and the existing Turbo code internal interleaver, as outlined in 3G TS 25.212. Other code rates are generated from the basic rate 1/3 Turbo code by applying rate matching by means of puncturing or repetition.

5.4.1 Channel Coding for Control Channels

Defined in Section 9.1 and 9.2.

5.4.2 Physical Layer Channel Coding Chain

Figure 1 depicts the channel coding and physical layer mapping chain for HS-DSCH.

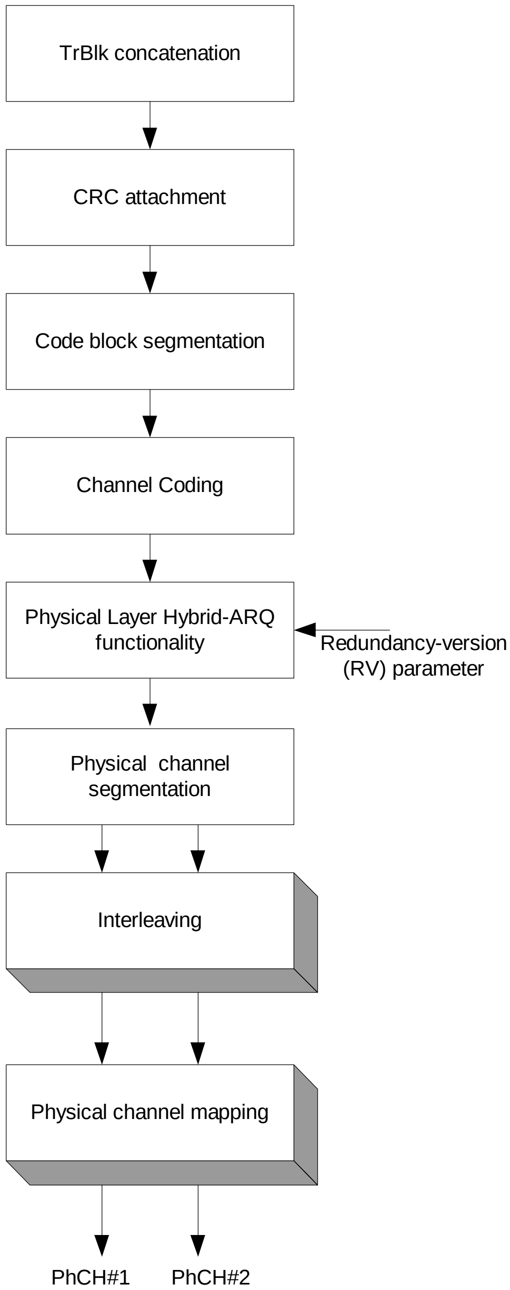


Figure 1. Transport Channel Coding Structure for HS-DSCH

5.5 Physical-layer Hybrid-ARQ functionality

The physical-layer Hybrid-ARQ functionality is an extension of the release 99 rate matching. The Hybrid-ARQ functionality matches the number of bits at the output of the channel (turbo) coder to the total number of bits of the HS-DSCH physical channels. The Hybrid-ARQ functionality is controlled by the parameter RV (Redundancy Version), i.e. the exact set of bits at the output of the physical-layer Hybrid-ARQ functionality depends on the number of input bits, the number of output bits, and the RV parameter.

The physical-layer Hybrid ARQ functionality consists of two rate-matching stages as shown in Figure 2.

The first rate-matching stage is identical to the release 99 rate-matching functionality except that the number of output bits does not match to the number of physical-channel bits available in the HS-DSCH TTI. Instead, the number of output bits matches to the available UE soft-buffering capability, information about which is provided by higher layers.

Note that, if the number of input bits does not exceed the UE soft-buffering capability, the first rate-matching stage is transparent.

The second rate-matching stage matches the number of bits at the output of the first rate-matching stage to the number of physical-channel bits available in the HS-DSCH TTI. The second rate-matching stage uses the same basic algorithm as release 99 rate matching. However, compared to release 99 rate matching, for the Hybrid-ARQ functionality, the rate-matching algorithm may use different values for the rate-matching parameters, e.g. the e_{ini} parameter, depending on the RV parameter. Depending on the value of the RV parameter, the rate matching algorithm may also be applied differently to different set of input bits (systematic and parity bits).

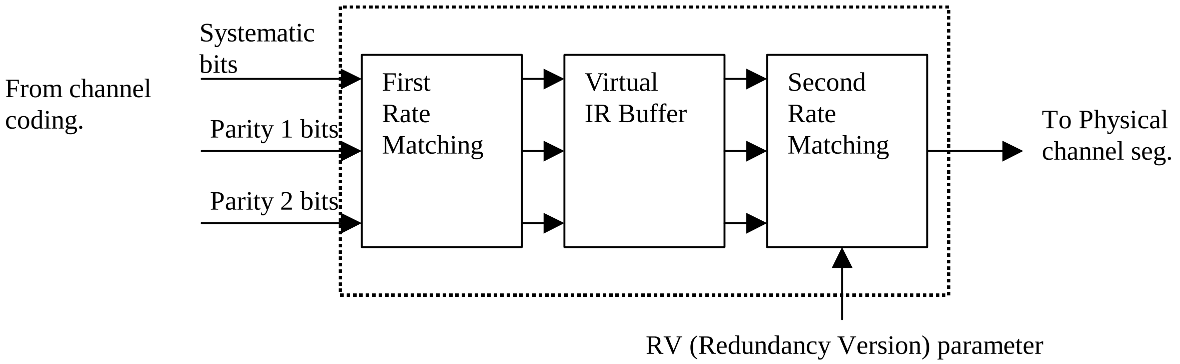


Figure 2. Physical layer Hybrid ARQ functionality

5.6 DTX indication bits

DTX insertion is not employed. Since only one transport channel per TTI is supported, the rate-matching algorithm is used to fill the available physical resource, instead of using DTX insertion.

5.7 Interleaving

Since the HS-DSCH TTI is static, only one interleaving (corresponding to Release-99 2^{nd} interleaving) is needed. The interleaver has to be adapted to 3 slots.

For TDD, interleaving adaptation has to be done to the HS-DSCH TTI length.

5.8 Physical channel mapping

The bits can be mapped to multiple physical channels in the same way as in release'99.

5.9 Modulation

Two types of modulations namely QPSK and 16-QAM may be applied for HS-DSCH.

6 Link Adaptation

For HS-DSCH, the transport format, including the modulation scheme and code rate, can be selected based on the downlink channel quality. The selection of transport format is done by the MAC-HS located in Node B and can be based on e.g. channel-quality feedback reported by the UE, see Section 9, or from the transmit power of an associated DPCH. Other methods may also be possible.

7 Hybrid ARQ

7.1 Choice of Hybrid ARQ combining schemes

a) For a retransmission, the transport-block set is the same as for the initial transmission. This means that, for a retransmission, the number of information bits N_{INFO} to be transmitted is the same as for the initial transmission. Furthermore, for a retransmission, the modulation scheme and the channelisation-code set, including the size of the channelisation-code set, and the transmission power, may be different compared to the initial transmission. This means that, for a retransmission, the number of available channel bits N_{ch} may differ compared to the initial transmission. Even if the number of available channel bits N_{ch} is the same, the set of channel bits may be different for the retransmission compared to the initial transmission (Incremental Redundancy).

b) Regardless of the number of information bits N_{INFO}, channel coding is done using a Turbo code with rate $R_{basic} = 1/3$. Each retransmission may use a different redundancy version, where each redundancy version is a different subset of the coded bits. Each subset may contain a different number of bits. Chase combining corresponds to defining or using only a single redundancy version.

7.2 Physical layer aspects of Hybrid ARQ

The following signalling is needed to support Hybrid ARQ. The details of signalling are described in Section 9.

Downlink Signaling

The HARQ information includes the Hybrid ARQ process identifier in the corresponding HS-DSCH TTI. The HARQ information also includes information about the redundancy version of the transmission in the corresponding HS-DSCH TTI.

Uplink Signaling

For communicating the HARQ acknowledgements, an *1*-bit ACK/NACK indication is used in the uplink.

8 Associated Signalling

8.1 Downlink

8.1.1 Overall Structure

Figure 3 illustrates the basic physical-channel structure for the HS-DSCH-related associated downlink signalling as seen from the UE point-of-view. It consists of a downlink DPCH and a number of SCCH-HSs. The number of SCCH-HSs can range from a minimum of one SCCH-HS (M=1) to a maximum of four SCCH-HSs (M=4).

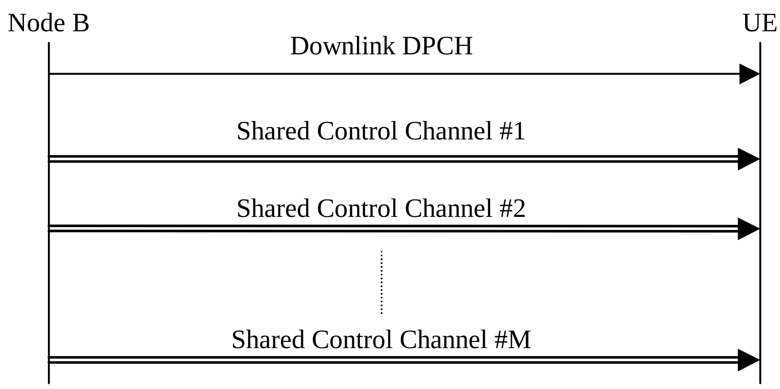


Figure 3. Basic physical-channel structure for HS-DSCH-related associated downlink signalling

8.1.2 Detailed Structure FDD

Shared Control Channel

For each HS-DSCH TTI, each Shared Control Channel (SCCH-HS) carries HS-DSCH-related downlink signalling for one UE. The following information is carried on the SCCH-HS:

- ***Transport-format and Resource related Information (TFRI)***

- Channelization-code set: 7 bits
- Modulation scheme: 1 bit
- Transport-block-set size + Transport-channel identity: 6 bits
- ***Hybrid-ARQ-related Information (HARQ information)***
.
- Hybrid-ARQ process number: 3 bits
- Redundancy version: [2] bits
- New-data indicator: [1] bit

The exact number of bits for the Hybrid-ARQ-related information is to be confirmed with RAN2.

The Shared-Control-Channel information is split into two parts:

- Part-1: Channelization code set and modulation scheme (8 bits)
- Part-2: Transport-block-set size + Transport-channel identity and Hybrid-ARQ-related information ([12] bits)

CRC attachment

Two cases are currently considered for CRC attachment to the Shared-Control-Channel signaling:

- Alternative 1: CRC (16 bits) calculated over Part-1 + Part-2 and attached to Part-2
- Alternative 2: CRC1 (12 bits) calculated over Part-1 and attached to Part-1, CRC2 (8 bits) calculated over Part-1 + Part-2 and attached to Part-2.

UE identity is implicitly included in the calculation of CRC (for alternative 1) and CRC1 (for alternative 2).

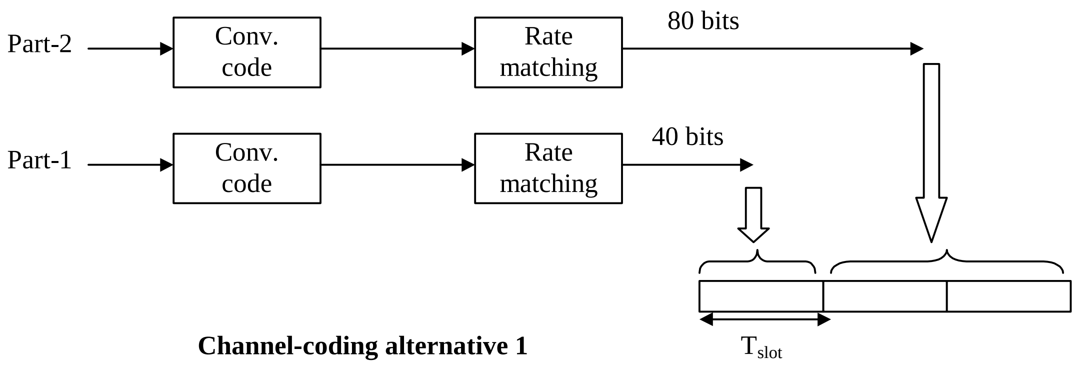
Channel coding

Channel coding for the SCCH-HS is based on release 99 convolutional coding.

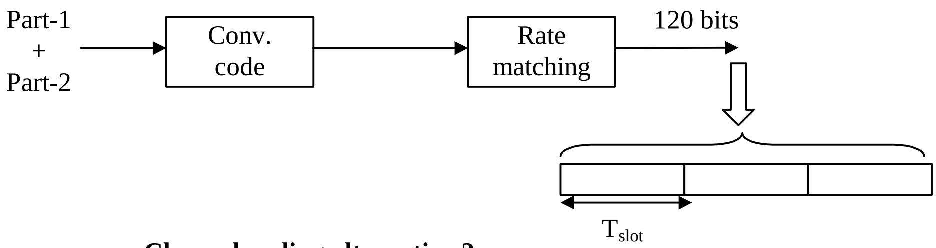
Two alternatives are currently considered for the details of the Shared-Control-Channel channel coding, see also Figure 1:

- Alternative1:
  Part-1 is separately coded and rate matched to fit into the first slot of the Shared Control Channel. Part-2 is separately coded and rate matched to fit into the second + third slot of the SCCH-HS. This alternative directly allows for extraction of the time-critical Part-1 information before the start of the HS-DSCH TTI, see timing relation below.

- Alternative2:
  Part-1+Part 2 is jointly coded and rate-matched to fit into the three slots of the SCCH-HS. The rate matching may not be applied equally to all SCCH-HS slots. By applying separate interleaving over e.g. the first 1½ slot, this scheme also allows for extraction of the time-critical Part-1 information before the HS-DSCH TTI, e.g. by early back-tracing of the trellis-decoding process.



Channel-coding alternative 1



Channel-coding alternative 2

CRC alternative 1:
Part-1: Channelization-code set + modulation scheme (8 bits)
Part-2: Transport-format + Transport-channel ID + HARQ-related information + CRC (28 bits)

CRC alternative 2:
Part-1: Channelization-code set + modulation scheme +CRC1 (20 bits)
Part-2: Transport-format + Transport-channel ID + HARQ-related information + CRC2 (20 bits)

Figure 4 Channel-coding alternative 1 and alternative 2

The alternatives above (CRC attachment and detailed channel-coding scheme) are to be evaluated and a single scheme is to be selected.

Downlink DPCH

If a downlink DPCH is present, it carries an HS-DSCH Indicator (HI), in addition to non-HS-DSCH-related physical-layer signalling and DCH transport channels. The HI consists of two information bits that indicate the SCCH-HS that carries the HS-DSCH-related signalling for the corresponding UE. The HI is transmitted in every third slot. If no SCCH-HS carries HS-DSCH-related signalling to the UE, the HI is not transmitted (DTX). As an example, if the HI is transmitted as one QPSK symbol, the possible signalling points are as in Figure 5. The QPSK symbol carrying the HI is punctured on the DPDCH. However, the puncturing position is TBD.

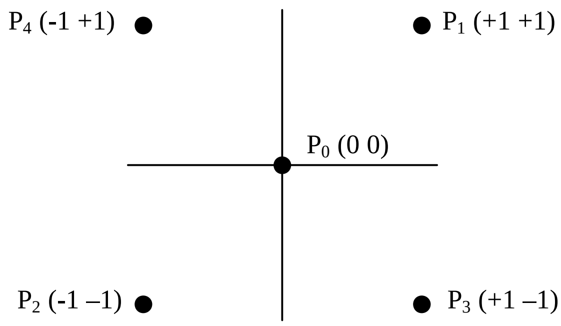


Figure 5. Example of coding of HI.
P_i indicates SCCH-HS #i ($i \in \{1, 2, 3, 4\}$). P_0 indicates that no SCCH-HS carries HS-DSCH-related signalling information to the UE.

Timing relations for HS-DSCH-related downlink signalling

Figure 6 illustrates the timing structure for the HS-DSCH control signalling. The fixed time offset between the SCCH-HS information and the start of the corresponding HS-DSCH TTI equals $\tau_{HS\text{-}DSCH\text{-}control}$ ($2{*}T_{slot}$+m*256chips=(5120+m*256)chips where $0 \le m \le 5$). The time offset between the DL DPCH slot carrying the HI and the start of the SCCH-HS information can vary in the interval [0, T_{slot}] depending on the timing of the downlink DPCH. It may be noted that the start of the HI overlaps with the first slot of the SCCH-HS Figure 4 illustrates the two extreme cases of the timing of DPCH vs SCCH-HS.

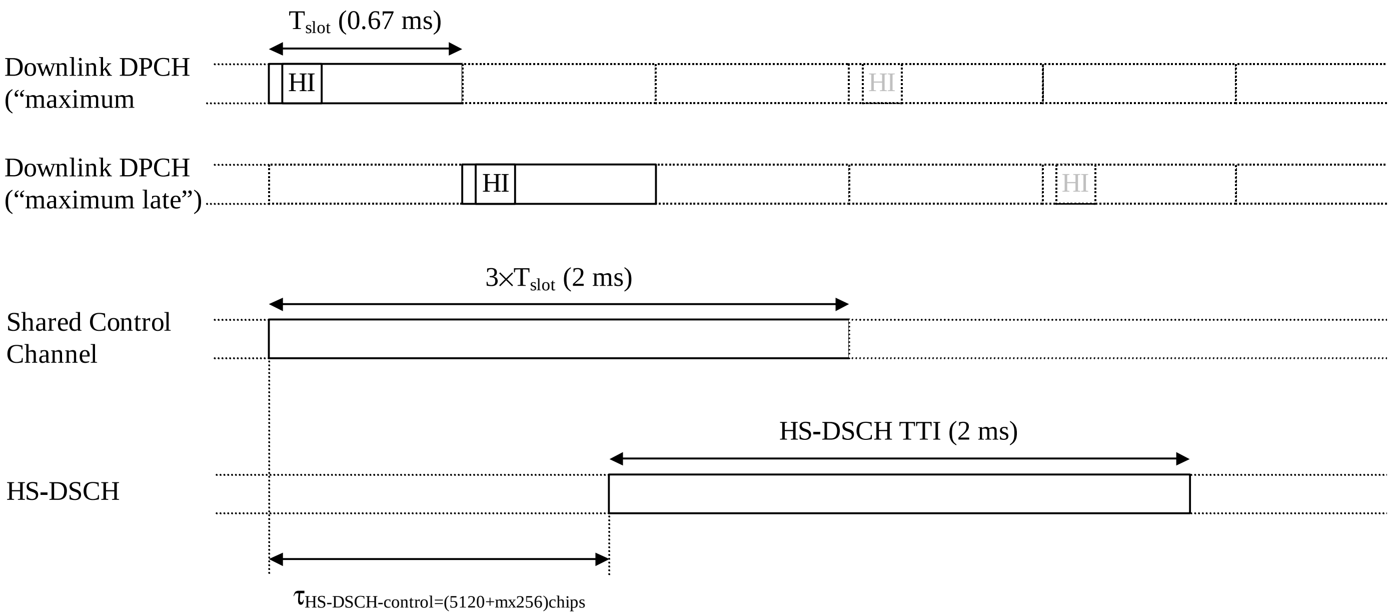


Figure 6. Timing structure for HS-DSCH control signalling

8.1.3 Detailed Structure TDD

The TDD overall downlink signalling structure is a two step approach based on associated dedicated channels and SCCH-HSs. As in Release-99, the associated dedicated channel can also be a fractionated channel for efficient resource usage with a corresponding repetition period in terms of TTIs. The associated dedicated channel carries an high-speed indicator (HI). This HI indicates, that the UE has to read the SCCH-HSs of the same TTI. If the repetition period is larger than 1, the UE has to read in addition the SCCH-HSs of the following TTIs for the whole repetition period to provide full scheduling flexibility. For continuous dedicated channels, the repetition period is consequently set to 1 TTI. The HI has to be sent in parallel or prior to the SCCH-HSs.

8.1.3.1 SCCH-HS

For each HS-DSCH TTI, each SCCH-HS carries HS-DSCH-related downlink signalling for one UE. The following information is carried on the SCCH-HS:

- UE Identifier
  Since the SCCH-HS may be being monitored by more than one UE, an identifier is required to identify the intended recipient. The UE Identifier is a 10 bit field that is combined with the CRC. Generation and length of the CRC field is ffs.

- Transport-format and Resource related Information (TFRI)
  The TFRI includes information about the dynamic part of the HS-DSCH transport format that identifies to the UE which resources are being used for the HS-DSCH, and how the data is being carried by these resources.
  The TFRI information fields required by the UE are:

Table 1

Parameter	1.28 Mcps TDD (5ms TTI)	3.84 Mcps TDD (10ms TTI)
Resource Allocation	12 bits (code + timeslot allocation)	16 bits (code + timeslot allocation)
Modulation	1 bit	1 bits
Transport Block Set Size and Transport Channel ID	6 bits	9 bits

- HARQ
  This is information that identifies to the UE the relationship between the current data being sent and other blocks sent previously.
  - HARQ process identifier = 3 bits
  - New data indicator =1 (2 bits ffs)
  - Incremental redundancy version number = 2 bits
- Uplink Synchronisation for 1.28 Mcps
  2 Synchronisation bits (SS) are used to maintain synchronisation for the associated High-Speed Information Channel (HICH).

- TPC
  2 bits TPC bits are used optionally to control the power of the associated HICH

8.1.3.2 Downlink DPCH

If a downlink DPCH is present, it carries an HS-DSCH Indicator (HI), in addition to non-HS-DSCH-related physical-layer signalling and DCH transport channels. The HI consists of one information bit. If the HI is set, the UE has to read all predefined HS-SCCH in the same TTI. In case of a fractional DPCH, the UE hat to read the predefined HS-SCCHs in all TTIs of the fraction period. If the UE detects that one of the HS-SCCH carries data for the UE, the UE should be able to stay on the same control channel with continuous data transmission. The maximum allocated number of HS-SCCHs to be read by the UE per TTI are defined by higher layers. A UE shall not be required to read more than 4 HS-

SCCHs. The HI information is repetition coded to 2 coded bits as shown in Table 2

HI Bits	HI command	Meaning
00	'Not-Set'	No HS-DSCH transmission
11	'Set'	Read all allocated HS-SCCH

Table 2: HI Bit Pattern

Table 2 shows the coding of the HI and Figure 7 the position of the HI information in a 1.28 Mcps burst prior to the TFCI field close to the midambles.

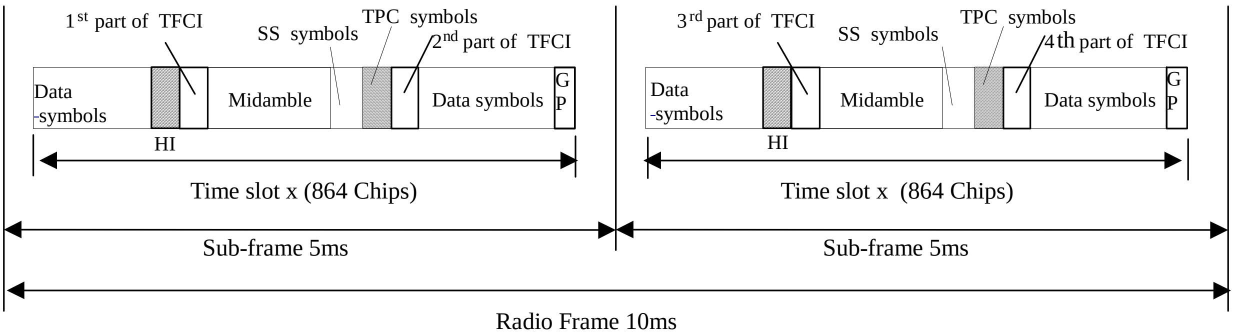


Figure 7: Position of HI information in the traffic burst in case of TFCI, TPC and SS in 1.28 Mcps TDD

8.1.3.3 Timing relations for the HS-DSCH related Downlink Signalling

Figure 8 depicts the timing structure of 1.28 Mcps TDD for HS-DSCH control signalling if continuos DPCH is used. The SCCH-HS has to be in parallel or later than the latest HI in the given timeslot. There is a minimum of 2 timeslots between the SCCH-HS and the HS-DSCH.

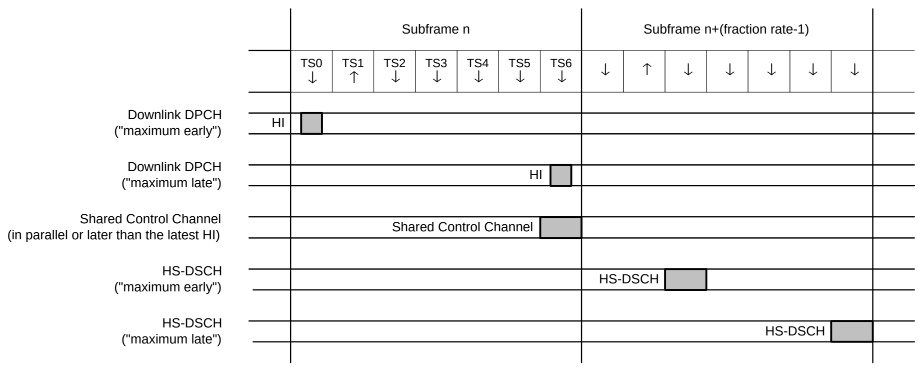


Figure 8: 1.28 Mcps Timing structure for HS-DSCH downlink control signalling using continuos DPCH

Figure 9 depicts the timing structure of 1.28Mcps TDD for HS-DSCH control signalling if fractionated DPCH is used. The latest SCCH-HS has to be in parallel or later than the latest HI timeslot shifted by (fraction rate – 1) sub-frames.

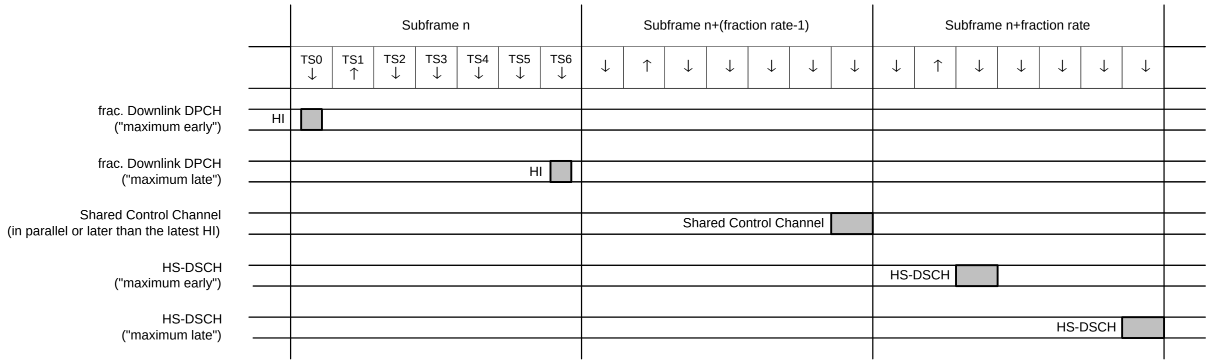


Figure 9: 1.28 Mcps Timing structure for HS-DSCH downlink control signalling using fractionated DPCH

8.1.4 Other aspects

{This section should describe how the downlink signalling operates in soft-handoff mode etc.}

8.2 Uplink

8.2.1 Overall Structure

In FDD, the HS-DSCH related uplink signalling uses DPCCH-HS with SF=256 that is code multiplexed with the existing dedicated uplink physical channels. The HS-DSCH related uplink signalling consists of H-ARQ acknowledgement and channel quality indicator.

In contrast to FDD, the TDD UE does not use its dedicated channel in uplink for transmitting ACK/NACK information, due to the associated fractionated dedicated channel option. To enable a SYNC UL scheme for HARQ, the UE will use a shared uplink resource for transmitting ACK/NACK information. The relation between the SCCH-HS in DL and shared UL resource can be pre-defined and is not signalled dynamically on the SCCH-HS.

8.2.2 Detailed Structure FDD

8.2.2.1 HS-DSCH Associated Uplink Dedicated Control Channel

The following information is carried on the HS-DSCH associated uplink dedicated control channel (DPCCH-HS):

- H-ARQ acknowlegemnt

A 1-bit Ack/Nack indication is used for a H-ARQ acknowledgement. The acknowlegement bit is repetition coded to 10 bits and transmitted in one slot. H-ARQ acknowledgement field is DTX'ed when there is no ACK/NACK inforamtion being sent.

- Measurement feedback information

Measurement feedback information contains channel quality indicator that may be used to select transport format and resource by HS-DSCH serving Node-B. A [5]-bit channel quality indicator is coded and transmitted over two slots. The transmission cycle and timing for channel quality indicator is determined by UTRAN and signalled by higher layer. (*Note: It is to be determined whether the transmission cycle is influenced by HS-DSCH activity* or downlink channel quality) Details for measurement feedback procedure is described in section 8.2.2.2.
The channel quality indicator consists of a recommended TFRC provided by the UE to Node-B. The recommended TFRC is chosen by the UE from a TFRC reference list. An example of TFRC reference list is provided in section 8.2.2.2.3.

The format for the additional DPCCH is shown in Figure 10. The ACK/NACK message is transmitted with a power offset ΔP_{AN} relative to the Release '99 uplink DPCCH. The power offset ΔP_{AN} is a higher-layer parameter.

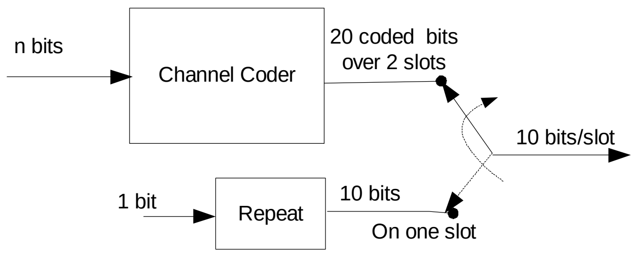


Figure 10. Format for additional DPCCH for HS-DSCH related uplink signalling

For TDD, the structure is TBD.

8.2.2.2 Measurement feedback procedure

8.2.2.2.1 UE procedure

This section provides an example for UE internal procedure used in adaptive modulation and coding operation. (*Note: following procedures need to be checked by WG4*)

UE measures a DL channel quality indicator from P-CPICH (alternatively S-CPICH in case of beamforming with S-CPICH is used). Taking into account the default power offset, P_{hs} , of the HS-DSCH code channel relative to P-CPICH (or S-CPICH), UE checks from its internal mapping table which TFRC from the TFRC reference list, it would be able to receive in this channel condition.

The UE uses the $BLER_{threshold}$ criteria to determine which TFRC it is able to receive in given channel conditions. If the channel quality, measured from P-CPICH (or S-CPICH in case beamforming with S-CPICH is used) indicates that TFRC x would be received with BLER< $BLER_{threshold}$ with HS-DSCH code channel power offset<y dB (steps *TBD*) in addition to the default power level, but TFRC x+1 would be received with BLER>$BLER_{threshold}$, then UE will report TFRC x and the required power offset y back to the network.

The UE should report a TFRC from the reference list together with a power offset at the transmission timing defined by higher layer signalling.

8.2.2.2.2 Parameters provided to the UE measurement feedback operation

Following connection specific parameters are informed to the UE by higher layer signalling:

1) P_{hs}, default power offset between HS-DSCH code channel and P-CPICH (or S-CPICH in case beamforming with S-CPICH is used).

2) BLER $_{threshold}$, BLER value that UE uses for selecting the TFRC. Possible values of the BLER $_{threshold}$ are FFS.

3) Measurement feedback cycle *k*. *k* has a possible value of [1,5, 10,20,,40,80] corresponding to the feedback cycle of [2,10,20,40,80, 160] msec. In addition, with the indication *k*=0, measurement feedback can be shut off completely. (*Note: It is to be determined whether k can have two values, in which case that k is selected depending on HS-DSCH activity*.)

4) Measurement feedback offset *l*. The exact definition of *l* is to be determined.

The use for the measurement feedback cycle *k* and feedback offset *l* is illustrated in Figure 11. (*Note: The timing relations in the figure do not reflect the differences in DPCH frame offset.)*

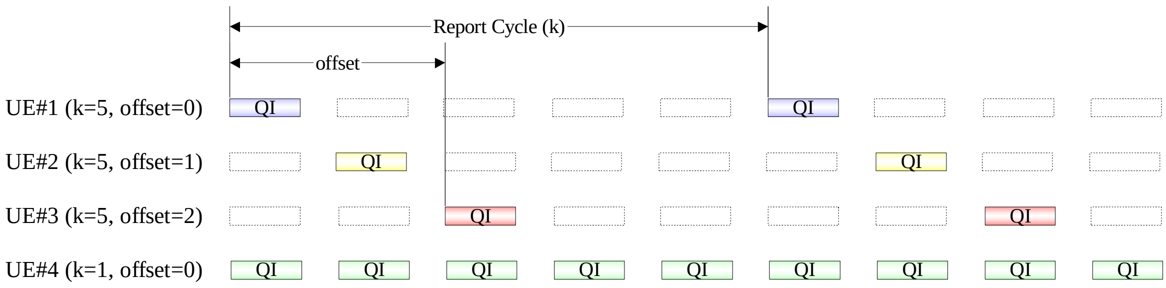


Figure 11 An illustration of feedback measurement transmission timing

8.2.2.2.3 Reference TFRC list

Only one reference TFRC list is specified, that all UEs should use for creating the measurement report. Each TFRC contains modulation, transport block set size, and number of code channels

Example of TFRC reference list with 6 TFRCs is shown in **Table 3**

Table 3. An example of a TFRC reference list

TFRCs	Modulation	Transport block set size	# of code channels
TFRC1	QPSK	1200	5
TFRC2	QPSK	2400	5
TFRC3	QPSK	3600	5
TFRC4	16QAM	4800	5
TFRC5	16QAM	6000	5
TFRC6	16QAM	7200	5

8.2.2.2.4 Measurement feedback definition

Measurement report can take up to [32] values. It contains one TFRC at a time from the reference list and a power offset value.

An example of possible UE measurement report list for 6 TFRCs and intermediate steps of 1 dB for power offset are shown in Table 4

Table 4 An example of a measurement report list

TFRC	Power offset	Measurement report value
TFRC1	12 dB	0
	11 dB	1
	10 dB	2
	9 dB	3
	8 dB	4
	7 dB	5
	6 dB	6
	5 dB	7
	4 dB	8
	3 dB	9
	2 dB	10
	1 dB	11
	0 dB	12
TFRC2	2 dB	13
	1 dB	14
	0 dB	15
TFRC3	2 dB	16
	1 dB	17
	0 dB	18

TFRC4	2 dB	19
	1 dB	20
	0 dB	21
TFRC5	2 dB	22
	1 dB	23
	0 dB	24
TFRC6	2 dB	25
	1 dB	26
	0 dB	27
NA	NA	28
NA	NA	29
NA	NA	30
NA	NA	31

8.2.3 Detailed Structure TDD

This section describes the detailed structure of the TDD HSDPA uplink signalling.

8.2.3.1 HICH

This section considers the structure of the HSDPA Information Channel (HICH). Three data fields have been identified that must be carried by the HICH:

- ACK / NAK
  If the transport block set received by the UE on the associated HS-DSCH is received without error, then an acknowledgement (ACK) is sent to the NodeB. If an error is detected, a negative acknowledgement (NAK) is sent. The UE can detect an error in the transport block set via the CRC. The ACK / NAK signaling consists of only a single bit of information, and the following mapping is proposed :

Message	Bit Field Representation
ACK	1
NAK	0

Table 5: Mapping of ACK / NAK Message to Bit Field

- Quality Indicator
  In order to assist the NodeB in selecting the appropriate modulation scheme and coding rate for the SIR currently being experienced by the UE, the UE sends quality information to the NodeB. This quality information is the SIR itself or is related to the SIR, as measured on the lateststst HS-DSCH transmission. If the HS-DSCH uses multiple timeslots, then quality information related to the average SIR value over those timeslots may be reported.

- TPC
  The HICH carries 2 TPC bits which are set by the UE based on the received SCCH-HS SIR. An outer loop algorithm for setting the target SIR is ffs.

8.2.3.2 Uplink DPCH

The uplink DPCH is not affected

8.2.3.3 Timing relations for the HS-DSCH related Uplink Signalling

Figure 12 depicts the timing structure for 1.28 Mcps HS-DSCH uplink control signalling. There is a minimum of 8 timeslots between the HS-DSCH and associated HICH allocation.

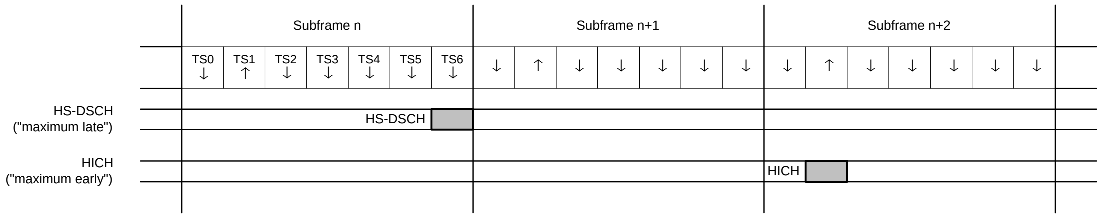


Figure 12: 1.28 Mcps Timing structure for HS-DSCH uplink control signalling

Figure 13 depicts the timing structure for 1.28 Mcps HS-DSCH up- and downlink control signalling. This case shows a slot configuration with minimum DL timeslots.

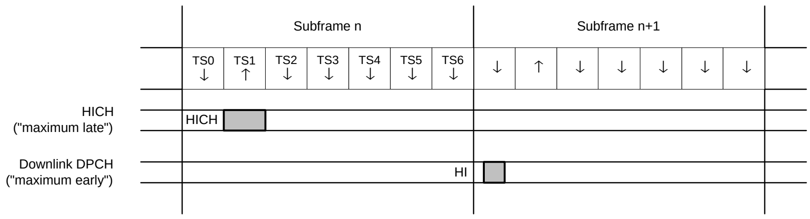


Figure 13: 1.28 Mcps Timing structure for HS-DSCH up- and downlink control signalling min. DL timeslots

Figure 14 depicts the timing structure for 1.28 Mcps HS-DSCH up- and downlink control signalling. This case shows a slot configuration with maximum DL timeslots.

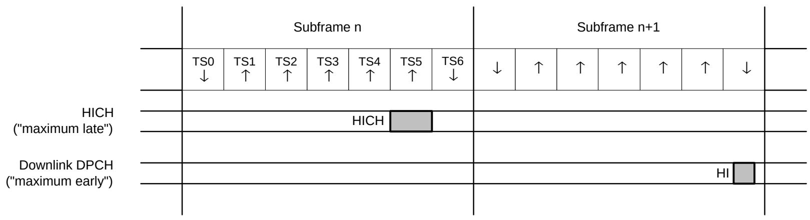


Figure 14: 1.28 Mcps Timing structure for HS-DSCH up- and downlink control signalling max. DL timeslots

8.2.3 Other aspects *(we need to find a suitable name)*

{This section should describe how the uplink signalling operates in soft-handoff mode etc.}

9 UE Capability

This section is tentative and subject to further revisions.

9.1 HS-DSCH UE capability parameters

Table 6. UE radio access capability parameter value ranges

		UE radio access capability parameter	Value range
RLC and MAC-HS parameters		Total buffer size	
		Maximum number of AM RLC entities	
PHY parameters	Transport channel parameters in downlink	Maximum number of HS-DSCH transport-channel bits that can be received within an HS-DSCH TTI	[1600], [4000], [6400], [9600], [14400], [19200], [27200]
	Physical channel parameters in downlink	Maximum number of HS-DSCH codes received	5, 10, 15
		Total number of soft channel bits	[19200], [38400], [48000], [57600], [76800], [96000], [115200], [153600], [172800]
		Minimum inter-TTI interval	1, 2, 3 NOTE: the interval depicts the distance from the beginning of a TTI to the beginning of the next TTI assigned to the UE

9.2 Reference UE radio access capability combinations

Some reference combinations for HS-DSCH capabilities are shown in Table 7. These combinations are specific for HS-DSCH and are thus separate from Rel-99 combinations.

Table 7. UE radio access capability parameter combinations, DL HS-DSCH parameters

Reference combination	1.2 Mbps capability	3.6 Mbps capability	7 Mbps capability	10 Mbps capability
RLC and MAC-HS parameters				
Total buffer size (kbytes)	tbd	tbd	tbd	tbd
Maximum number of AM RLC entities	tbd	tbd	tbd	tbd
Transport channel parameters				
Maximum number of HS-DSCH transport-channel bits that can be received within an HS-DSCH TTI	9600	9600	19200	27200
Physical channel parameters				
Maximum number of HS-DSCH codes received	5	5	10	15
Minimum inter-TTI interval	3	1	1	1
Total number of soft channel bits	19200	57600	115200	172800

The limit on the minimum number of UEs within a TTI and the lowest capability UE class should be defined in such a way that prevents under-utilization of the HS-DSCH resources.

10 Overview of the changes required in the specification

{This section should describe overview of the changes required in the physical layer spec 25.211 to 25.214 etc. to support HS-DSCH}

11 Informative Annex A

Requirements for the evaluation of techniques for High Speed Downlink Packet Access

The following considerations should be taken into account in the evaluation of the different techniques proposed for HSDPA.

1. The focus shall be on the streaming, interactive and background services. It should be noted that it may not be possible to simultaneously optimise the characteristics of HSDPA for all of the above traffic classes.
2. System performance improvement shall be obtained with the concomitant reduction in delay of service.
3. Priority shall be given to urban environments and then to indoor deployments. The techniques shall not be limited to these environments however.
4. The techniques accepted shall be optimised at speeds typical of urban environments but techniques should apply at other speeds also. Full mobility shall be supported, i.e., mobility should be supported for high-speed cases also, but optimisation should be for low-speed to medium-speed scenarios.
5. Features or group of features considered should demonstrate significant incremental gain.
6. Features accepted shall provide the benefit at reasonable cost to the operators. The value added per feature should be considered in the evaluation.
7. The techniques should be compatible with advanced antenna and receiver techniques.
8. The techniques should take into account the impact on R99 networks both from a protocol and hardware perspective.
9. The choice of techniques (such as HARQ) shall take into account UE processing time and memory requirements.
10. The UE complexity shall be minimised for a given level of system performance.

An evolutionary philosophy shall be adopted as opposed to a revolutionary one in adopting new techniques and architectures.

Annex B: History

V0.0.1	**8/31/01**	**AG**			**Initial TR as per agreement in RAN1#21**		
V0.0.2	9/4/01	AG			Revised as per comments received in the reflector		
V0.0.3	9/7/01	AG			Revised as per comments received on the reflector		
V0.0.4	9/10/01	AG			Revised sections 8.2 and 9.1.2 . New Tdoc #0989		
V0.1.0	11/07/01	AG			Revised section 4.1, 5.9		
V0.1.1	11/23/01	AG			Revised relevant sections as per text proposals		
V0.1.2	11/30/01	AG			Revised as per comments received on the reflector		
V0.2.0	12/04/01	AG			Cleaned up RAN#1 version		
V1.0.0	12/04/01	AG			RAN version to be presented at the RAN#14 meeting		