

**TSG-RAN Meeting #13**  
**Beijing, China, 18 - 21, September, 2001**

**RP-010529**

**Title:** Agreed CRs (Rel-4) to TS 25.222

**Source:** TSG-RAN WG1

**Agenda item:** 8.1.4

No.	Spec	CR	Rev	R1 T-doc	Subject	Release	Cat	W/I Code	V_old	V_new
1	25.222	058	-	R1-01-0784	5ms TTI for PRACH for 1.28 Mcps TDD	REL-4	F	LCRTDD-Phys	4.0.0	4.1.0
2	25.222	060	-	R1-01-0812	A correction on the meaning of FPACH in TS 25.222	REL-4	F	LCRTDD-Phys	4.0.0	4.1.0

CR-Form-v3

## CHANGE REQUEST

⌘ **25.222 CR 058** ⌘ rev **-** ⌘ Current version: **4.0.0** ⌘

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**Proposed change affects:** ⌘ (U)SIM  ME/UE  Radio Access Network  Core Network

<b>Title:</b>	⌘ 5ms TTI for PRACH for 1.28 Mcps TDD		
<b>Source:</b>	⌘ TSG RAN WG1		
<b>Work item code:</b>	⌘ LCRTDD-Phys	<b>Date:</b>	⌘ 22.08.2001
<b>Category:</b>	⌘ <b>F</b>	<b>Release:</b>	⌘ REL-4
Use <u>one</u> of the following categories: <b>F</b> (essential correction) <b>A</b> (corresponds to a correction in an earlier release) <b>B</b> (Addition of feature), <b>C</b> (Functional modification of feature) <b>D</b> (Editorial modification) Detailed explanations of the above categories can be found in 3GPP TR 21.900.		Use <u>one</u> of the following releases: 2 (GSM Phase 2) R96 (Release 1996) R97 (Release 1997) R98 (Release 1998) R99 (Release 1999) REL-4 (Release 4) REL-5 (Release 5)	

<b>Reason for change:</b>	⌘ The TTI for PRACH for 1.28 Mcps TDD can also be 5ms, which is currently not included in TS25.222
<b>Summary of change:</b>	⌘
<b>Consequences if not approved:</b>	⌘ Erroneous description of multiplexing chain

<b>Clauses affected:</b>	⌘		
<b>Other specs affected:</b>	<input type="checkbox"/> Other core specifications <input type="checkbox"/> Test specifications <input type="checkbox"/> O&M Specifications	⌘	
<b>Other comments:</b>	⌘		

### How to create CRs using this form:

Comprehensive information and tips about how to create CRs can be found at: [http://www.3gpp.org/3G\\_Specs/CRs.htm](http://www.3gpp.org/3G_Specs/CRs.htm). Below is a brief summary:

- 1) Fill out the above form. The symbols above marked ⌘ contain pop-up help information about the field that they are closest to.
- 2) Obtain the latest version for the release of the specification to which the change is proposed. Use the MS Word "revision marks" feature (also known as "track changes") when making the changes. All 3GPP specifications can be downloaded from the 3GPP server under <ftp://www.3gpp.org/specs/> For the latest version, look for the directory name with the latest date e.g. 2000-09 contains the specifications resulting from the September 2000 TSG meetings.
- 3) With "track changes" disabled, paste the entire CR form (use CTRL-A to select it) into the specification just in front of the clause containing the first piece of changed text. Delete those parts of the specification which are not relevant to the change request.

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## 4 Multiplexing, channel coding and interleaving

### 4.1 General

Data stream from/to MAC and higher layers (Transport block / Transport block set) is encoded/decoded to offer transport services over the radio transmission link. Channel coding scheme is a combination of error detection, error correcting (including rate matching), and interleaving and transport channels mapping onto/splitting from physical channels.

In the UTRA-TDD mode, the total number of basic physical channels (a certain time slot one spreading code on a certain carrier frequency) per frame is given by the maximum number of time slots which is 15 and the maximum number of CDMA codes per time slot.

### 4.2 Transport channel coding/multiplexing

Figure 1 illustrates the overall concept of transport-channel coding and multiplexing. Data arrives to the coding/multiplexing unit in form of transport block sets, once every transmission time interval. The transmission time interval is transport-channel specific from the set {5 ms<sup>(\*)</sup>, 10 ms, 20 ms, 40 ms, 80 ms}.

Note: <sup>(\*)</sup> may be applied for PRACH for 1.28 Mcps TDD

The following coding/multiplexing steps can be identified:

- add CRC to each transport block (see subclause 4.2.1);
- TrBk concatenation / Code block segmentation (see subclause 4.2.2);
- channel coding (see subclause 4.2.3) ;
- radio frame size equalization (see subclause 4.2.4);
- interleaving (two steps, see subclauses 4.2.5 and 4.2.10);
- radio frame segmentation (see subclause 4.2.6);
- rate matching (see subclause 4.2.7);
- multiplexing of transport channels (see subclause 4.2.8);
- bit scrambling (see subclause 4.2.9);
- physical channel segmentation (see subclause 4.2.10);
- sub-frame segmentation(see subclause 4.2.12 only for 1.28Mcps TDD)
- mapping to physical channels (see subclause 4.2.13).

The coding/multiplexing steps for uplink and downlink are shown in figures 1 and 2.

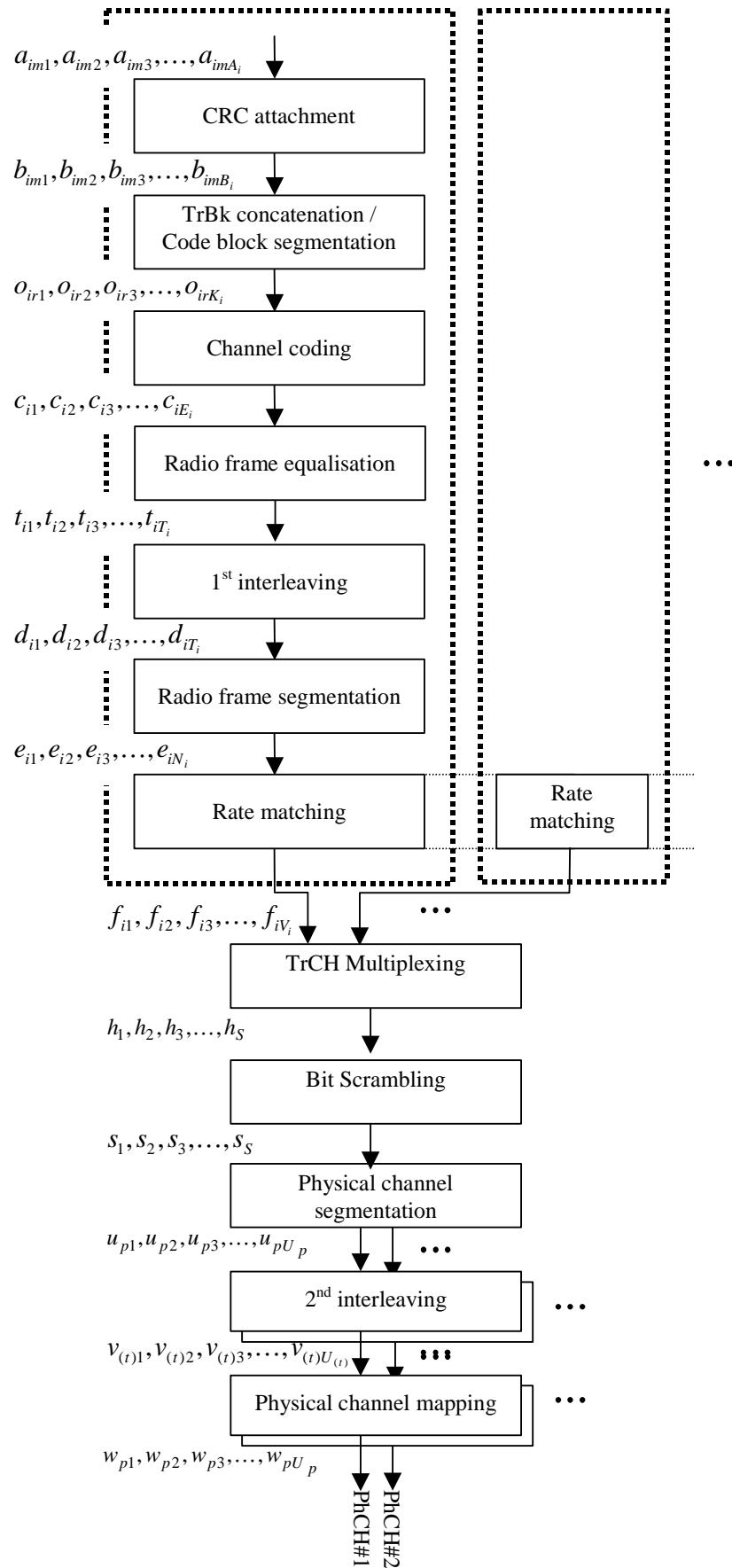
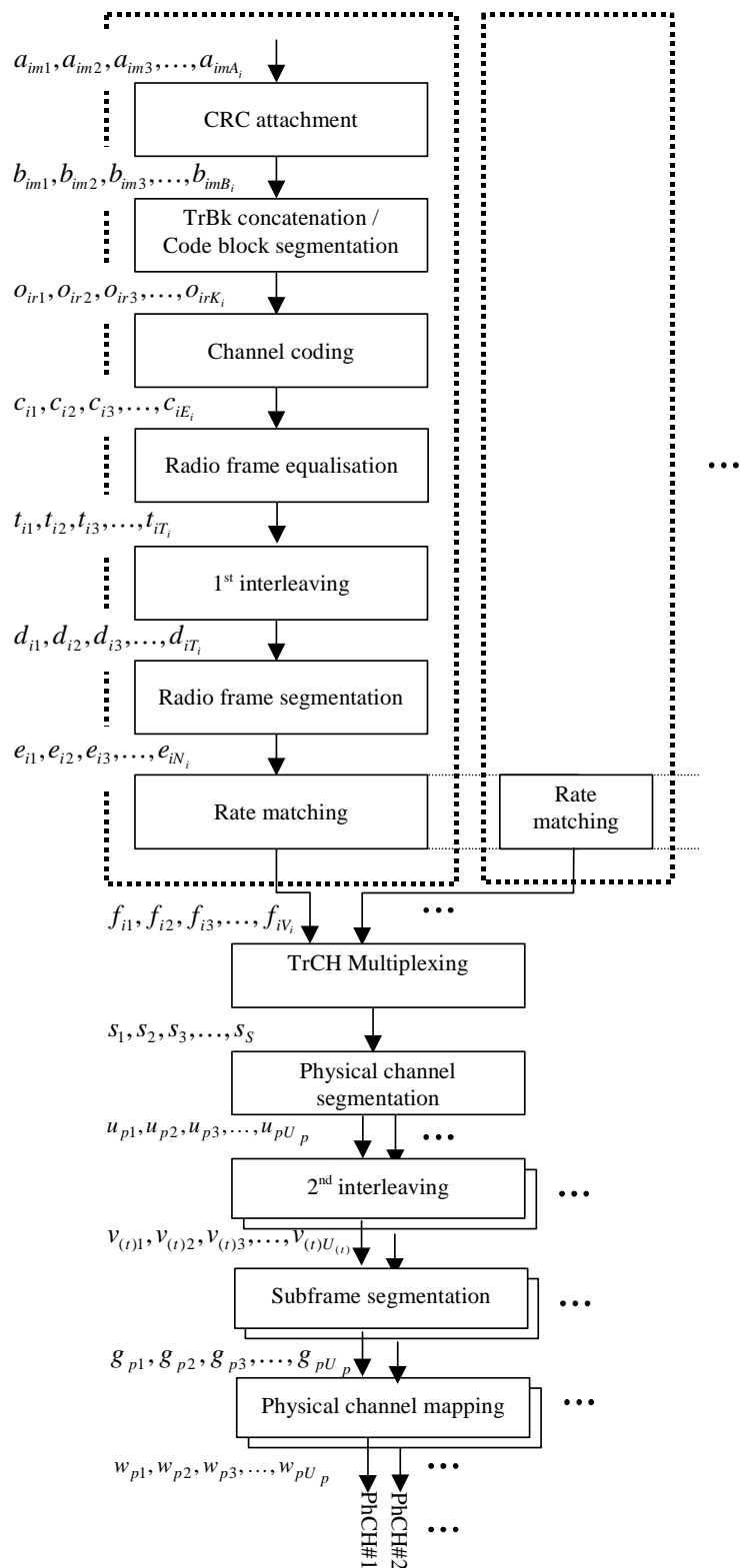


Figure 1: Transport channel multiplexing structure for uplink and downlink for 3.84Mcps TDD



**Figure 2: Transport channel multiplexing structure for uplink and downlink of 1.28Mcps TDD**

Primarily, transport channels are multiplexed as described above, i.e. into one data stream mapped on one or several physical channels. However, an alternative way of multiplexing services is to use multiple CCTrCHs (Coded Composite Transport Channels), which corresponds to having several parallel multiplexing chains as in figures 1 and 2, resulting in several data streams, each mapped to one or several physical channels.

## 4.2.5 1st interleaving

The 1<sup>st</sup> interleaving is a block interleaver with inter-column permutations. The input bit sequence to the block interleaver is denoted by  $x_{i,1}, x_{i,2}, x_{i,3}, \dots, x_{i,X_i}$ , where  $i$  is TrCH number and  $X_i$  the number of bits. Here  $X_i$  is guaranteed to be an integer multiple of the number of radio frames in the TTI. The output bit sequence from the block interleaver is derived as follows:

- 1) select the number of columns  $C1$  from table 5 depending on the TTI. The columns are numbered 0, 1, ...,  $C1 - 1$  from left to right.

- 2) determine the number of rows of the matrix,  $R1$  defined as

$$R1 = X_i / C1.$$

The rows of the matrix are numbered 0, 1, ...,  $R1 - 1$  from top to bottom.

- 3) write the input bit sequence into the  $R1 \times C1$  matrix row by row starting with bit  $x_{i,1}$  in column 0 of row 0 and ending with bit  $x_{i,(R1 \times C1)}$  in column  $C1 - 1$  of row  $R1 - 1$ :

$$\begin{bmatrix} x_{i,1} & x_{i,2} & x_{i,3} & \dots & x_{i,C1} \\ x_{i,(C1+1)} & x_{i,(C1+2)} & x_{i,(C1+3)} & \dots & x_{i,(2 \times C1)} \\ \vdots & \vdots & \vdots & \dots & \vdots \\ x_{i,((R1-1) \times C1+1)} & x_{i,((R1-1) \times C1+2)} & x_{i,((R1-1) \times C1+3)} & \dots & x_{i,(R1 \times C1)} \end{bmatrix}$$

- 4) Perform the inter-column permutation for the matrix based on the pattern  $\langle P1_{C1}(j) \rangle_{j \in \{0,1,\dots,C1-1\}}$  shown in table 5, where  $P1_{C1}(j)$  is the original column position of the  $j$ -th permuted column. After permutation of the columns, the bits are denoted by  $y_{i,k}$ :

$$\begin{bmatrix} y_{i,1} & y_{i,(R1+1)} & y_{i,(2 \times R1+1)} & \dots & y_{i,((C1-1) \times R1+1)} \\ y_{i,2} & y_{i,(R1+2)} & y_{i,(2 \times R1+2)} & \dots & y_{i,((C1-1) \times R1+2)} \\ \vdots & \vdots & \vdots & \dots & \vdots \\ y_{i,R1} & y_{i,(2 \times R1)} & y_{i,(3 \times R1)} & \dots & y_{i,(C1 \times R1)} \end{bmatrix}$$

- 5) Read the output bit sequence  $y_{i,1}, y_{i,2}, y_{i,3}, \dots, y_{i,(C1 \times R1)}$  of the block interleaver column by column from the inter-column permuted  $R1 \times C1$  matrix. Bit  $y_{i,1}$  corresponds to row 0 of column 0 and bit  $y_{i,(R1 \times C1)}$  corresponds to row  $R1 - 1$  of column  $C1 - 1$ .

**Table 5 Inter-column permutation patterns for 1st interleaving**

TTI	Number of columns $C1$	Inter-column permutation patterns $\langle P1_{C1}(0), P1_{C1}(1), \dots, P1_{C1}(C1-1) \rangle$
5ms <sup>(*)</sup> , 10 ms	1	$\langle 0 \rangle$
20 ms	2	$\langle 0, 1 \rangle$
40 ms	4	$\langle 0, 2, 1, 3 \rangle$
80 ms	8	$\langle 0, 4, 2, 6, 1, 5, 3, 7 \rangle$

<sup>(\*)</sup> can be used for PRACH for 1.28 Mcps TDD

## 4.2.8 TrCH multiplexing

Every 10 ms, one radio frame from each TrCH is delivered to the TrCH multiplexing. These radio frames are serially multiplexed into a coded composite transport channel (CCTrCH). If the TTI is smaller than 10ms, then no TrCH multiplexing is performed.

The bits input to the TrCH multiplexing are denoted by  $f_{i,1}, f_{i,2}, f_{i,3}, \dots, f_{i,V_i}$ , where  $i$  is the TrCH id number and  $V_i$  is the number of bits in the radio frame of TrCH  $i$ . The number of TrCHs is denoted by  $I$ . The bits output from TrCH multiplexing are denoted by  $h_1, h_2, h_3, \dots, h_S$ , where  $S$  is the number of bits, i.e.  $S = \sum_i V_i$ . The TrCH multiplexing is

defined by the following relations:

$$h_k = f_{1,k} \quad k = 1, 2, \dots, V_1$$

$$h_k = f_{2,(k-V_1)} \quad k = V_1+1, V_1+2, \dots, V_1+V_2$$

$$h_k = f_{3,(k-(V_1+V_2))} \quad k = (V_1+V_2)+1, (V_1+V_2)+2, \dots, (V_1+V_2)+V_3$$

...

$$h_k = f_{I,(k-(V_1+V_2+\dots+V_{I-1}))} \quad k = (V_1+V_2+\dots+V_{I-1})+1, (V_1+V_2+\dots+V_{I-1})+2, \dots, (V_1+V_2+\dots+V_{I-1})+V_I$$

3GPP TSG RAN Meeting #13  
Beijing, China, 18<sup>th</sup> – 21<sup>st</sup>, September, 2001

**R1-01-0812**

CR-Form-v4

## CHANGE REQUEST

⌘ **25.222 CR 060** ⌘ rev **-** ⌘ Current version: **4.0.0** ⌘

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**Proposed change affects:** ⌘ (U)SIM  ME/UE  Radio Access Network  Core Network

<b>Title:</b>	⌘ A correction on the meaning of FPACH in TS 25.222		
<b>Source:</b>	⌘ TSG RAN WG1		
<b>Work item code:</b>	⌘ LCRTDD-Phys	<b>Date:</b>	⌘ Aug.15 <sup>th</sup> , 2001
<b>Category:</b>	⌘ <b>F</b> Use <u>one</u> of the following categories: <b>F</b> (correction) <b>A</b> (corresponds to a correction in an earlier release) <b>B</b> (addition of feature), <b>C</b> (functional modification of feature) <b>D</b> (editorial modification) Detailed explanations of the above categories can be found in 3GPP TR 21.900.	<b>Release:</b>	⌘ <b>REL-4</b> Use <u>one</u> of the following releases: 2 (GSM Phase 2) R96 (Release 1996) R97 (Release 1997) R98 (Release 1998) R99 (Release 1999) REL-4 (Release 4) REL-5 (Release 5)

<b>Reason for change:</b>	⌘ The meaning of FPACH in TS 25.222 is not consistent with that of TS 25.221.
<b>Summary of change:</b>	⌘ The meaning of FPACH in the table of contents and subclause 4.4.3 is corrected.
<b>Consequences if not approved:</b>	⌘ Meaning of FPACH will be confused.

<b>Clauses affected:</b>	⌘ Table of contents and subclause 4.4.3		
<b>Other specs affected:</b>	⌘ <input type="checkbox"/> Other core specifications	⌘ <input type="checkbox"/>	
	<input type="checkbox"/> Test specifications		
	<input type="checkbox"/> O&M Specifications		
<b>Other comments:</b>	⌘		

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### 4.4.3 Coding of the ForwardFast Physical Access Channel (FPACH) information bits

The FPACH burst is composed by 32 information bits which are block coded and convolutional coded, and then delivered in one sub-frame as follows:

1. The 32 information bits are protected by 8 parity bits for error detection as described in sub-clause 4.2.1.1.
2. Convolutional code with constraint length 9 and coding rate  $\frac{1}{2}$  is applied as described in sub-clause 4.2.3.1. The size of data block  $c(k)$  after convolutional encoder is 96 bits.
3. To adjust the size of the data block  $c(k)$  to the size of the FPACH burst, 8 bits are punctured as described in sub-clause 4.2.7 with the following clarifications:
  - $N_{i,j}=96$  is the number of bits in a radio sub-frame before rate matching
  - $\Delta N_{i,j} = -8$  is the number of bits to punctured in a radio sub-frame
  - $e_{mi} = a \times N_{ij}$

The 88 bits after rate matching are then delivered to the intra-frame interleaving.

4. The bits in input to the interleaving unit are denoted as  $\{x(0), \dots, x(87)\}$ . The coded bits are block rectangular interleaved according to the following rule: the input is written row by row, the output is read column by column.

$$\begin{bmatrix} x(0) & x(1) & x(2) & \dots & x(7) \\ x(8) & x(9) & x(10) & \dots & x(15) \\ \vdots & \vdots & \vdots & \dots & \vdots \\ x(80) & x(81) & x(82) & \dots & x(87) \end{bmatrix}$$

Hence, the interleaved sequence is denoted by  $y(i)$  and are given by:

$$y(0), y(1), \dots, y(87)=x(0), x(8), \dots, x(80), x(1), \dots, x(87).$$