TSG-RAN meeting #4
Miami, 17th – 19 th June, 1999

TSG RAN#4 (99)~~339~~383

Agenda Item:

Source: **RAN WG4**

To: **TSG RAN**

Title: **Liaison statement on Impact of OHG harmonization recommendation on UTRA/FDD and UTRA/TDD**

Document for: **Discussion and Information**

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1 Introduction

At its meeting in Miami on 14th – 16th June, RAN WG4 commenced discussions about the implications of the OHG Recommendation on harmonisation of the two main CDMA-based proposals for IMT 2000 (UTRA and cdma2000) on its work. WG4 concluded that the change of chip rate proposed by OHG will have an impact on its specifications. WG4 has noted that work on reviewing the changes proposed by OHG has already started in WG1. In order to initiate similar progress in TSG-RAN WG4 without impacting the WG4 work plan (TSGR4#4(99)190, approved in WG4 #4 meeting at Stockholm) have been started.

In this liaison statement, WG4 identifies some of the key parameters of the current UTRA/FDD and UTRA/TDD specifications which need to be modified to implement the OHG recommendation. This liaison statement from RAN WG4 provides TSG RAN with the opinion of RAN WG4 on the impact of harmonisation, to assist TSG RAN in making a decision to endorse the change of the chip rate.

2 Procedure of WG4

In order to progress this issue in WG4, the following procedure is proposed:

- As the number of affected parameters are few in WG4, this LS to TSG-RAN includes information on both the current chip rate 4.096 Mcps and 3.84 Mcps wherever possible.
- If TSG-RAN decides to change the chip rate then the agreed parameters in the specifications will be modified by their editors before the next meeting of WG4.
- Some parameters like reference sensitivity will require further simulation. As soon as these are available they should be discussed in WG4 for incorporation in the WG4 specifications.

3 Effects of 3.84 Mcps on the FDD mode

3.1 Channel spacing

This items refers to TS25.101 (v1.2.0) section 5.4.1.

It is proposed that the chip rate change should not impact the current agreed channel spacing. Therefore the nominal channel spacing should still be maintained as 5 MHz , but can be adjusted to optimise performance in a particular deployment.

3.2 Roll-Off Factor

This item refers to TS25.101(v1.2.0) section 6.8.1 Pulse shaping and TS25.201(v2.0.0) 7.2.3 Modulation & spreading.

The current roll-off factor is derived from the channel spacing and chip rate. Although it is possible to change the roll-off factor it is felt the current roll-factor should be maintained in order to provide the flexibility in the allocation of channel spacing for inter operator and intra-operator spacing. Either the channels can be pushed closer together or left at the same frequency offset and compatibility improved. It is felt this flexibility would be more useful in addressing the various deployment scenarios. Therefore the roll-off factor of 0.22 should be retained.

Maintaining the existing roll off factor will have a small impact on the transmitter performance in particular the ACLR value and a slightly larger impact on the receiver performance in terms of the ACS value. The impact on these parameters are reviewed in sections 3.3 and 3.4.

3.3 ACLR

Computer simulation have be performed on the impact of ACIR for both UL and DL with the new chip rate and are presented in Annex A. Simulations are also provided showing the impact of the change of chip rate from 4,096 to 3,84 Mchip/s and the change of roll-off factor.

From the results presented in figure 3 we can conclude that the ACLR value will be improved by 0,5 to 0,7 dB with new chip rate of 3,84 Mchip/s. Also can be seen that the roll-off factor change from 0,22 to 0,3 does not bring any significant impact to the performance of ACLR.

Hence it can be stated that from an implementation perspective and with new chip rate the ACLR performance can be improved <1dB compared to chip rate of 4.096Mcps.

3.4 ACS

The chip rate change will have a positive impact to receiver sensitivity performance. By keeping the 5 MHz channel spacing and roll-off 0,22 the simulated improvement of adjacent channel selectivity is in the range of 2 dB depending on actual filter response. If the roll-off is changed to 0,3 all this gain can not be utilized, and the performance would be unchanged. This result also supports retaining the current roll-off in order to achieve a higher ACS value to improve system performance.

Hence it can be stated that from an implementation perspective and with new chip rate the ACS performance can be improved 2 dB compared to chip rate of 4.096Mcps.

3.5 Reference Sensitivity

This item refers to TS25.101(v1.0.0) 7.3 Static reference sensitivity level, as well as TS25.104, the equivalent for BTS.

TSGR1#5(99)677 is proposing modification of the frame structure from 16 slots per frame to 15, keeping the frame length, slot structure, and number of chips per symbol constant, as well as changing the chip rate from 4.096Mcps to 3.84Mcps. In theory the chip rate change does not have any impact to reference sensitivity due the fact that both processing gain and noise BW will be affected by the same amount, and hence they cancel each others impacts. Changing frame structure may affect the required Eb/No of each service, and this requires computer simulation with new parameters. After finishing the computer simulation, specification of sensitivity should be fixed according to the same way as proposed in TSGR4#1(99)012 and TSGR4#4(99)204.

4 Effects of 3.84 Mcps on the TDD mode

Following the general philosophy of harmonisation between the FDD and TDD mode most changes mentioned in section 3 are also applicable to the TDD mode.

4.1 Channel spacing

Refer to section 3.1.

4.2 Roll-Off Factor

Refer to section 3.2

4.3 ACLR

Computer simulations to determine the ACLR requirements for the TDD mode are ongoing. However it is anticipated that the change in the chip rate will not lead to any significant change in the results (as already shown for the FDD mode). ACLR requirements for the TDD mode will be defined in the ongoing standardisation process off WG4.

4.4 ACS

Refer section 3.4, although the performance gains may not be numerically the same as stated in section 3.4.

4.5 Reference Sensitivity

Refer section 3.5.

Annex A

Figure 1 and figure 2 show the UL and DL capacity loss with respect to ACIR

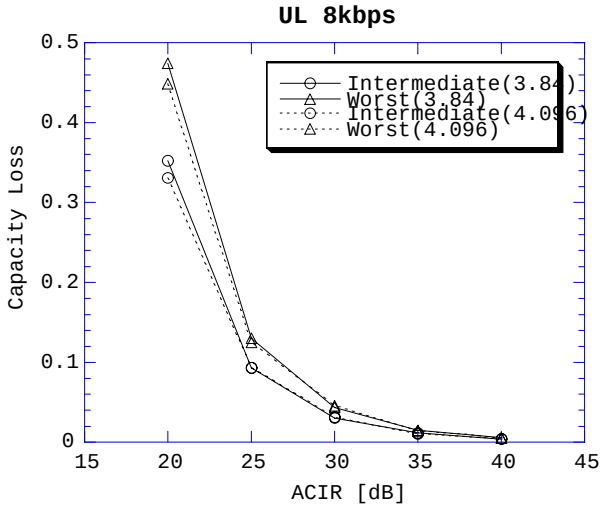

Fig. 1 Up-Link Capacity Loss with respect to ACIR

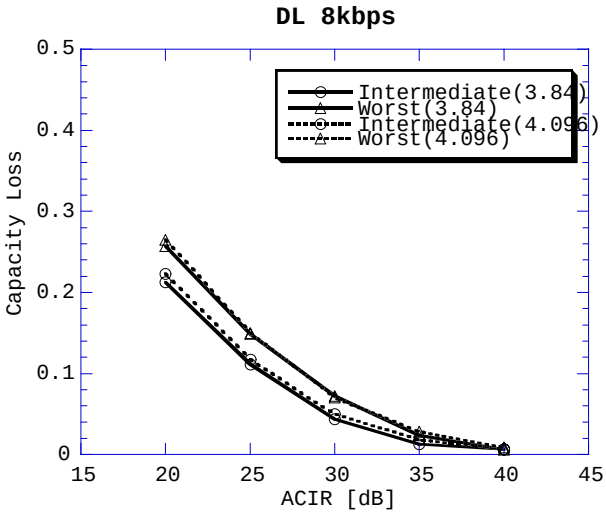

Fig. 2 Down-Link Capacity Loss with respect to ACIR

Figure 3 shows the impact of ACLR on the roll-off factor.

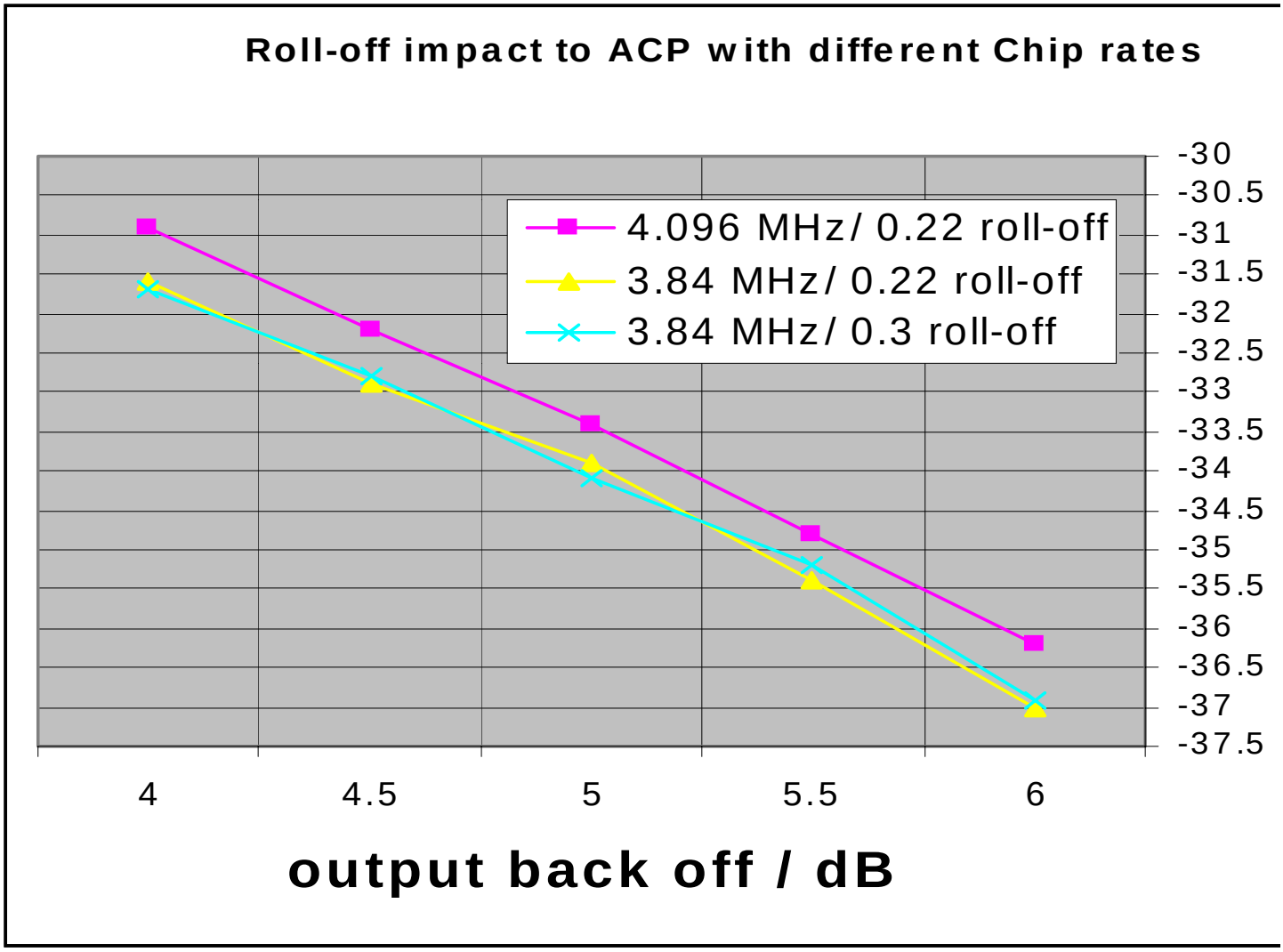

Fig. 3 Impact of chip rate change and different roll-off to ACLR

Table 1 and 2 are the parameters used in the UL and DL simulations.

Table 1 Up-Link Simulation Parameters

MCL	70 dB
BS antenna gain	11 dBi
MS antenna gain	0 dBi
Log normal shadowing	Standard Deviation of 10 dB
# of snapshot	3000
Handover threshold	3 dB
Noise figure of BS receiver	5 dB
Thermal noise (NF included)	-103.16 dBm@3.84MHz
Max TX power of MS	21 dBm
Power control dynamic range	65 dB
Cell radius	577 m (for both systems)
Inter-site distance	1000 m (for both systems)
BS offset between two systems (x, y)	Intermediate: (0.25 km, 0.14425 km) -> 0.289 km shift Worst: (0.5 km, 0.2885 km) -> 0.577 km shift
User bit rate	8 kbps
Activity	100%
Target Eb/I0	6.1 dB
ACIR	20, 25, 30, 35, 40 dB

Table 2 Down-Link Simulation Parameters

MCL	70 dB
BS antenna gain	11 dBi
MS antenna gain	0 dBi
Log normal shadowing	Standard Deviation of 10 dB
# of snapshot	3000
Handover threshold	3 dB
Noise figure of MS receiver	9 dB
Thermal noise (NF included)	-99.16 dBm@3.84MHz
Max TX power of BS	43 dBm (30 dBm for each traffic channel)
Power control dynamic range	25 dB
Cell radius	577 m (for both systems)
Inter-site distance	1000 m (for both systems)
BS offset between two systems (x, y)	Intermediate: (0.25 km, 0.14425 km) -> 0.289 km shift Worst: (0.5 km, 0.2885 km) -> 0.577 km shift
User bit rate	8 kbps
Activity	100%
Target Eb/I0	7.9 dB
ACIR	20, 25, 30, 35, 40 dB