CP-150843: UICC proactive polling and eDRX

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Background info

- What is UICC proactive polling?
  - ME sends STATUS command to the UICC to check if there is any pending proactive command
  - See ETSI TS 102 221 subclause 14.6.2 (referenced by TS 31.101)
- How often does UICC polling occur?
  - Default value for UICC polling interval is 30 seconds
  - UICC can change it using POLL INTERVAL proactive command, and disable it using POLLING OFF proactive command
  - ME and UICC can negotiate it using Poll Interval Negotiation procedure (from Rel-12 onwards)
- UICC proactive polling is **expensive** in terms of power consumption
  - UICC consumes up to 10mA for the duration of the STATUS command
  - ME also provides the clock to the UICC and monitors response from the UICC
- Use of UICC proactive polling
  - In practice, proactive polling is used for time tracking by some UICCs (e.g., to initiate a procedure after a certain time)
  - This is **not** the intended purpose of this mechanism. Correct alternative is the TIMER MANAGEMENT command
    - TIMER MANAGEMENT command exists since Rel-99 for the UICC to track time
    - Corresponding mandatory test case => must be supported by all terminals
    - Does not require ME to send periodic commands to the UICC

UICC proactive polling and eDRX

- Power savings from eDRX are greatly reduced if ME has to poll UICC e.g. every 30 seconds
- CT6 agreed CRs (C1-150636 and C1-150637) to allow ME to suspend UICC proactive polling for the duration of eDRX cycle
- Issue is that ability for ME to do this is disabled by default in the UICC:
  - Whether ME is allowed to suspend polling while in eDRX is tied to value of “extended DRX cycle” bit in the USIM (b4 in in EF_{AD})
  - Bit was previously reserved -> it is set to 0 in existing UICCs
  - In agreed CRs, bit set to 0 means the ME is not authorized to suspend polling
- Consequently, MEs which support eDRX won’t get the full power savings from eDRX unless the operator:
  - Provides a new UICC with the bit set to 1.

  OR
  - Updates the UICC contents OTA to change the bit from 0 to 1

Proposed way forward

- Revise C6-150636 and C6-150637 to have the ability to suspend UICC proactive polling while in eDRX enabled by default
  - b4=0: the ME is ~~not~~ authorized to modify the polling interval and/or disable the UICC interface during extended DRX cycle.
  - b4=1: the ME is not authorized to modify the polling interval and/or disable the UICC interface during extended DRX cycle
- Corresponding revisions are submitted in CP-150844 and CP-150845

Thank you

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